BBC ETD

INFORMATION SHEET

FERRITE CORE-STORES

(This note is based on information supplied by C.E.X.B's department)

Facilities for the storage, and subsequent retrieval, of data in the form of binary-coded electrical information form part of certain modern BBC equipment, including some computers.

Any electro-mechanical system, such as magnetic tape, involves loss of time in locating the information required, as unwanted information must be scanned before the required section is reached. Where immediate access to the stored data is needed, high speed electronic switching is used. "Ferrite core-stores" are widely used for such purposes. As the name indicates use is made of a number of individual pieces of magnetic material which form the cores of electro-magnets. Each core is capable of indicating, by the polarity of its remanent magnetism; either state (0 or 1) of a binary digit (bit). A number of these cores are grouped in assemblies during manufacture a few square inches in size termed a "matrix-plane". A single matrix is capable of accepting or yielding only one "bit" of information at a particular instant in time; in practical systems, groups of bits called "words" have to be handled simultaneously. Thus a complete store system will contain several matrix-planes in one or more stacks. Cores in the same relative position in each matrix are selected together.

SQUARE-LOOP FERRITES

The magnetic materials used for the storage elements are classified as "square loop ferrites" because of the shape of the hysteresis loops. The main characteristics of these materials are:

(a) They are magnetically bi-stable. A magnetising force of saturation strength is required to change the polarity.

(b) Magnetising forces of less than saturation strength have negligible effect on the remanent flux.

(c) The remanent flux is not significantly weaker than that existing when a saturating magnetic force is applied.

Fig. 1 shows a typical hysteresis loop for square-loop ferrite material with points A and B indicating the amount of remanent magnetism. The positive point A could represent the binary figure 1 and the negative point B the binary figure 0. A change from 0 to 1 is made by subjecting the material to a magnetising force of saturation strength and appropriate polarity. Current I produces the magnetising force to cause saturation. With this current applied the flux density reaches point C and drops to point A when the current is removed. Likewise a reverse current of magnitude I would give a flux density of D with a remanent flux of B.

MATRIX PLANE

The cores or elements in a matrix-plane take the form of small rings or beads of ferrite material threaded with wires. The elements are arranged in a grid pattern as illustrated in Fig. 2.

Only 9 cores are shown in the diagram but typical matrix planes in use have 25 to 64 horizontal and vertical rows thus providing storage capacities ranging from 625 to 4096 bits.

OPERATION OF X AND Y WIRES

A current pulse applied to any of the X or Y wires will induce a magnetic field in the elements threaded by the wire and if the current pulse is of sufficient strength to cause saturation (I in Fig. 1), all elements in the row will have a remanent polarity according to its direction. In order to saturate only one core in the matrix the appropriate X and Y wire should be fed with a current of half the value required for saturation (known as a half current and equal to I/2). These two half currents have the same effect magnetically as a full current through one wire. This is illustrated in Fig. 2 where X_2 and Y_2 have a half current and core number 5 is thereby "switched". Other elements (in X_2 row and Y_2 row) , being subjected to a field of only half saturation strength, will retain their original polarity. Pulses applied to individually selected X and Y wires will switch any element required thus providing what is called "random access". As normally used, information may be fed into, or retrieved from, only one element in the whole matrix plane at any time.

"INHIBIT WIRE" AND "WRITING-IN" PROCESS

The switching of elements to the 0 or 1 state by co-incident currents in X and Y provides a means of writing information into a matrix-plane. This is done by arranging for the direction of the half-current pulses to be one way when a 1 is to be written in and reversed when a 0 is required.

When a number of matrix-planes are operated on simultaneously (i.e. when a "word" or group of "bits" is to be written in) it is more economical to connect corresponding X and Y wires of each matrix in series and operate them from one set of drive-wire circuits. To prevent all matrix-planes being switched to the same logical condition (1 or 0) each matrix-plane is provided with an additional wire which threads all cores in that matrix-plane. This is called the "inhibit" wire and its function is to modify, if required, the effect of a switch by the X and Y wires. When the information to be stored requires an element to be switched, the inhibit wire carries no current and therefore has no effect on the switching action. If the state of the core is required to be unchanged the switching action is inhibited by feeding a half-current pulse through the inhibit wire so as to oppose the action of the pulse in the X wire. Since the Y wire has a half-current only, the switching action is suppressed.

The above conditions may be summarized by the diagram of Fig. 3. An inhibit wire current of $\frac{I}{2}$ opposes the X current of $\frac{I}{2}$ and no switching action occurs.

"SENSE-WIRE" AND "READING-OUT" PROCESS

In order to retrieve stored data a further wire is included in the matrix-plane called the "sense"wire which, like the inhibit wire, threads all cores in turn, although in a different manner to that of the inhibit wire as will be seen in Fig. 4.

"Reading-out" is achieved by feeding both the X and Y wires associated with the core to be read with a half-current pulse, as in the "writing-in" but of reverse direction. If the element was switched in "writing-in" it will now undergo a complete magnetic reversal producing a pulse in the "sense" wire, whereas if it was not switched in "writing-in", no magnetic reversal will occur and only a small spurious signal will appear due to the small change of flux as shown by BD in Fig. 1. The spurious signal would not occur if the hysteresis loop had a perfectly horizontal part instead of the slight slope shown in Fig. 1.

Although the spurious pulse from each element is small compared with the pulse resulting from a polarity reversal, the sum of the current pulses from all elements subject to a half-current pulse would be sufficient to mask the wanted signal. To prevent this the "sense" wire is threaded so that pick-up from adjacent elements - both vertically and horizontally - is reversed throughout the matrix so minimising the result by mutual cancellation. Due to the method of threading used for the "sense" wire, the wanted pulses may appear in either direction so that full-wave rectification has to be used to produce a unidirectional train of pulses similar to that fed into the store originally.

Fig. 4 shows a typical arrangement of "drive", "inhibit" and "sense" wires although a practical matrix would have many times the number of cores shown.

Alternate X and Y drive wires require drive currents of opposite direction. This is to enable the "inhibit" wire to follow a back and forth path through the horizontal rows and maintain the correct polarity. The arrows shown on the rectangles representing the cores indicate relative magnetic polarities, and by following the path of the "sense" wire it will be seen that the reversal causes cancellation of the spurious pulses throughout the matrix.

Fig. 5 shows a simple arrangement of three matrix-planes each containing four cores. The two X and two Y wires are shown threading all three matrix-planes. Each matrix-plane has its individual inhibit and sense wires. Suppose a 3-bit word consisting of the binary form 101 is to be written into the three planes A, B and C respectively. A particular core in each plane is used by appropriate choice of X and Y drive wires for the half currents. All three cores (one in each plane) would be switched simultaneously but it is first necessary to apply a half current in the correct direction to the inhibit wire of plane B, to oppose the effects of the X and Y half currents, because B is not to be set to the 1 condition as a 0 condition was chosen in this example.

THE READ/WRITE CYCLE

The reading-out process causes the logical "1" information to be erased. This is known as "Destructive Readout". In the example given above A and C were in the 1 state and the cores which were holding this information have now been switched to the 0 state. Arrangements must therefore be included to re-write logical 1s after readout. This is done by following the "read" pulses in the X and Y wires immediately by "write" pulses (reverse direction), and operating the "inhibit" wire from an amplified and delayed version of the information obtained from the "sense" wire on read-out. This sequence is called the Read/Write cycle.

X AND Y WIRE GROUPING

A matrix-plane having a capacity of, for instance, 4096 elements will require internal circuitry capable of switching drive-wire currents to any one of its 64-X and 64-Y wires at a time and the most obvious way of doing this would seem to be to insert an electronic switch in each of the 128 wires. A more economic and space-saving arrangement is possible by the grouping of wires and with the use of double switching. This is illustrated in Fig. 6. On the left-hand side of the matrix the wires are formed in 8 groups of 8 wires, with the wires of each group connected together thus providing 8 connection points for the 64 wires. On the right-hand side of the matrix, all number one wires (1, 9, 17, etc.) of each group are connected together, all number two wires, and so on, so as to provide a further 8 connection points. In order to gain access to a particular wire it is now necessary to select only one of the 8 connections on each side of the matrix, i.e. a system requiring 16 switches, compared with 64 required in the original method. A similar set of 16 switches is required for the Y wires. Thus if information is to be written into, or retrieved from the X_1 Y_1 Core, switches S1 and S9 for both X and Y wires are closed.

ADDRESS SELECTION

As with any system of storage, precise control of available capacity and accurate retrieval are basic essentials. Therefore associated with every piece of data to be stored must be a reference indicating the location of the information in the store. This is known as the "address location" and is presented to the store in the form of a binary-coded signal which presets a number of high-speed semi-conductor switches, and so routes the drive-wire pulses to the appropriate X and Y wires. The circuitry performing this function is termed the "address decoding" unit of the store.

IMPORTANT CHARACTERISTICS OF FERRITE CORE-STORE

If the ferrite core-store method of storing data electronically is compared with other methods, including electro-mechanical processes such as tape recording, the following points emerge :

The important characteristics of the ferrite core-store are :

- Immediate access to data
- Compact
- Reliable
- Data not lost if supply voltage fails (compare the bistable)
- Expensive

Generally it is true to say that the ferrite core-store is used where a long-term memory is required (especially where the number of bits is large), but the bistable is used as a short-term memory, i.e. where the time of storage is short.

Mr. M. R. H. Scott/APC 19th January 1971

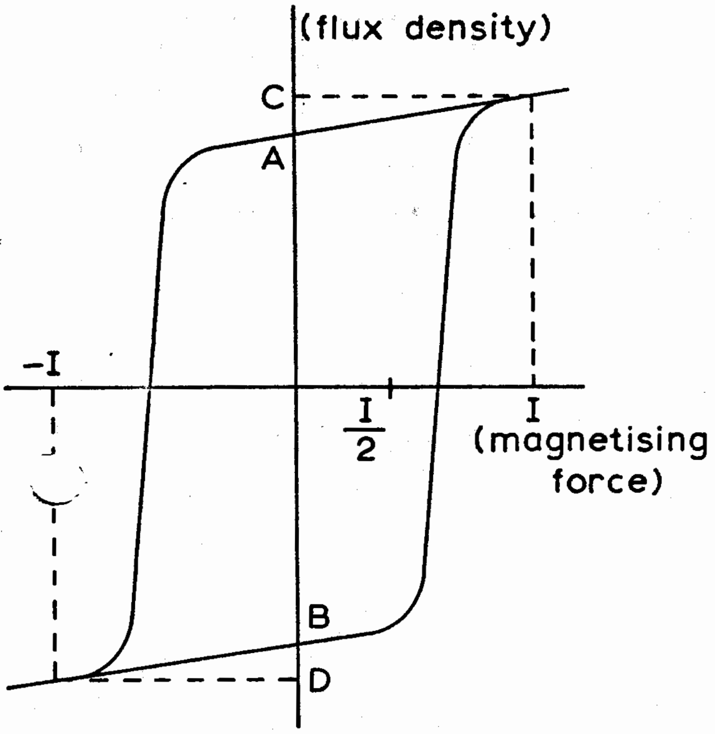


Fig. 1

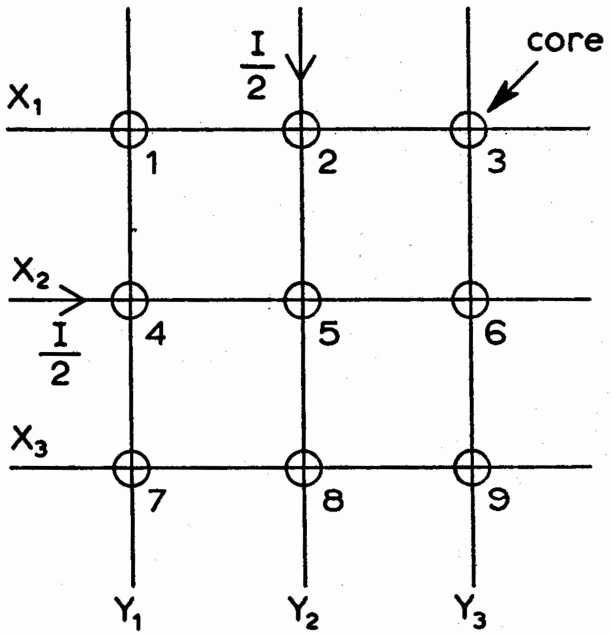


Fig. 2

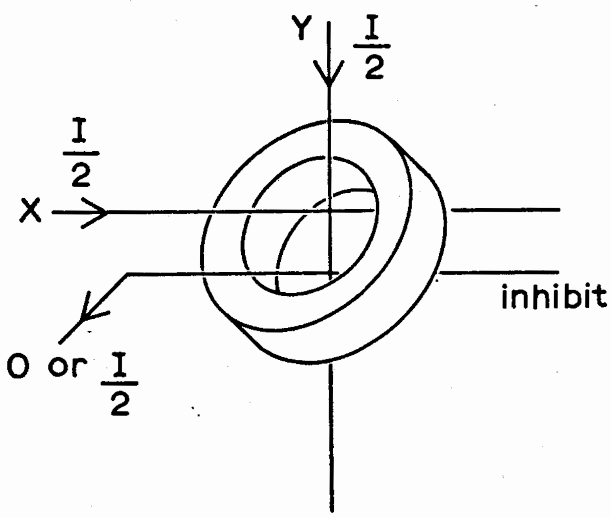
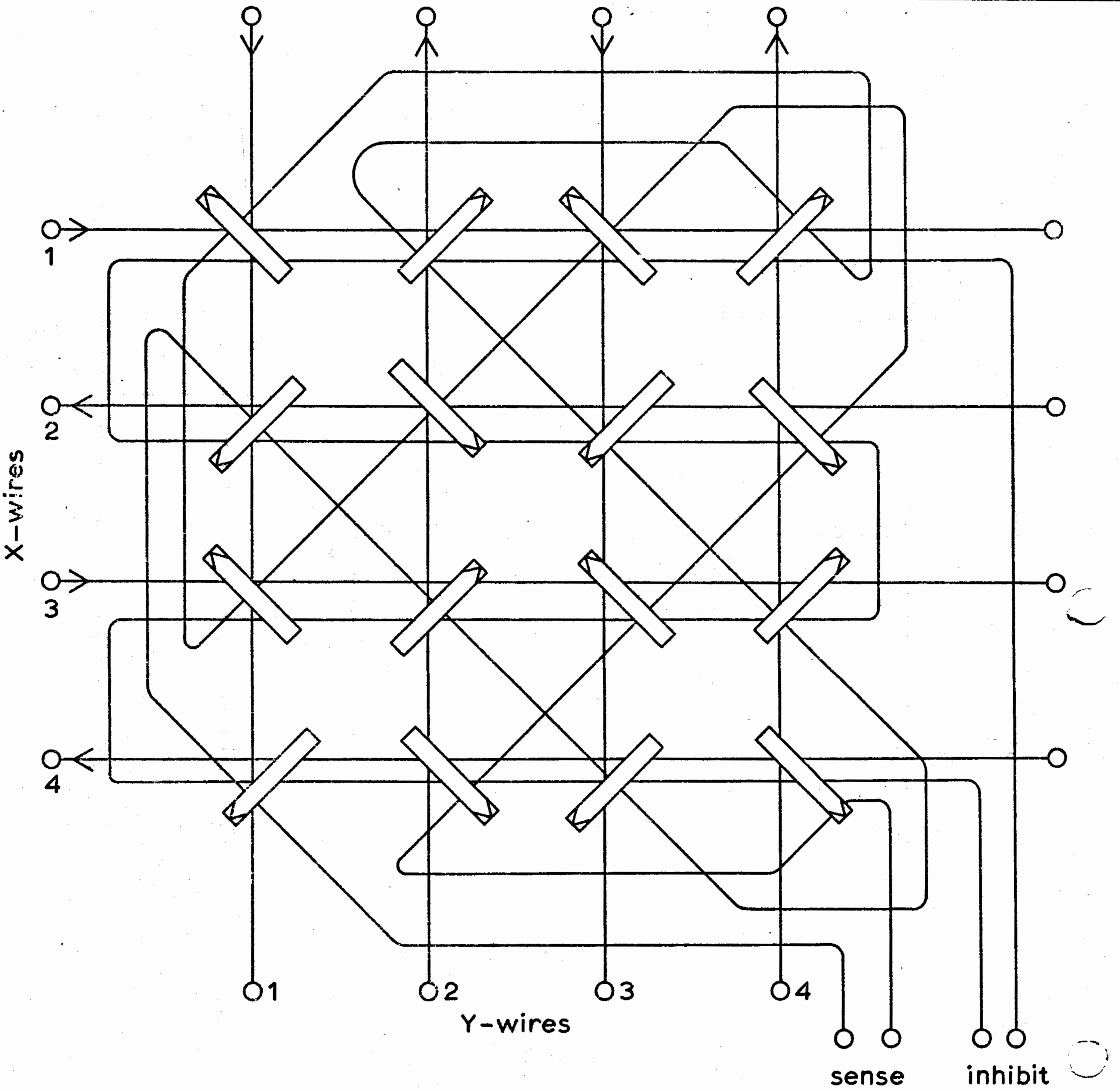
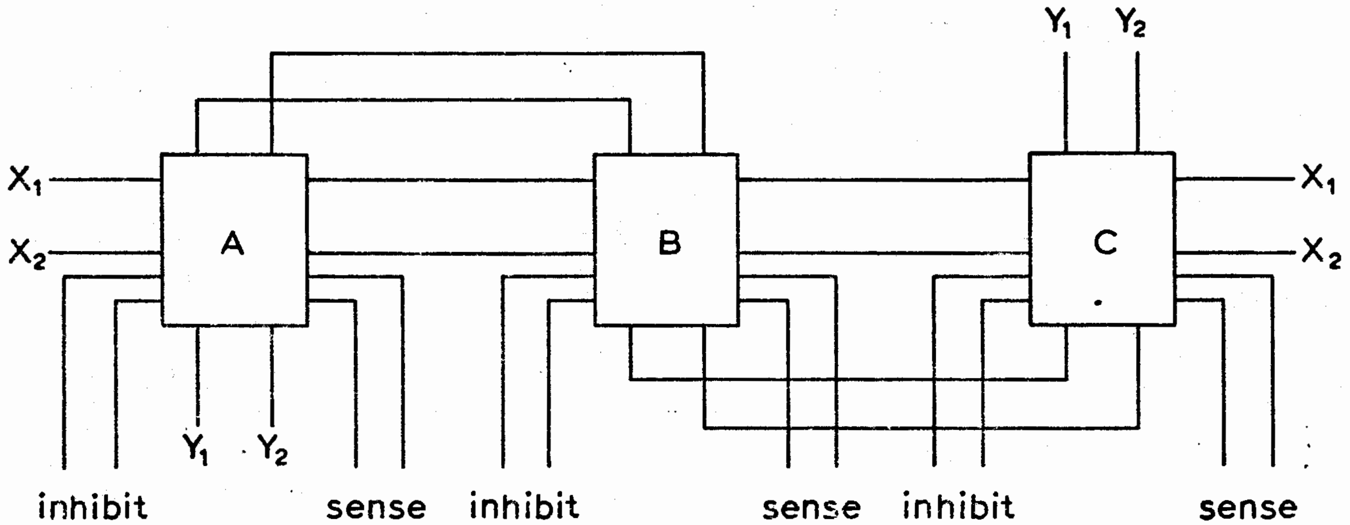


Fig. 3



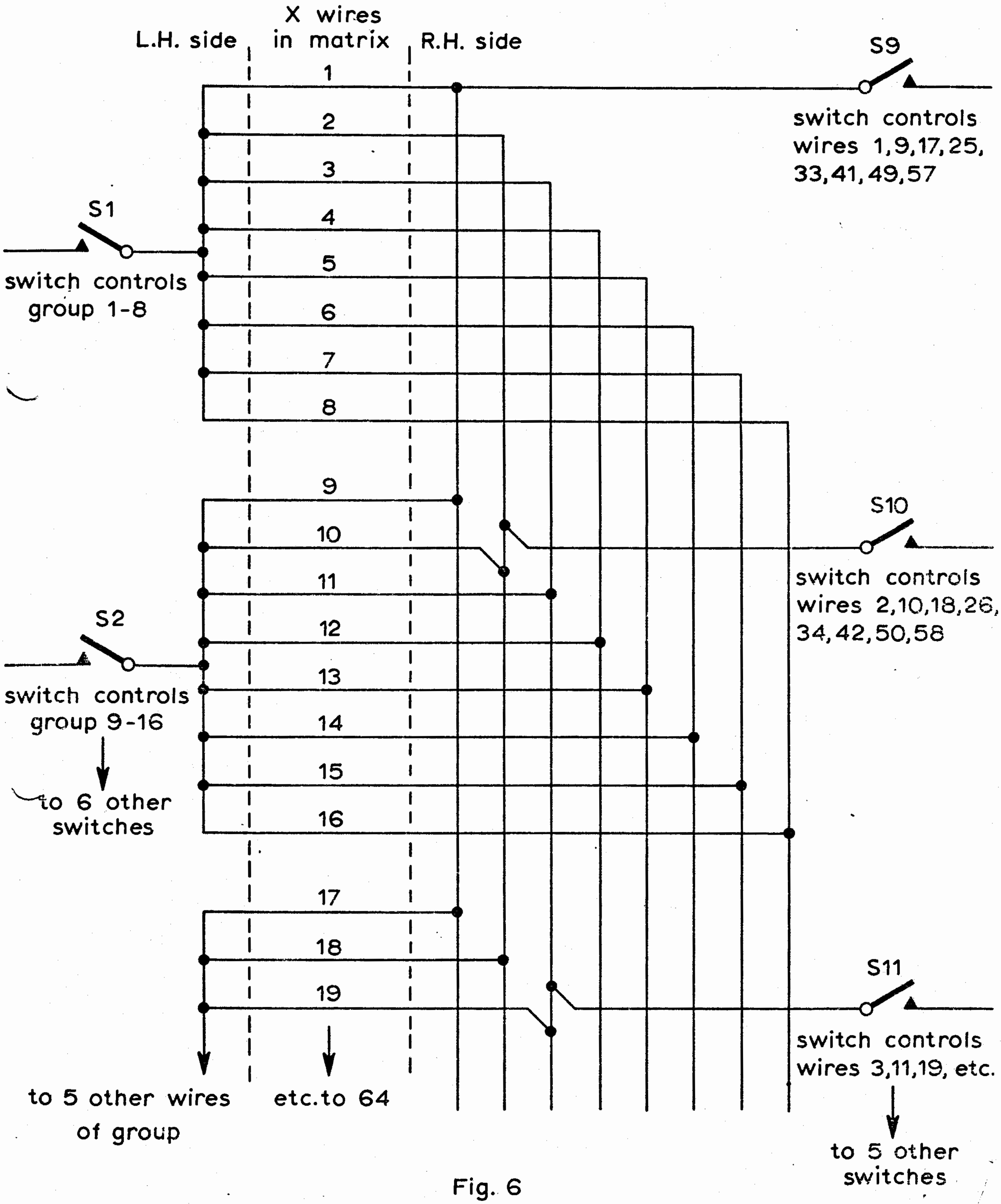
X–wires
1
2
3
4
1
2
3
4
Y–wires
sense wire
inhibit wire

Fig. 4



X_1
X_2
A
B
C
Y_1
Y_2
inhibit A
sense A
inhibit B
sense B
inhibit C
sense C

Fig.5



X wires
L.H. side
in matrix
R.H. side
S9
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
switch controls
wires 1,9,17,25,
33,41,49,57
S1
switch controls
group 1-8
S10
switch controls
wires 2,10,18,26,
34,42,50,58
S2
switch controls
group 9-16
to 6 other
switches
S11
switch controls
wires 3,11,19, etc.
to 5 other wires
of group
etc. to 64
to 5 other
switches

Fig. 6