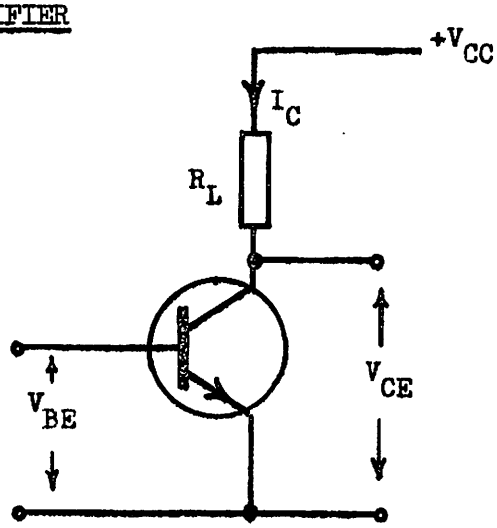
C PART 1

TRANSISTOR DC CONDITIONS AND BIAS

1. COMMON EMITTER AMPLIFIER



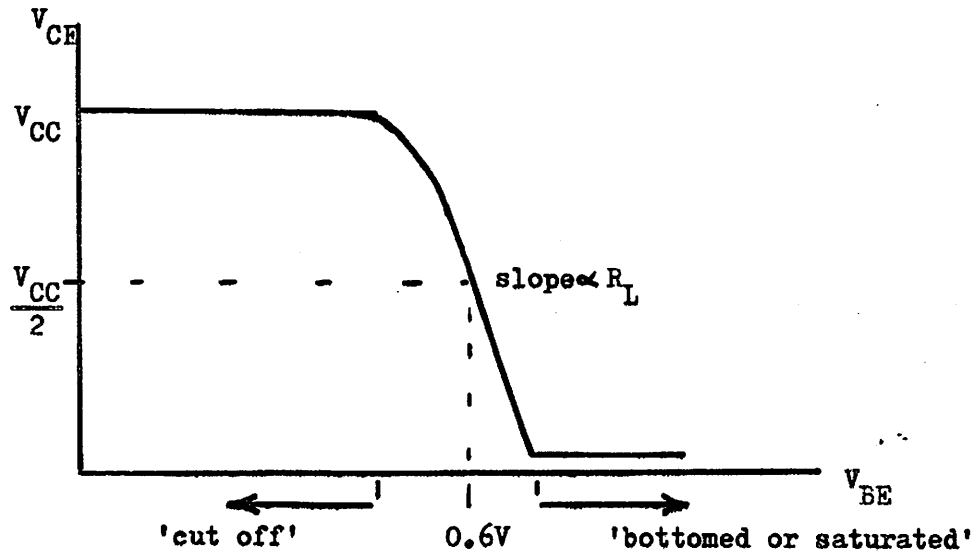


Figure 1: Voltage Transfer Characteristic

1.1 Below approximately 0.55V, base-emitter bias the transistor is 'cut-off', no collector current flows and the collector potential will be V_{CC}.

Above approximately 0.65V base-emitter bias the collector will fall to approximately 0.2V. Any further increase in V_{BE} will not result in an increase in I_C or a fall in V_{CE}. The transistor is said to be bottomed or saturated.

TRANSISTOR DC CONDITIONS AND BIAS

1.2 For maximum output swing without clipping when an a.c. signal is applied to the base the quiescent value of collector current should be such that:

$$V_{CE} = V_{RL}$$

$$= \frac{V_{CC}}{2} \quad \text{in this circuit.}$$

1.3 The transfer characteristic suggests that to give $V_{CE} = \frac{V_{CC}}{2}$, V_{BE} should be approximately 0.6V.

2. CIRCUIT CONFIGURATIONS AND DC CONDITIONS

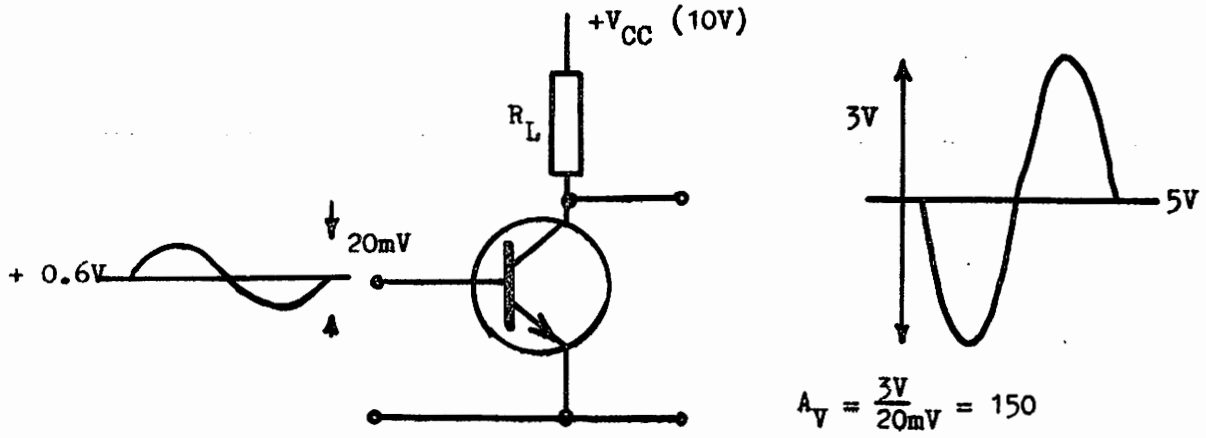


Figure 2(a): Common Emitter Amplifier

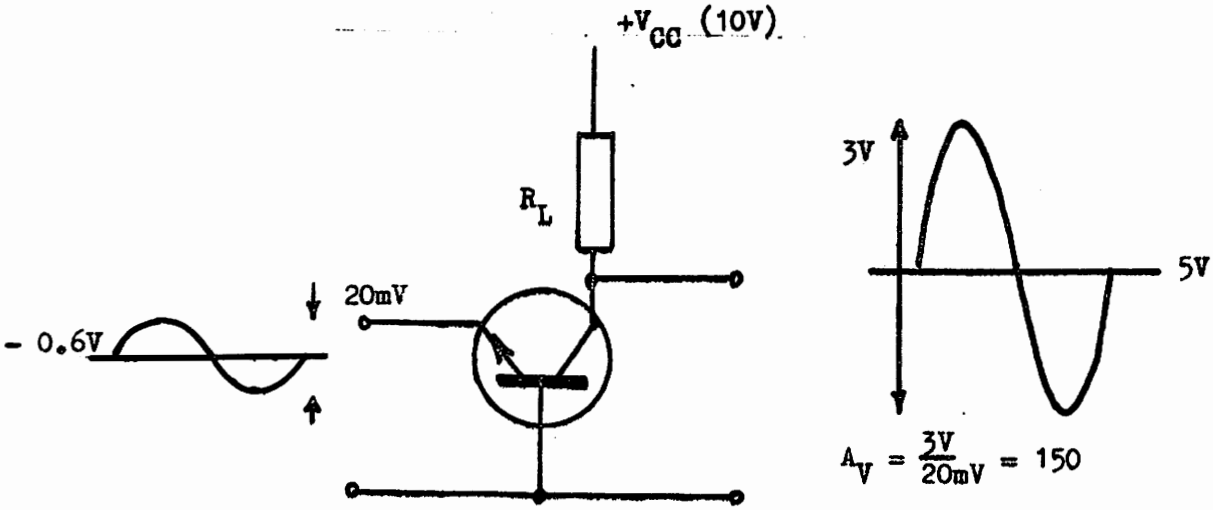


Figure 2(b): Common Base Amplifier

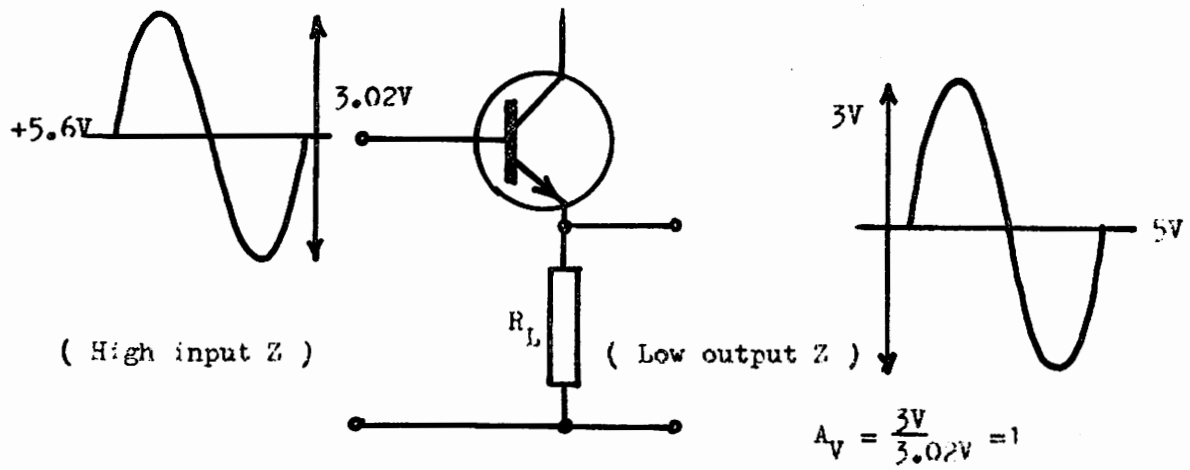


Figure 2(c): Common Collector Amplifier (Emitter Follower)

3. SIMPLE CURRENT BIAS

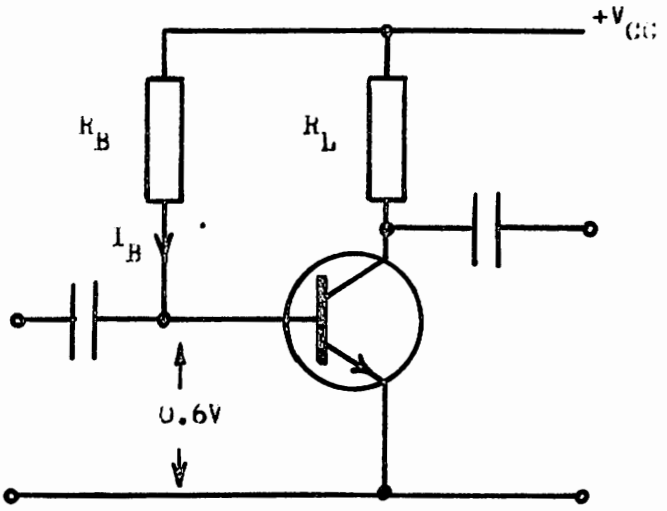


Figure 3: Simple Current Bias

3.1 For maximum voltage swing at the collector the collector d.c. potential V_{CE} should equal the p d across R_L

$$V_{CE} = V_{RL} = \frac{V_{CC}}{2}$$

and the collector current

$$I_C = \frac{V_{CC}}{2} \div R_L$$

To give this value of collector current the base current

$$I_B = \frac{I_C}{h_{FE}} \qquad \left(h_{FE} = \frac{I_C}{I_B} \right)$$

As the base-emitter potential should be 0.6V the value of the base resistor will be

$$R_B = \frac{V}{I_B} = \frac{V_{CC} - 0.6}{I_B}$$

TRANSISTOR DC CONDITIONS AND BIAS

4. FULLY STABILISED BIAS

4.1 The operating conditions (I_C : V_{CE}) of a transistor using simple current bias have the disadvantage of being dependant on the h_{FE} of the transistor. A transistor with an h_{FE} quoted as 200 can, owing to manufacturing tolerance have a value anywhere between 100 and 400.

4.2 The operating conditions are also affected by variations in the transistor's V_{BE} with temperature; -2.5mV per ^{o}C rise in temperature.

4.3 The collector leakage current will also depend on the operating temperature of the transistor althought in silicon transistors leakage currents are not significant.

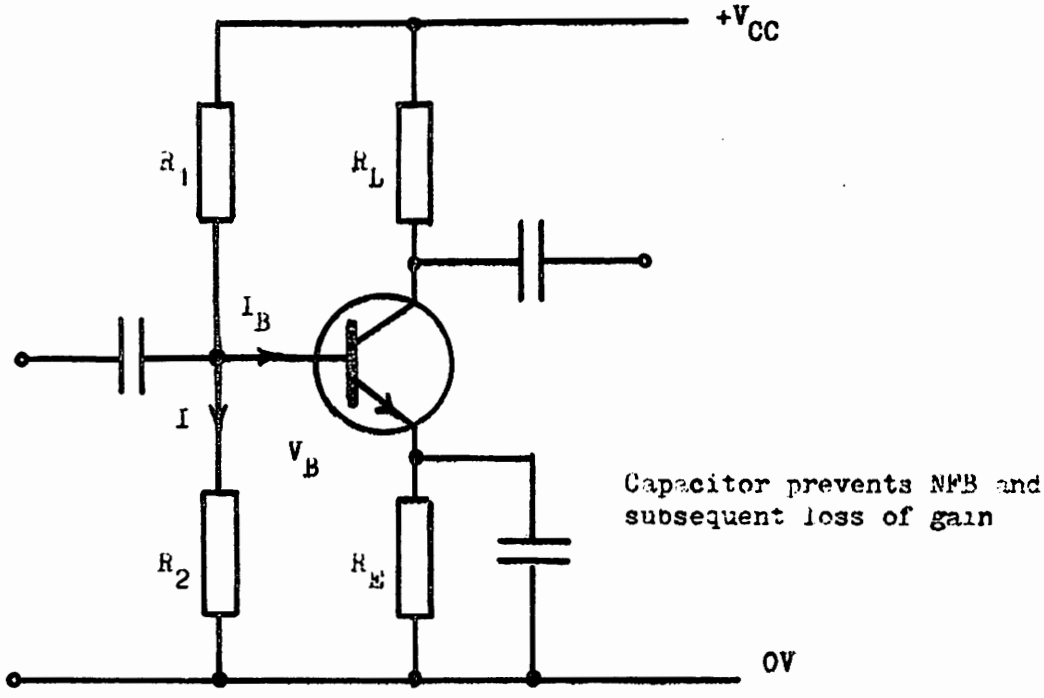


Figure 4: Fully Stabilised Common Emitter Amplifier

4.4 With reference to figure 4, R_2 is chosen to ensure I is very much greater than I_B, eg. $I \geqslant 10I_B$. This ensures the transistor base potential is set by the potential divider R_1, R_2. Hence V_B is substantially independant of I_B.

4.5 R_E is chosen to give an emitter potential ($V_E = I_E R_E$) of 1V to 2V (10% V_{CC}).

4.6 For maximum collector voltage swing without clipping $V_{CE} = V_{RL}$.

Note that $V_{CE} + V_{RL} + V_E = V_{CC}$

As $I_C \simeq I_E = \frac{V_E}{R_E}$

Where $V_E = V_B - 0.6V$.

then $I_C = \frac{V_B - 0.6}{R_E}$

V_B is set by R_1 and R_2 hence the transistor operating point I_C and V_{CE}, is now substantially independant of the transistor h_{FE}.

4.7 Any variation in the transistor V_{BE} with temperature will affect V_C. As long as V_E is much greater than the likely variation in V_{BE}, neither V_E not I_C will change significantly with temperature.

TRANSISTORS DC CONDITIONS AND BIAS

5. DC COUPLED AMPLIFIERS

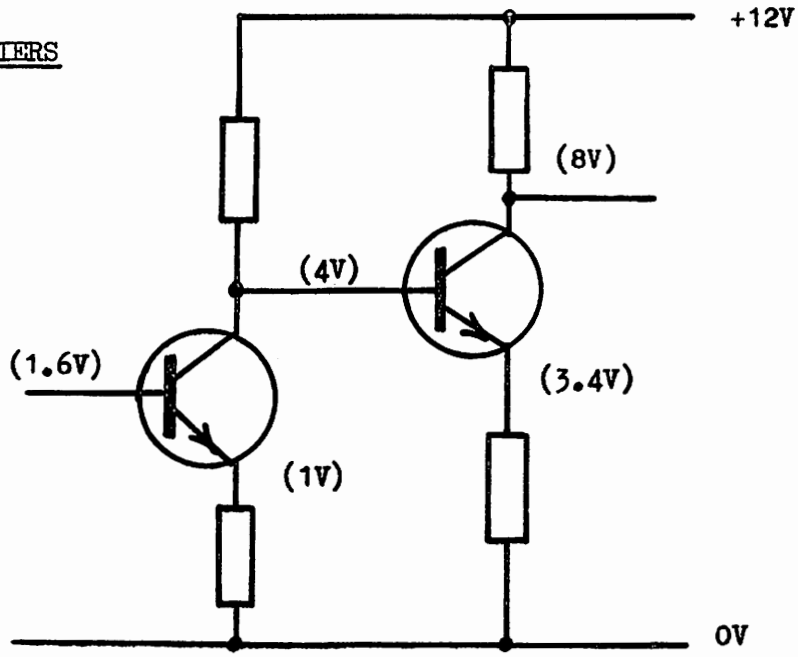


Figure 5(a): DC Coupled Amplifier

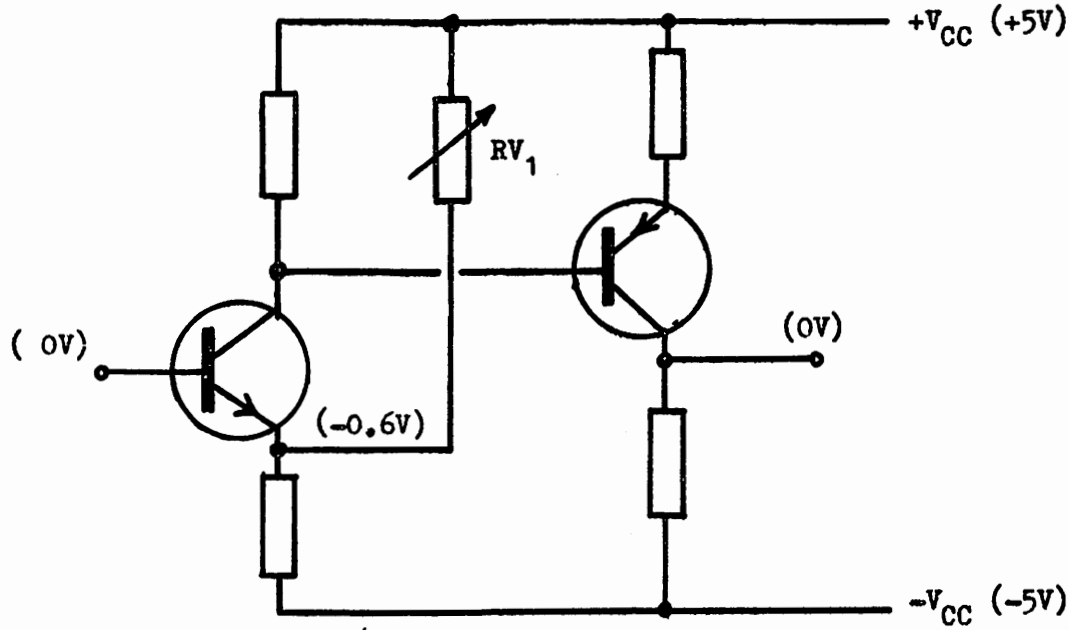


Figure 5(b): DC Coupled Complementary Transistor Amplifier

5.1 DC coupling between stages gives improved low frequency response. The use of complementary transistors and split power supplies enables the circuits d.c. conditions to be adjusted, using R_{V1} to give zero volts at the output for zero volts at the input. R_{V1} is known as an 'Offset Null' or 'Set Balance' control.

5.2 One major problem with d.c. coupled amplifier is that any variation in the voltage supplies or operating temperature of the amplifier can cause changes in the output voltage. Such changes normally occur slowly and are referred to as 'drift'.

6. DC STABILISATION USING NFB

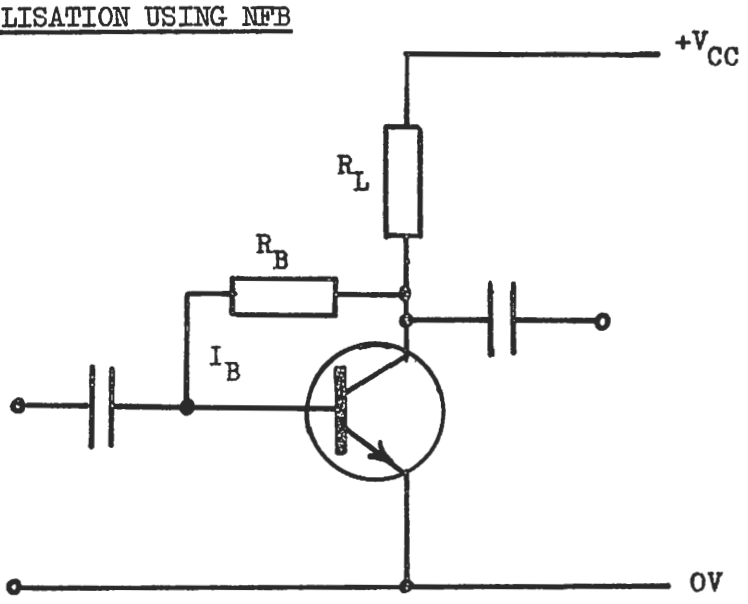


Figure 6: DC Stabilisation using NFB

6.1 If in the circuit of figure 6 the collector voltage rises above its optimum value then the potential at the top of the base resistor also rises, thus increasing the base current. This causes the collector current to rise and the collector potential to fall, reducing the original rise in potential. The feedback stabilises the d.c. conditions under which the transistor operates. In more detail

$$V_{CE} = V_{CC} - I_C R_L$$

The base current

$$I_B = \frac{V_{CE} - 0.6}{R_B} = \frac{V_{CC} - I_C R_L - 0.6}{R_B}$$

The collector current $I_C = h_{FE} I_B$

$$\text{hence } I_C = h_{FE} \times \frac{V_{CC} - I_C R_L - 0.6}{R_B}$$

$$I_C = \frac{V_{CC} - 0.6}{\frac{R_B}{h_{FE}} + R_L}$$

If the h_{FE} of the transistor is not to affect the operating point, then $\frac{R_B}{h_{FE}} \ll R_L$.

i.e. R_B should be a low value resistor.

TRANSISTORS DC CONDITIONS AND BIAS

6.2 For a given bias current using a small value of R_B the voltage applied to the top R_B needs to be low. One arrangement that gives such conditions is as follows:

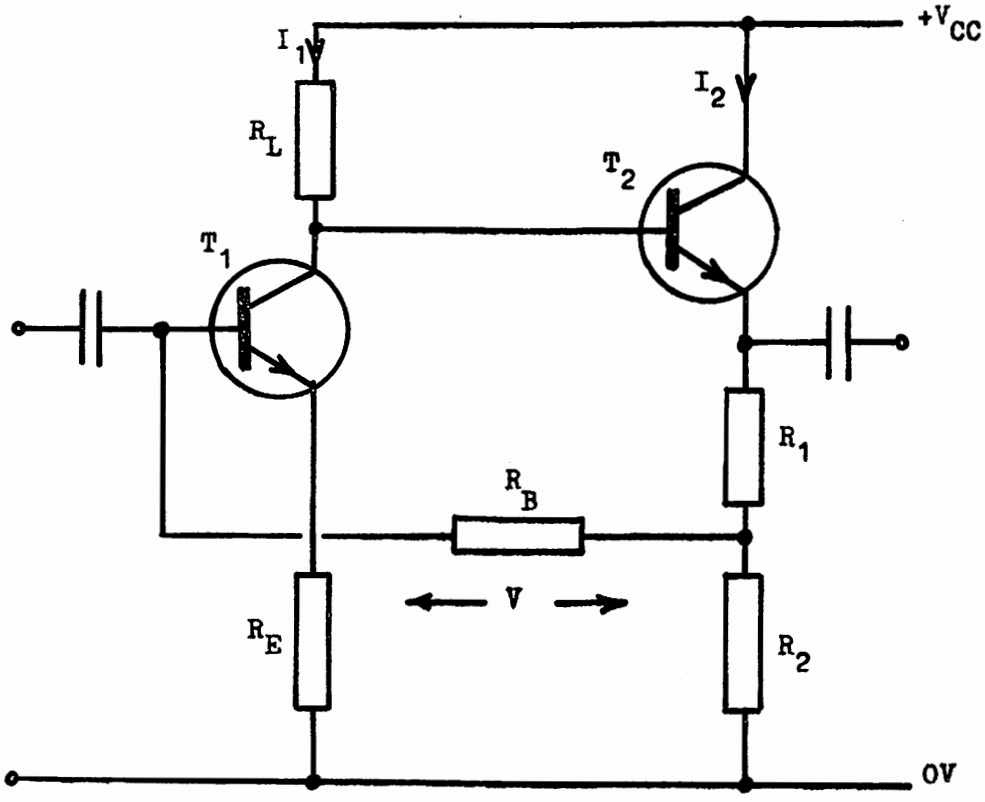


Figure 7: Multistage amplifier stabilised by NFB

6.3 R_B is normally of the order of 10kΩ and V is approximately 0.1V and can be ignored in calculations. The d.c. conditions of the circuit will be

T_1 base potential = pd across R_2

$$I_1 R_E + 0.6 = I_2 R_2$$

The sum of the potential drops across R_L, T_2 V_{BE}, R_1 and R_2 will equal V_{CC}.

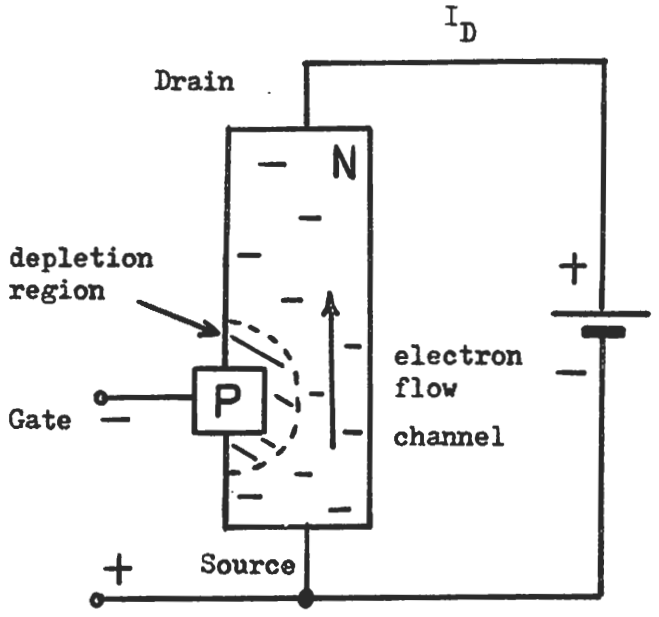
$$I_1 R_L + 0.6 + I_2 (R_1 + R_2) = V_{CC}$$

From these two equations the value of I_1 and I_2 can be obtained.

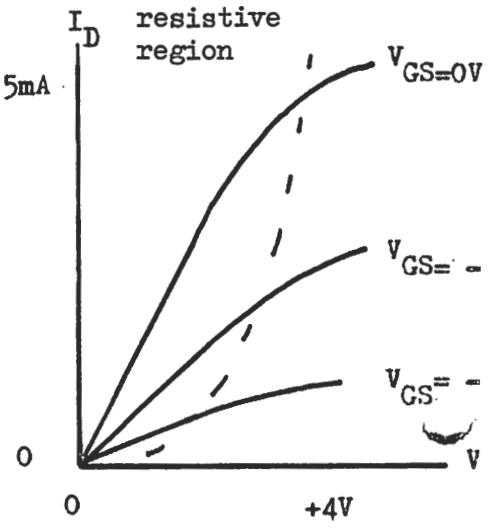
7. FIELD EFFECT TRANSISTORS

7.1 There are two main types of field effect transistor or FET. The junction field effect transistor or JFET relies on the depletion layer between the gate terminal and the main body of the transistor to give a high input impedance. The insulated gate field effect transistor or IGFET more commonly known as a metal oxide semiconductor field effect transistor or MOSFET relies on a thin film of silicon oxide to isolate the gate terminal from the source-gate channel of the transistor.

7.2 Both transistors have a very high input resistance, some tens of megohms for a JFET and up to 10^{12} ohms for a MOSFET. FETs do not suffer from shot noise and in general produce less noise than bipolar transistors and are often used in circuits where low noise is important.



N channel JFET



Typical Drain characterist for low values of V_{DS}

Figure 8: JFET Circuit Action

7.3 Figure 8 shows diagramatically how a JFET works. The width of the depletion region depends on the potential between gate and source. As the gate potential is made more negative with respect to the source, the depletion region becomes wider. This reduces the width of the channel linking the source to the drain. At low values of drain-source voltage (V_{DS}) the transistor acts as a fixed resistance between source and drain, the value of which depends on the gate

source voltage. The drain characteristics shown in figure 8 illustrate this point. In the resistive region to the left of the dotted line the characteristics approximate to straight lines.

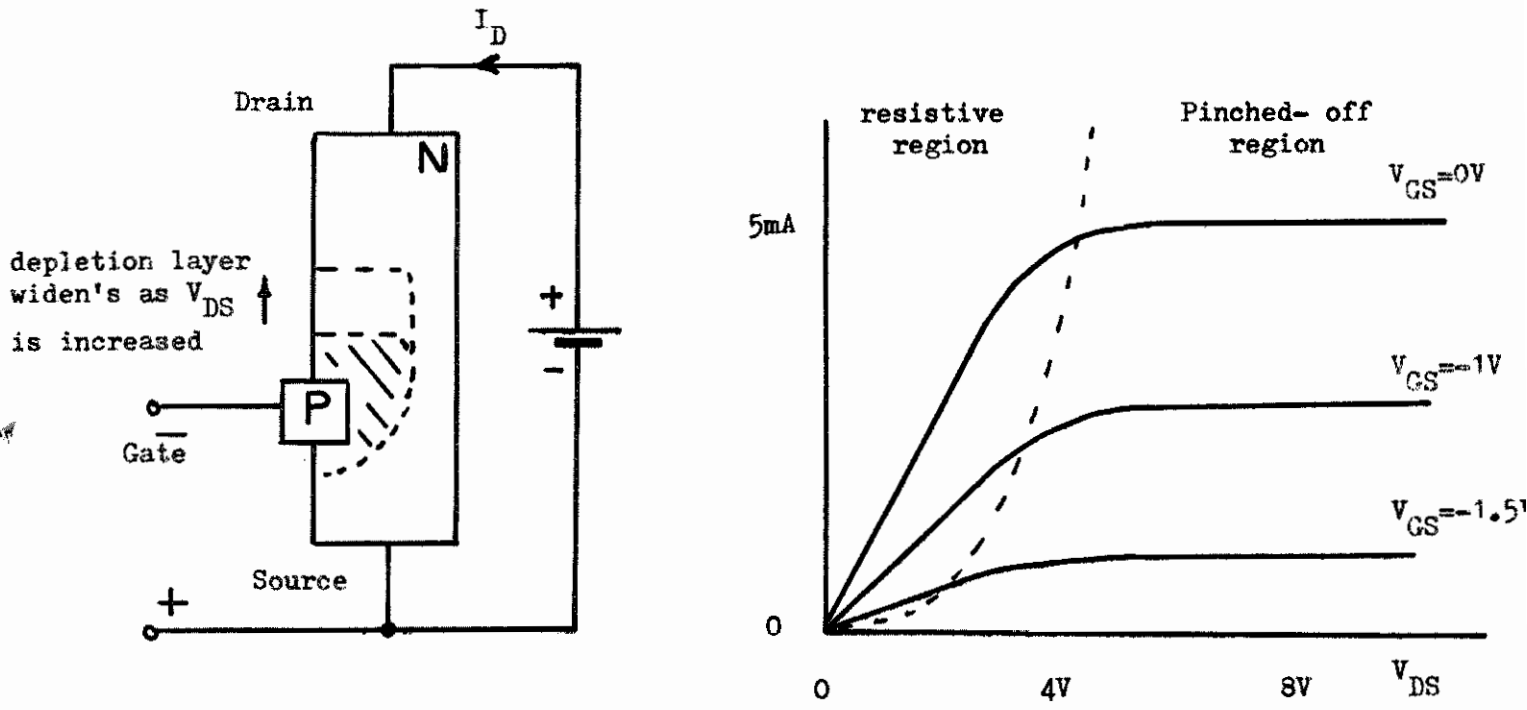


Figure 9: JFET action after 'pinch-off'

7.4 Increasing the drain-source potential beyond a certain point 'distorts' the depletion region around the gate. Above a particular drain-source voltage the channel stops reducing in width and is said to be 'pinched-off'. Further increase in the drain potential causes the depletion region to widen only in the direction of the drain. The result of this is that the resistance of the source drain channel rises with increase in V_{DS}. This increase in resistance means that beyond pinch-off the drain current becomes virtually independant of the drain-source voltage.

7.5 The gate of an FET would normally be biased negative with respect to the source to ensure that the gate source never becomes forward biased. Figure 10 shows a typical FET circuit employing automatic bias. R_G ties the gate to zero volts DC whilst maintaining a high input impedance to a.c. signals. The source current through R_S ensures the gate's d.c. potential is negative with respect to the source.

TRANSISTORS DC CONDITIONS AND BIAS

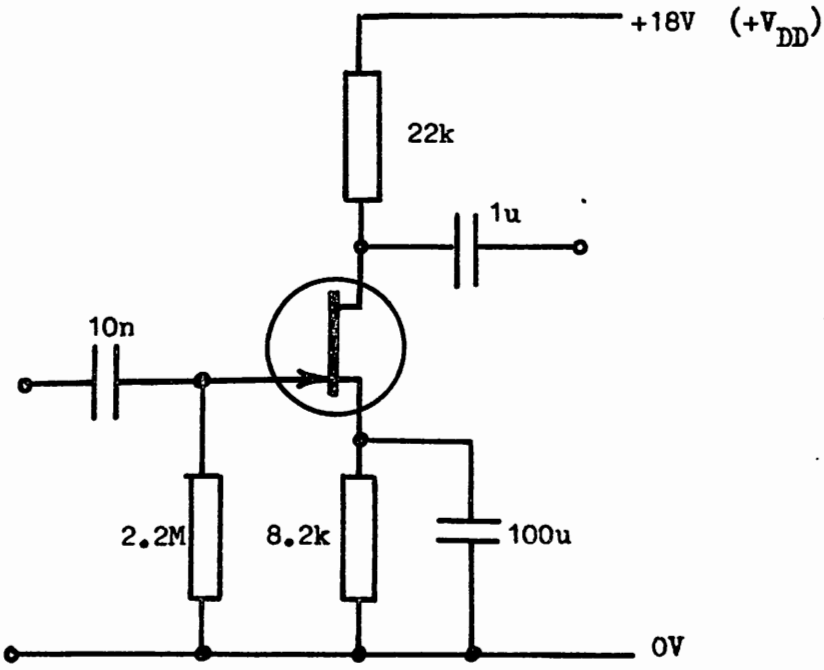


Figure 10: JFET Amplifier Employing Automatic Bias

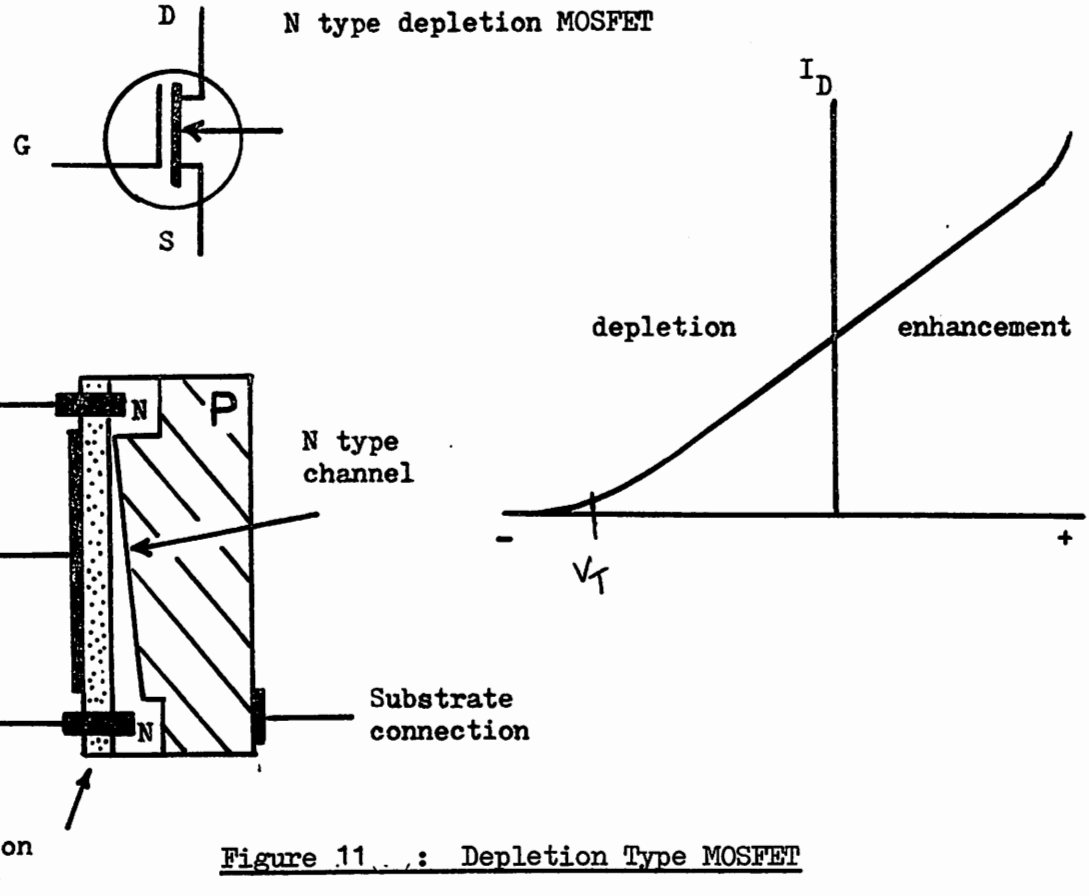


Figure 11 : Depletion Type MOSFET

TRANSISTORS DC CONDITIONS AND BIAS

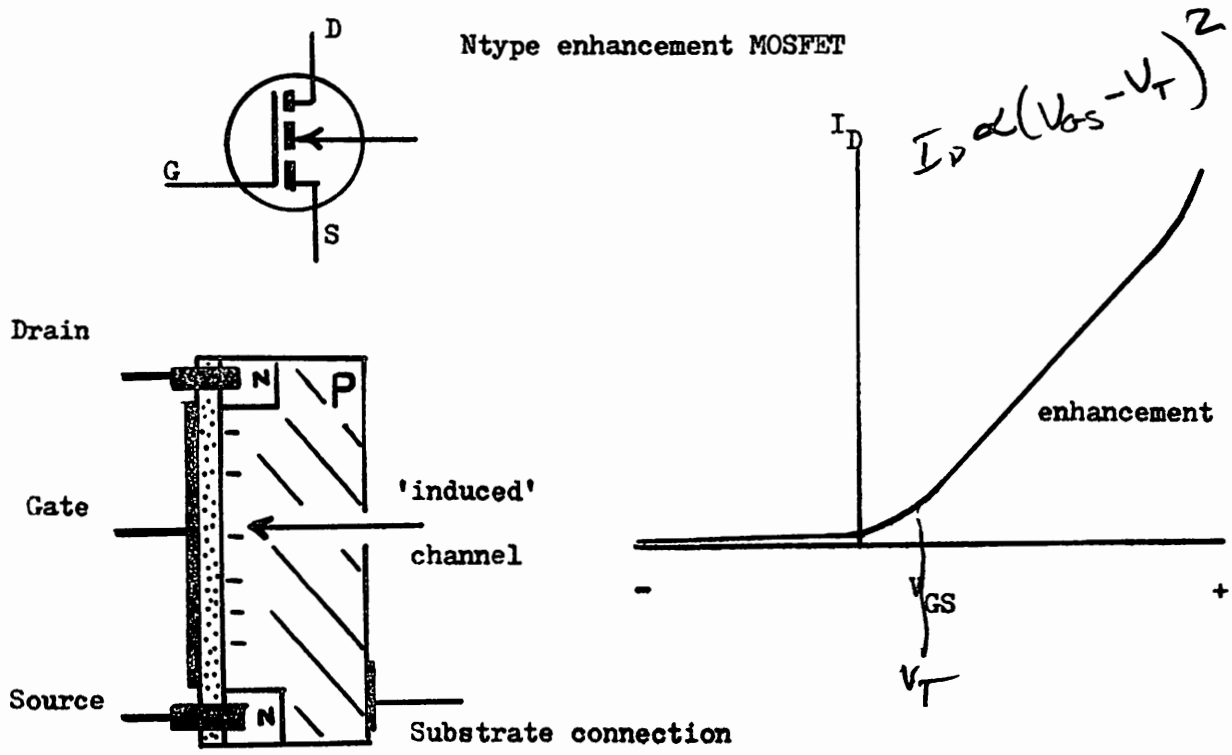


Figure 12 : Enhancement Type MOSFET

7.6 Figure 11 & 12 illustrate the construction of the two basic types of MOSFET. In the depletion type the source gate channel is 'built' into the device by suitably doping the substrate whereas in the enhancement type the channel is induced in the substrate by voltages applied to the gate. The depletion type device is similar to a JFET in that it conducts with zero gate-source bias whereas an enhancement type device will not. In all other respects the circuit action is similar to that of a JFET.

8. FET OPERATING CONDITIONS AND VOLTAGE GAIN

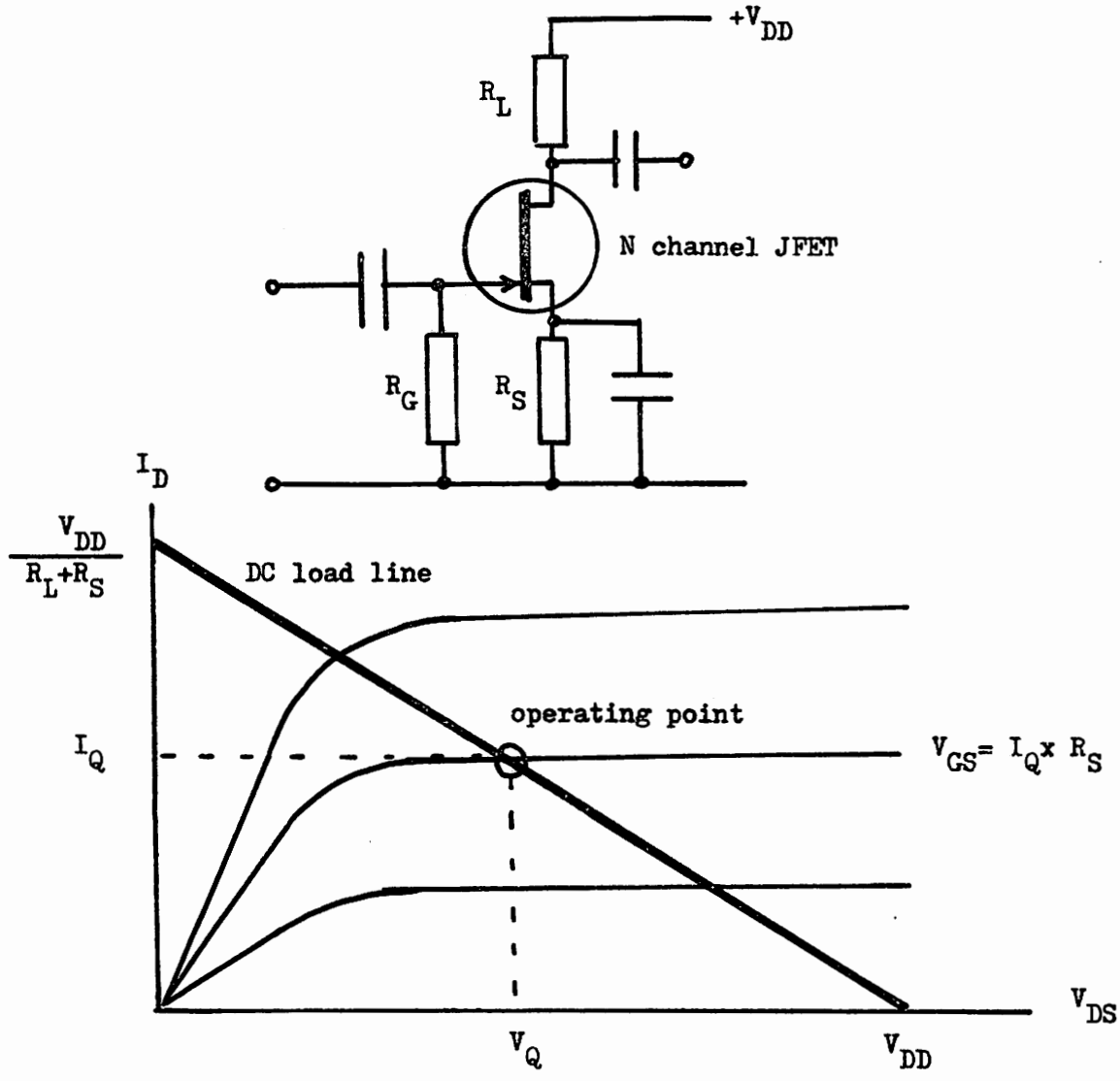


Figure 13: FET amplifier DC load line

8.1 The d.c. operating conditions for a typical JFET common source amplifier can be deduced by drawing the d.c. load line for the circuit.

With reference to figure 13

$$V_{DD} = V_{RL} + V_{DS} + V_{RS}$$

hence $V_{DS} = V_{DD} - I_D (R_L + R_S)$

It follows that when $I_D = 0$

$$V_{DS} = V_{DD}$$

and when $V_{DS} = 0$

$$I_D = \frac{V_{DD}}{R_L + R_S}$$

The DC load line will be a straight line between these two points.

8.2 The operating point on the load line will be a point where the bias V_{GS} is equal to the drain current at that point multiplied by R_S.

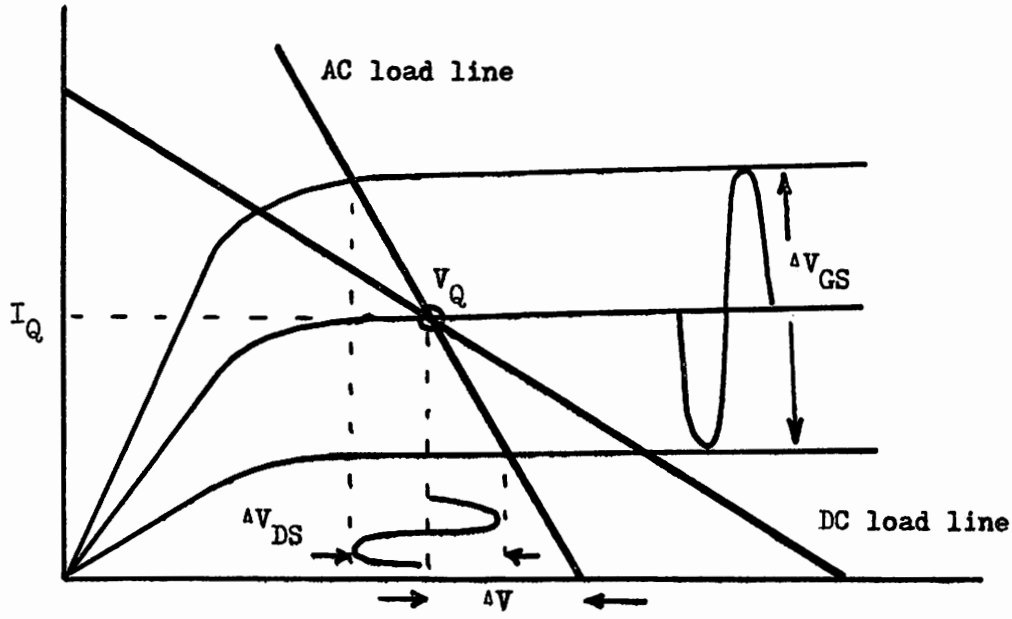


Figure 14: FET amplifier AC load line

8.3 The a.c. load line runs from the point $(V_Q + \Delta V)$ through the operating point where

$$\Delta V = I_Q \times R_{AC}$$

R_{AC} is the a.c. load on the FET and is equal to R_L in parallel with the input Z of any stage that follows. In this example

$$R_{AC} = R_L$$

8.4 The voltage gain of the amplifier

$$A_V = \frac{\Delta V_{DS}}{\Delta V_{GS}}$$

where ΔV_{GS} is the peak to peak input signal on the gate
and ΔV_{DS} is the corresponding variation in the drain potential.

SOURCE FOLLOWER

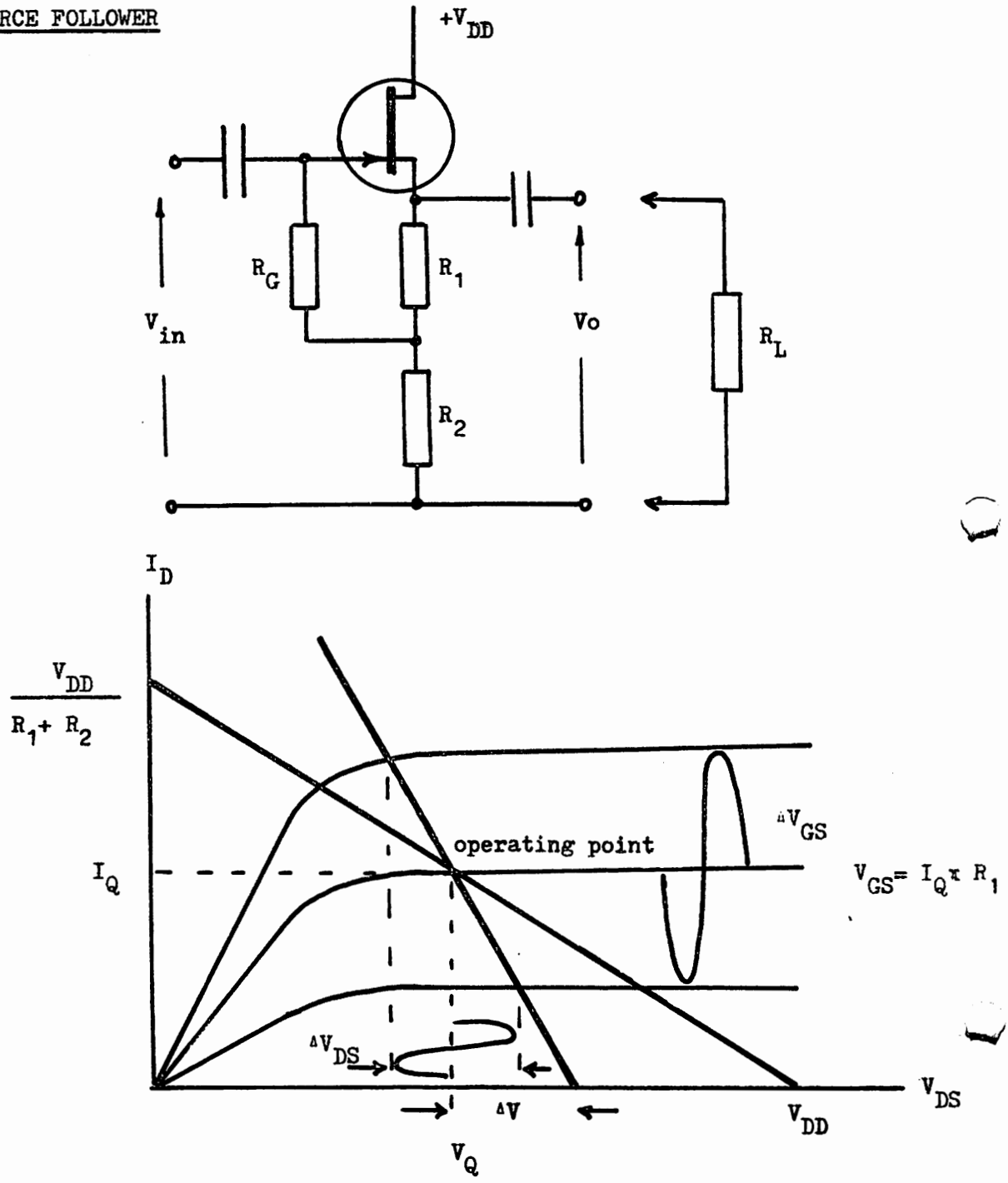


Figure 15: Load line for a source follower

8.5 Figure 15 shows a typical source follower. The DC load line runs between

V_{DD} and $\frac{V_{DD}}{R_1 + R_2}$

The operating point will be at a point on the load line where I_D

and V_{GS} are such that

$$I_Q R_S = V_{GS}$$

8.6 The ac load on the FET will comprise the source resistors $R_1 + R_2$ in parallel with load R_L.

Voltage Gain

The circuit comprising, the drain-source of the FET and the resistors R_1 and R_2 can be considered a potential divider across the input terminals hence

$$V_{in} = V_{gs} + V_o$$

V_{gs} and V_o can be obtained from the ac load line hence the voltage gain

$$A_V = \frac{V_o}{V_{in}} = \frac{V_o}{V_{gs} + V}$$

where $V_{gs} = \Delta V_{GS}$

and $V_o = \Delta V_{DS}$