

PULSE DISTRIBUTION AMPLIFIER AM4/521

Introduction

The AM4/521 accepts any of the standard drive pulses used in a Television Studio and provides ten outputs; it has a gain of 6dB.

It employs a CH1/12A chassis with index-pegs 24 and 34 and requires a PN3A/25 termination panel for mounting on a PN3/23 framework.

General Description

Input	1 V p-p pulses
Outputs	10 of 2 V p-p across 75 ohms
Output Impedance	75 ohms
Input Impedance	high
Gain	6dB
Overload Margin	3dB
Propagation Delay	14ns
Mains Power Input	6.6W (9.5VA) at 210V-250V 50-60 Hz

Circuit Description

The circuit diagram is given in Fig. 1. The input signal is amplified by an S.T.C. thin film 3-stage negative feedback amplifier labelled IC1 (see Fig. 2). The output from IC1 is fed to TR2, an emitter follower output stage with TR1 as a constant-current emitter load. The output d.c. potential is zero within 0.1 volt when loaded and this is set by R4. In the feedback circuit, R6 sets the gain and C4 adjusts the frequency response.

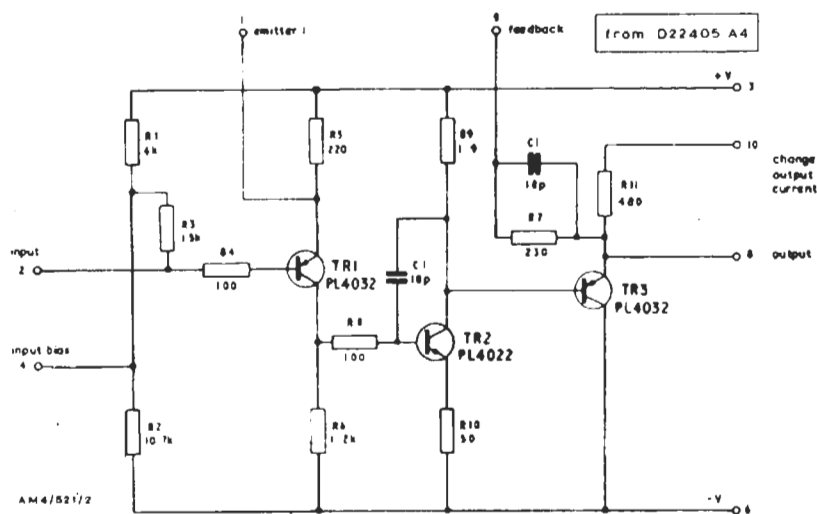
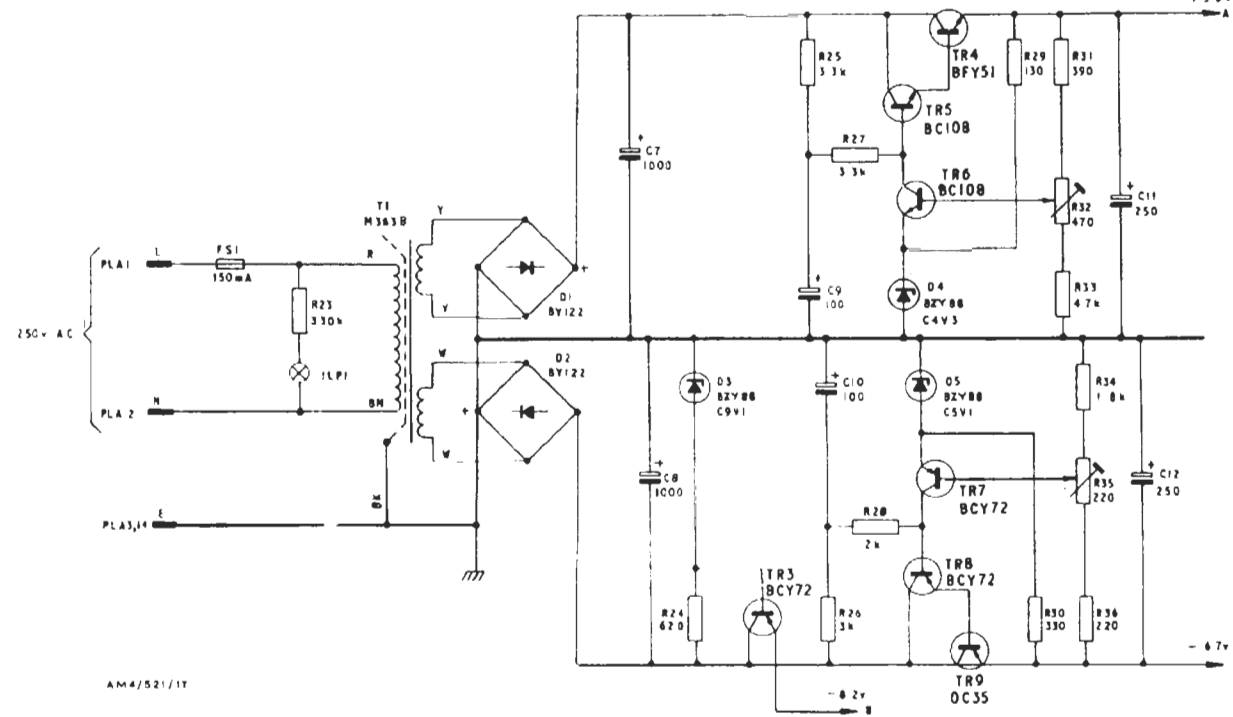
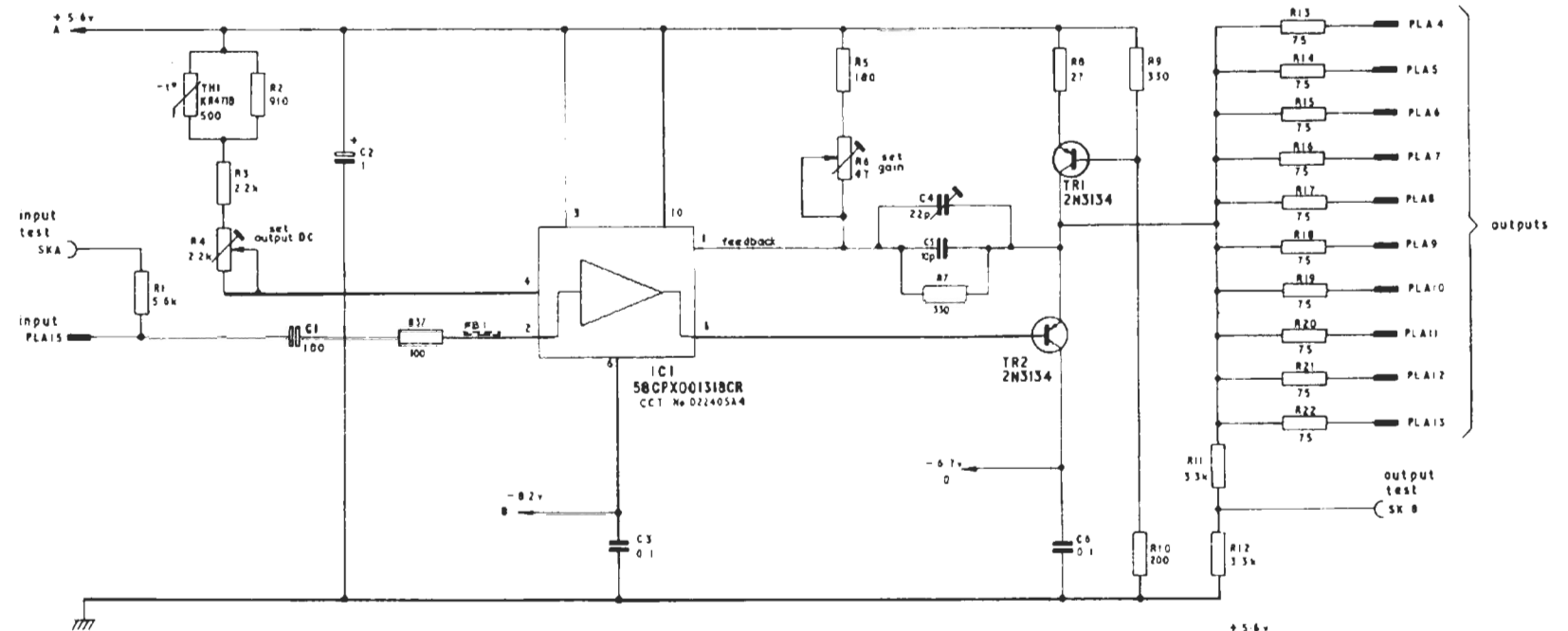


Fig. 2 Details of Thin-film Amplifier



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parts list D23B45 A4

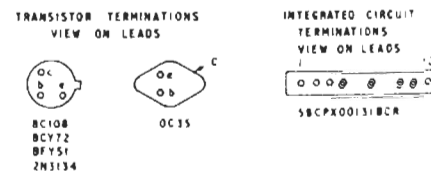


Fig. 1 Circuit of the Pulse Distribution Amplifier AM4/521

Maintenance (provisional)

Routine maintenance is not required but the following points can be noted.

1. Set the voltage across C11 to 5.6V by means of R32. Set the voltage across C12 to 6.7V by means of R35.
2. Terminate the input and all outputs in 75 ohms. Adjust R4 so that the d.c. across the terminations does not exceed 0.1V.
3. Provide an input signal at 10 kHz, 0.5V p-p. Adjust R6 to make the gain 6 dB; i.e. an output of 1V p-p across each 75-ohm termination.

4. Change the input signal to 5 MHz. Check that the gain is 6dB ± 0.1 dB and adjust if necessary by means of C4.
5. Change the input signal to 10 MHz and reduce the input level to -9 dB relative to 1V (to prevent distortion). Check that the gain is between 4 and 6 dB. Note: If any adjustments are made in tests 3, 4 or 5 then test 2 should be repeated.
6. Change the input signal to mixed syncs. Ensure that overloading does not occur until the output exceeds 2.8V p-p.

Reference

1. Designs Department Specification No. 8.325(69)