MAIN DRIVE AMPLIFIER AM5/508

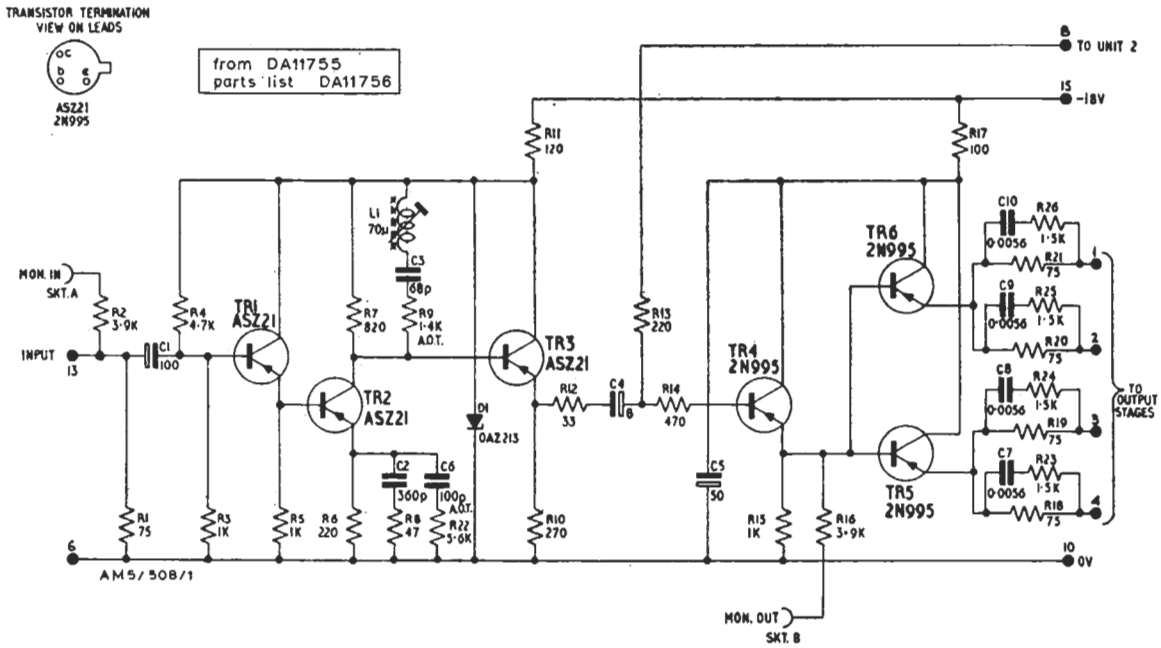

Fig. 1 Circuit of Unit 1 in the AM5/508

Introduction

This amplifier accepts a blanked picture signal[1,2] of approximatcly 0·7-volt amplitudc and a fced of mixed-synchronising pulses. It delivers the picture signal, amplified to 4 volts (measured at low frequencies) and clamped to a blanking level of −12 volts, from a source suitable to drive a capacitive load of 0·04 μF.

The amplifier comprises units of three types, one of which is quadruplicated; thus there are a total of six units, each built on a printed-wiring board accommodated in a Chassis Type CH1/12A.

Supplies of 225 mA at −18 volts, 4 A (maximum) at −13 volts and 78 mA at +6 volts are required.

General Specification

Supply Potentials	−18 V
	−13 V
	+6 V
Clamping Reference Potential	−12 V
Input-signal Amplitudes:	
Blanked picture signal (approx.)	0·7 V p-p
Mixed-synchronising pulses	2 V p-p
Input Impedances:	
Blanked picture signal	75 ohms
Mixed-synchronising pulses	High w.r.t. 75 ohms
Output-signal Amplitudes:	
Low-frequency components	4 V p-p across 0·04 μF
High-frequency components	6 V p-p across 0·04 μF
Output Impedance	1 ohm

Unit 1

This unit contains the low-level stages of the amplifier. It requires a supply of d.c. at −18 volts. The index-peg-position numbers of the chassis are 8 and 24.

The circuit of the unit is given in Fig. 1. C2, R8

compensate for the capacitive nature of the load into which the complete amplifier is designed to operate. C6, R22 and L1, C3, R9 compensate for the characteristics of associated equipment. The networks in the emitter leads of TR5 and TR6 provide further low-frequency correction.

Clamping by the feedback method is applied at the junction of C4, R14.

Each of the connections from the emitters of TR5 and TR6 is to the input of one of the four No.-3 units; the emitter circuits of the transistors are completed via these units.

potential and the sampled blanking level. The collector of TR1 is connected to the clamping point in unit 1, already described.

Some variation of the reference potential is possible by means of R13; this is a pre-set control mounted inside the unit, on the printed-wiring board.

The reference potential is fed out of the unit via TR5 and TR4. In addition to giving a low output impedance, these transistors are affected by changes of ambient temperature in a manner which offsets similar changes elsewhere in the parent equipment.

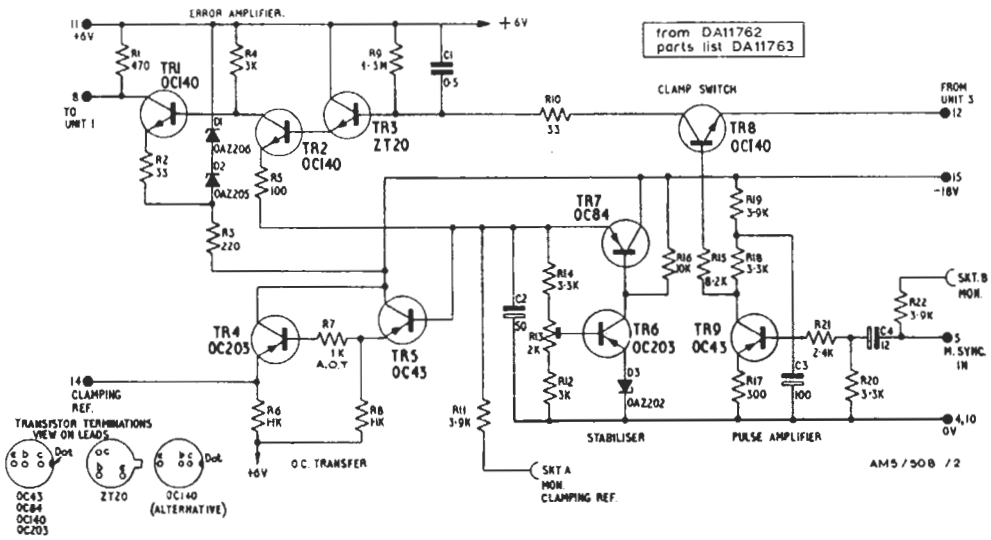

Fig. 2 Circuit of Unit 2 in the AM5/508

Unit 2

This unit contains the feedback chain by means of which clamping is effected in unit 1, together with the associated pulse circuits and reference-potential source. It requires supplies at +6 volts and −18 volts. The index-peg-position numbers of the chassis are 8 and 26.

The circuit diagram of the unit is given in Fig. 2. TR8, driven by amplified and inverted mixed-synchronising pulses, samples the potential at the output of one of the units 3 during blanking and applies the resulting error pulses, integrated by capacitor C1, to the error amplifier TR3—TR1. A stabilised reference potential, derived from the circuit of TR6, TR7, is applied to the emitter of TR2; the potential at the collector of TR2 (and therefore at the output of the error amplifier) depends on the relationship between this reference

Unit 2A

This unit is similar in function to unit 2, and is physically interchangeable with it.

The circuit diagram of the unit is given in Fig. 3. The unit differs from unit 2 mainly in having a difference amplifier TR2, TR5—TR8 in place of the error amplifier TR1—TR3 (Fig. 2). The integrated samples of blanking level from the output of one of the units 3 appear as a potential on C5 (Fig. 3) and are compared by the difference amplifier with the clamping-reference potential derived from the stabiliser. The difference potential appears at the collector of TR5 and at low impedance at the emitter of TR1, whence it is fed via pin 8 of the connector to unit 1.

R24, connected across TR10, has no effect on the operation of the unit in normal conditions, but serves to prevent damage to the amplifier in the

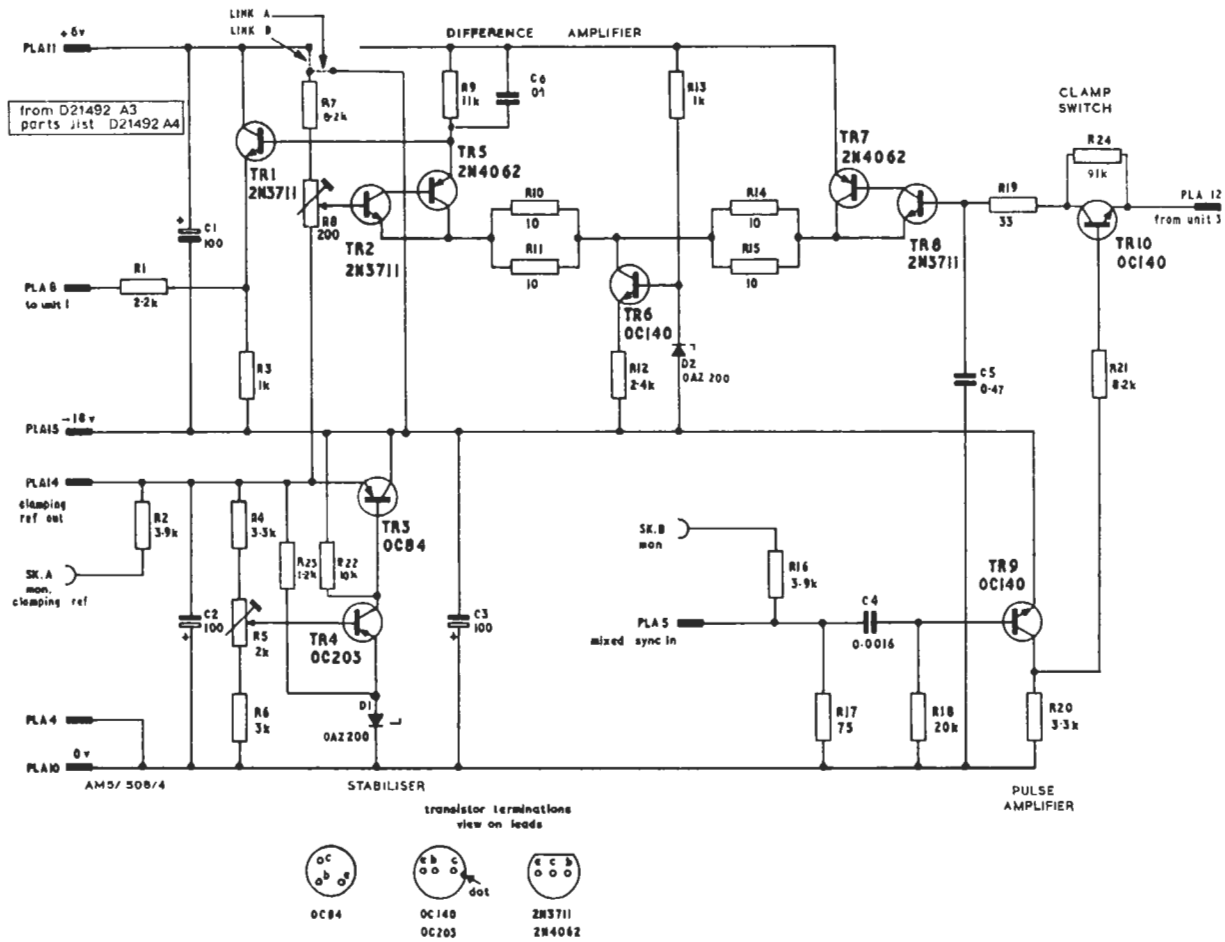

Fig. 3 Circuit of Unit 2A in the AM5/508

event of loss of incoming signal and synchronising pulses. In the absence of R24, loss of signal would, initially, result in a potential corresponding to blanking level at the output of the units 3. Loss of synchronising pulses results in prolonged non-conduction of TR10 and the potential on C5 would drift, because of leakages, so as to give a spurious difference potential and cause the signal path to assume a potential close to normal white level. This would cause heavy conduction of the power transistors with consequent risk of damage by overheating. The action of R24 is to maintain the potential on C5 close to that at the output of the units 3, i.e., close to blanking level.

A small potential (the offset potential), developed across part of R8 by current in R7, R8, appears in series with the reference potential at the base of TR2. The offset potential is variable by means of R8, and can have a polarity either aiding or opposing the reference potential, depending on whether link A or link B is used to connect R7 to the −18-volt supply or to the +6-volt supply respectively. The effect of the offset potential is to cause the blanking level at the output of the amplifier to differ slightly from the reference potential.

Unit 3

This unit contains three output stages of the amplifier; the complete amplifier includes four of these units and all the twelve output stages are paralleled. The unit requires a supply at −13·0 volts. The index-peg-position numbers of the chassis are 9 and 16.

The circuit diagram of the unit is given in Fig. 4. Each stage comprises a common-emitter amplifier

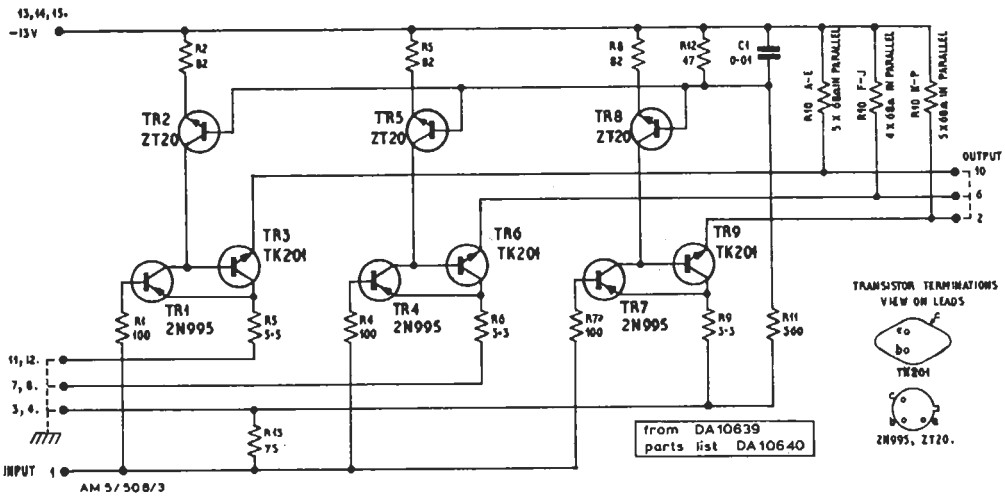

Fig. 4 Circuit of Unit 3 in the AM5/508

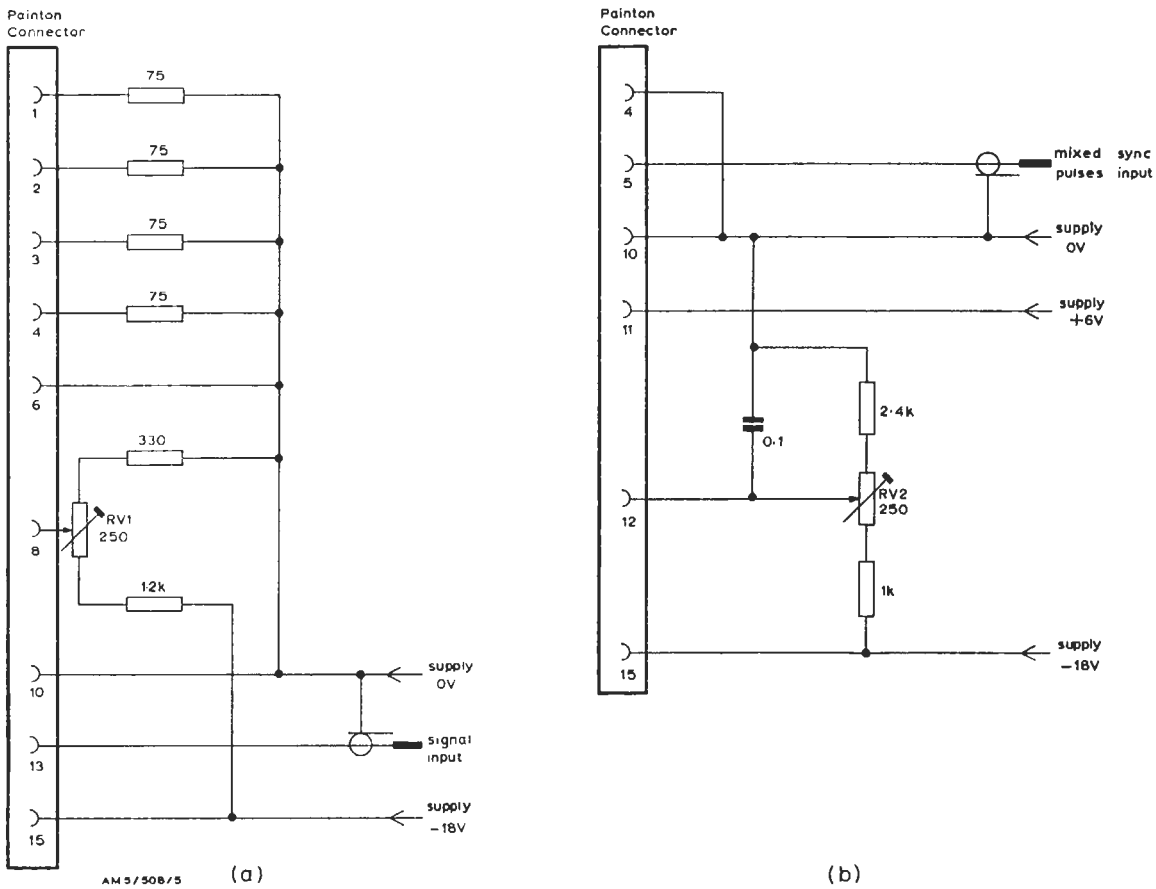

Fig. 5 Test Circuits for the AM5/508

TR1, TR4, TR7 with a constant-current load TR2, TR5, TR8 directly coupled to an emitter-follower TR3, TR6, TR9. R3, R6, R9 provide voltage negative feedback which gives the stages a high output impedance. R10 completes the emitter circuits of TR3, TR6, TR9; to minimise the inductance of this resistor, it is made up of three groups of paralleled resistors.

Maintenance

Apparatus Required

Avometer, Model 8
Cathode-ray oscilloscope
Line-sawtooth Generator GE4/506A
Test circuits as shown in Fig. 5
Feed of mixed-synchronising pulses
Sources of 200 mA d.c. at −18 volts and 100 mA d.c. at +6 volts (both stabilised)

Test Procedure, Unit 1

1. Connect the 18-volt supply to test circuit (a) and adjust RV1 to obtain −4·5 V on tag 8 of the connector with respect to tag 10.
2. Plug the unit to the test circuit and measure the total supply current, which should be 160 mA ±30 mA.
3. Apply a 625-line video signal of sawtooth waveform and 1 V p-p amplitude to the input connector of the test circuit.
4. Adjust the oscilloscope to respond to the d.c. components of applied signals, and check the output signals at tags 1, 2, 3 and 4 of the connector. These should be video signals of sawtooth waveform and 1·4 V p-p amplitude, inverted in polarity with respect to the input signal, and with a blanking level of −1·25 V.

Test Procedure, Unit 2

1. Connect the supplies and mixed-synchronising pulses to test circuit (b) and adjust RV2 to obtain −12·5 V at tag 12 of the connector with respect to tag 10.
2. Plug the unit to the test circuit and measure the supply currents, which should be 80—90 mA from the 18-volt supply and 70—80 mA from the 6-volt supply.
3. Adjust R13 in the unit to obtain −13 V at the emitter of TR7 with respect to chassis.
4. Adjust RV2 throughout its range and check that the potential at tag 8 of the connector varies between −8 V and +5·5 V with respect to chassis.

Test Procedure, Unit 2A

1. Connect the supplies and mixed-synchronising pulses to test circuit (b), and adjust RV2 to obtain −12·5 V at tag 12 of the connector with respect to tag 10.
2. Plug the unit to the test circuit and measure the supply currents, which should be 48—50 mA from the 18-volt supply, and 25—28 mA from the 6-volt supply.
3. Check that 18-volt, positive-going pulses are present at the collector of TR9.
4. Adjust R5 in the unit to obtain −12 V at the emitter of TR3 with respect to chassis.
5. Adjust RV2 throughout its range and check that the potential at tag 8 of the connector varies between approximately −12·5 V and +1 V with respect to chassis.

The setting of R8 in the unit does not significantly affect the above tests; adjustment of R8 must be carried out when the unit is installed in the parent equipment.

Test Procedure, Unit 3

Measure the resistances between pin 13 and pins 3, 7 and 11 of the unit connector, applying the test-meter leads in both senses for each measurement so as to make the measured pin first positive and then negative with respect to pin 13. (N.B. the black lead of the test meter is of positive polarity when the instrument is set to measure resistance.) The results should be as shown in Table 1.

TABLE 1

Measured between	*Pin 13 +ve*	*Pin 13 −ve*
Pin 13—pin 3	400—420 ohms	400—420 ohms
Pin 13—pin 7	4—7 kilohms	1—2 kilohms
Pin 13—pin 11	4—7 kilohms	1—2 kilohms

References

1. Input Amplifying Panel PA1/517
2. Line-store Standards Converter CO6/501A
3. Designs Department Technical Memorandum No. 7.82(64)
4. Designs Department Specification No. 7.11(64)

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