TONE ENCODER CD2/501

Introduction

The CD2/501 accepts PAL subcarrier, four d.c. error control-signals related to sync-pulse timing[1] and colour-burst phase[2] in the Natlock System[3], and a d.c. test signal. It provides the seven Natlock tone error-signals and an eighth test tone, all determined by the combination of d.c. signal inputs.

The Tone Encoder requires an external d.c. supply of −12 V, 280 mA and is constructed on a single printed-wiring board accommodated in a CH1/12A chassis using index pegs 8 and 39.

General Specification

Signal Inputs

PAL subcarrier	1 V p-p (minimum level 0·5 V)
Error control signals	(see Table 1)
a) A', R', F' (binary logic)	0 V and −6 V (nominal)
b) C' (ternary logic)	0 V, −3 V and −6 V (nominal)
Test signal, X (binary logic)	0 V and −6 V (nominal)

Input Impedances

PAL subcarrier	about 1 kilohm
D.C. signals	high

Signal Output	Natlock tone error signal
Level (w.r.t. 1 mW into 600 ohms)	0 dB
Impedance	600 ohms, centre-tapped to earth
Power Input	−12 V, 280 mA, d.c.
Ambient Temperature Range	0°C to 45°C
Weight	0·45 kg

TABLE 1

Error Control Signal Tolerances

Nominal Voltage	*Voltage Tolerances*	
	binary logic	*ternary logic*
0	more +ve than −1·5	more +ve than −1·5
−3	–	from −2·2 to −3·25
−6	more −ve than −4·5	more −ve than −4·5

General Description

The block diagram of the CD2/501 is given in Fig. 1. The unit uses PAL subcarrier to feed a divider chain the division ratio of which can have eight values selected by changing the feedback connections with

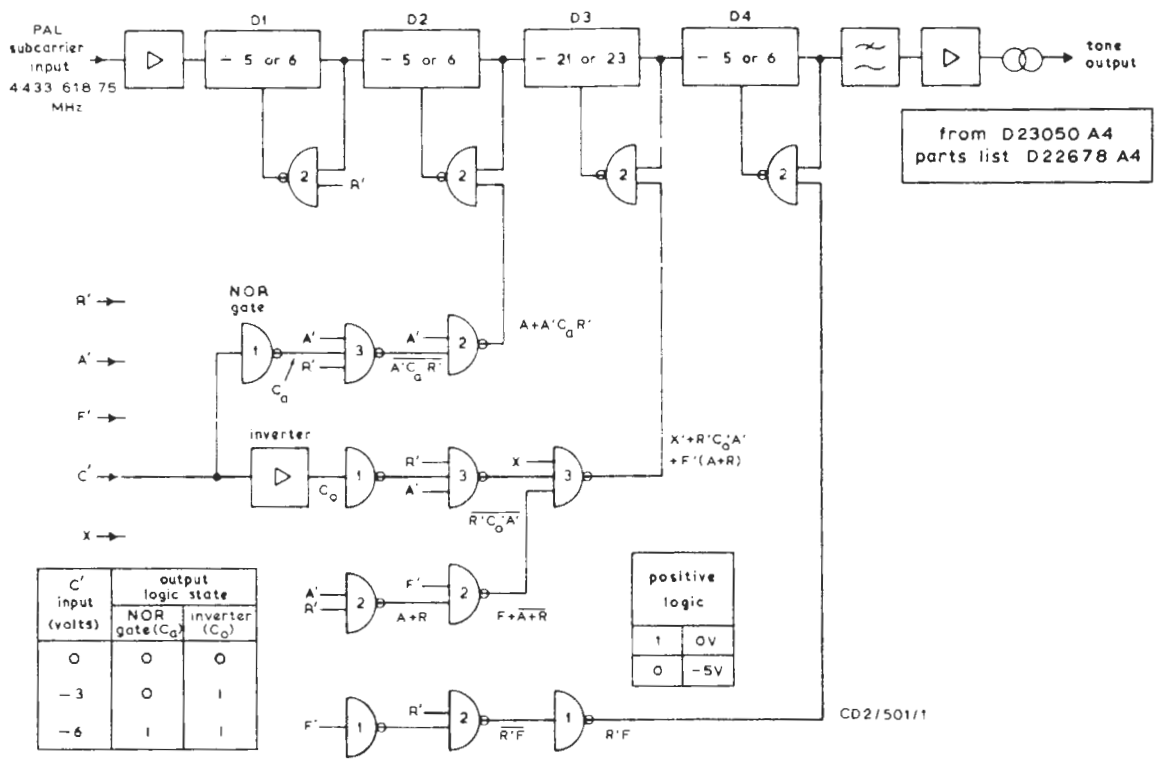

Fig. 1. Block Diagram of the Tone Encoder CD2/501

logic gates. The gates are controlled by the d.c. error and test signal inputs. The output from the divider chain is a single tone at one of eight discrete frequencies. The error control functions corresponding to the tone frequencies are given in Table 2.

890 Hz to 1700 Hz in mutual 21:23 geometric progression.

Divider Operation

Two types of divider, each with two division ratios

TABLE 2

Input Voltage/Output Frequency for Error Control Functions

Error Control Function	*Input Voltages*					*Check Voltages*				*Divider Ratios*				*Output Frequency (Hz)*
	R'	*A'*	*F'*	*C'*	*X*	*IC9a pin 13*	*IC9b pin 2*	*IC9c pin 5*	*IC10d pin 10*	*Dl*	*D2*	*D3*	*D4*	
fast retard	–6	0	–6	*	0	–6	–5	–5	–5	6	6	23	6	892
retard	–6	0	0	*	0	–6	–5	0	–5	6	6	21	6	997
colour retard	0	0	0	–3	0	0	–5	–5	–5	5	6	23	6	1071
normal	0	0	0	0	0	0	–5	0	–5	5	6	21	6	1173
colour advance	0	0	0	–6	0	0	0	–5	–5	5	5	23	6	1285
advance	0	–6	0	*	0	0	0	0	–5	5	5	21	6	1407
fast advance	0	–6	–6	*	0	0	0	–5	0	5	5	23	5	1542
test	0	–6	–6	*	–6	0	0	0	0	5	5	21	5	1689

Note: Voltages indicated * are immaterial; R' and A' take precedence.

Tone at 0 dB from the unit output is higher in level than is usually acceptable for Post Office lines and the output transformer secondary is tapped to earth only to provide earth-loop information for the local tone decoder[4]. The output tone must therefore be attenuated and passed through a correctly-balanced repeating coil before it is connected to a Post Office line.

System Description

Coder Design Considerations

Error information is coded by frequency-shift keying of a single tone. Seven frequencies are required as error tones; an eighth tone is made available as a test signal.

Design of the associated decoders[4,5] is simplified if the tones are in geometric ratio. Conveniently, dividing PAL subcarrier successively by the ratios given in Table 2 provides the output frequencies in the range

are used in the coder. In the first type, in positions D1, D2 and D4 (see Fig. 1) the basic divide-by-six mode is changed to divide-by-five when feedback is applied. The JK bistables used in the divider chain are master-slave[6] types which have the truth table given in Table 3. Information is read in by the J and K inputs at the positive-going edge of the clock pulse and is transferred to the outputs at the negative-going edge of the clock pulse.

The block diagram of the divide-by-five or divide-by-six divider is shown in Fig. 2. Corresponding waveforms in Fig. 3 are derived from the truth table and from the initial condition that all $\bar{Q}$ outputs are at level 1 for one clock pulse period in the division cycle. The divider is a synchronous divide-by-three followed by a bistable which provides feedback to the first stage when divide-by-five is required.

The second type of divider in position D3 is a ripple-through counter[6] with a division ratio of 23 which is changed to 21 when feedback is applied to the second stage. An intermediate ratio of divide-by-22 can be obtained by removing *Strap C*. A tone at 1026 Hz is obtained when input voltages corresponding to *Colour Retard* are selected. This tone is used solely for decoder[4,5] alignment and is not part of the error control system.

Feedback Gating

The feedback gate inputs required for each divider to operate at its lower division ratio are included in Table 2. Derivation of these signals for dividers 1 and 4 can be followed on the block diagram (Fig. 1). The colour error signal required for dividers 2 and 3 must be translated from three states to two; specifically, the signals indicating *Colour Advance* and *Colour* are required.

TABLE 3

Truth Table for JK Bistable

Input Conditions at Leading Edge of Clock Pulse		*Output at Trailing Edge of Clock Pulse*
J	*K*	Q_{n+1}
0	0	Q_n
1	0	1
0	1	0
1	1	Q_n

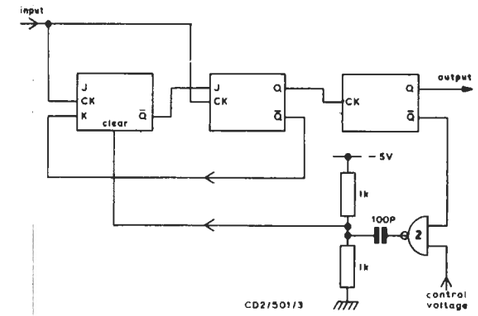

Fig. 2. Block Diagram of the Divide-by-5 or Divide-by-6 Counter

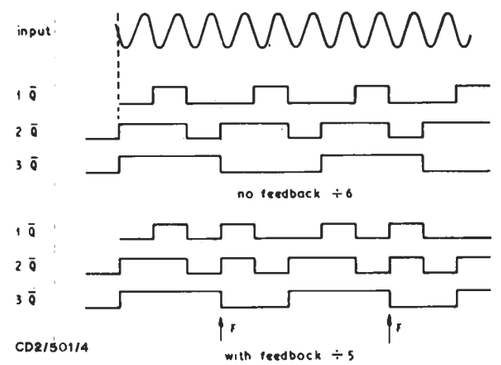

Fig. 3. Waveforms in Divider 1

The colour-error input is applied to both a NOR gate and an inverter (shown on the circuit diagram in Fig. 4). The NOR gate threshold is at −3·6 volts; thus colour error inputs at 0 volts and −3 volts will be treated as level 1 and the −6 volt signal (Colour Advance) as .0. The gate output is therefore 1 for *Colour Advance* and 0 for *Colour Retard* and *Normal*. This output signal, designated C_a in Fig. 1, is then gated with A' and R' signals so that they take precedence.

The inverter stage has a threshold more positive than −3 volts. Thus the output will be logic 1 whenever *Colour Advance* or *Colour Retard* information is present at the input. This binary output signal is here represented by C_O. The following gate inverts this to give C'_O for gating with A' and R' signals.

given under General Description.

Maintenance and Alignment

Routine maintenance is not necessary. The coder can be tested as part of the parent unit[7,8], or with reference to the information given in Table 2.

Modifications for Use with a Moving Source

Some units CD2/501 bear the label *Modified for Moving Source* and a three-position switch *Static/Normal/Rove*. In this case provision has been made to switch error signals to the tone coder in a three-stop sequence when locking a mobile source. Details of the circuit changes are shown in Fig. 4.

Details of modification and operation are given in Designs Department Technical Memorandum 10.31(70).

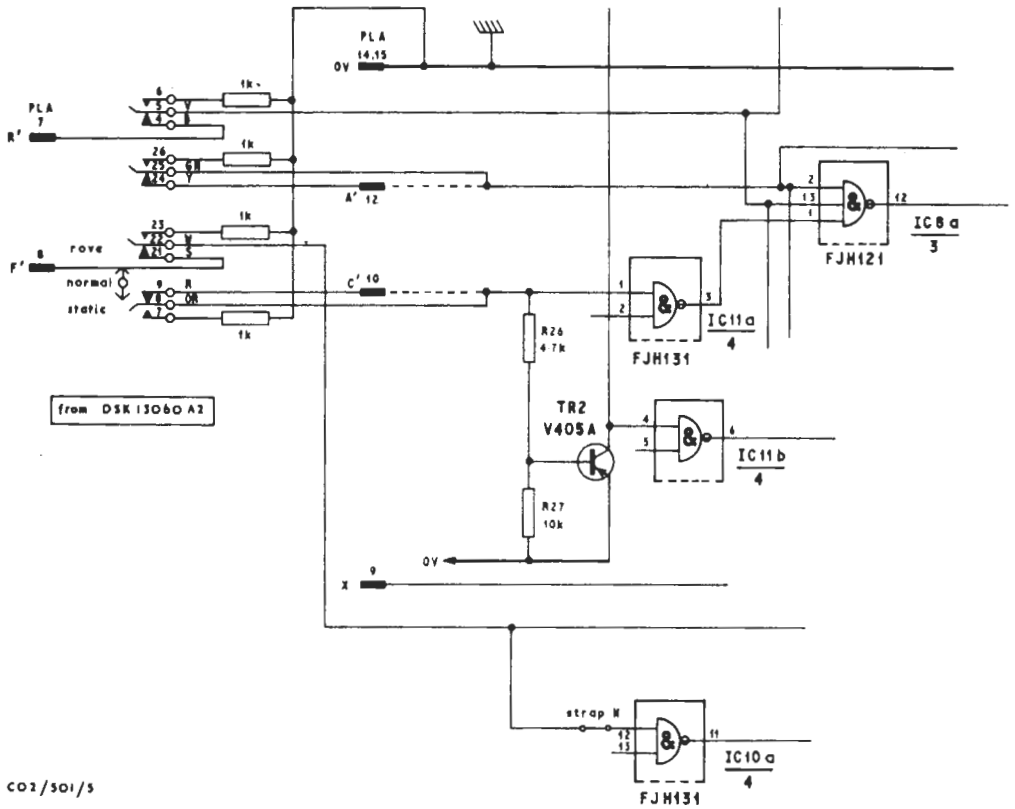

Fig. 4. Circuit of the switch, added to the CD2/501 when used with Mobile Source

Test Facility

The eighth tone is generated to facilitate decoder[5] line-up. An additional input X, when at −6 volts, will cause divider 3 to divide by 21. When inputs for *Fast Advance* are also applied the output frequency is 1689 Hz.

Output Stages

The filter stage including TR3 gives a low-pass response with a basic slope of 18 dB/octave. R20 and C11 further increase this slope.

The output amplifier TR4,5 is preset by R31 to deliver a 0-dB 600-ohm output which must not be connected directly to Post Office lines for reasons

References

1. Comparator Unit UN17/506
2. Colour Subcarrier Phase Comparators EP5/505,6 series
3. *Picture Source Synchronising*; Instruction P.1
4. Tone Decoder and Pulse Comparator Unit UN17/518
5. Tone Decoder CD3/501
6. *Switching Circuits and Logic*; Instruction GP.1
7. Error Signal Generators (PAL) GE1L/532, GE1M/540, GE1M/568
8. Natlock Tone Test Equipment EP14L/503.

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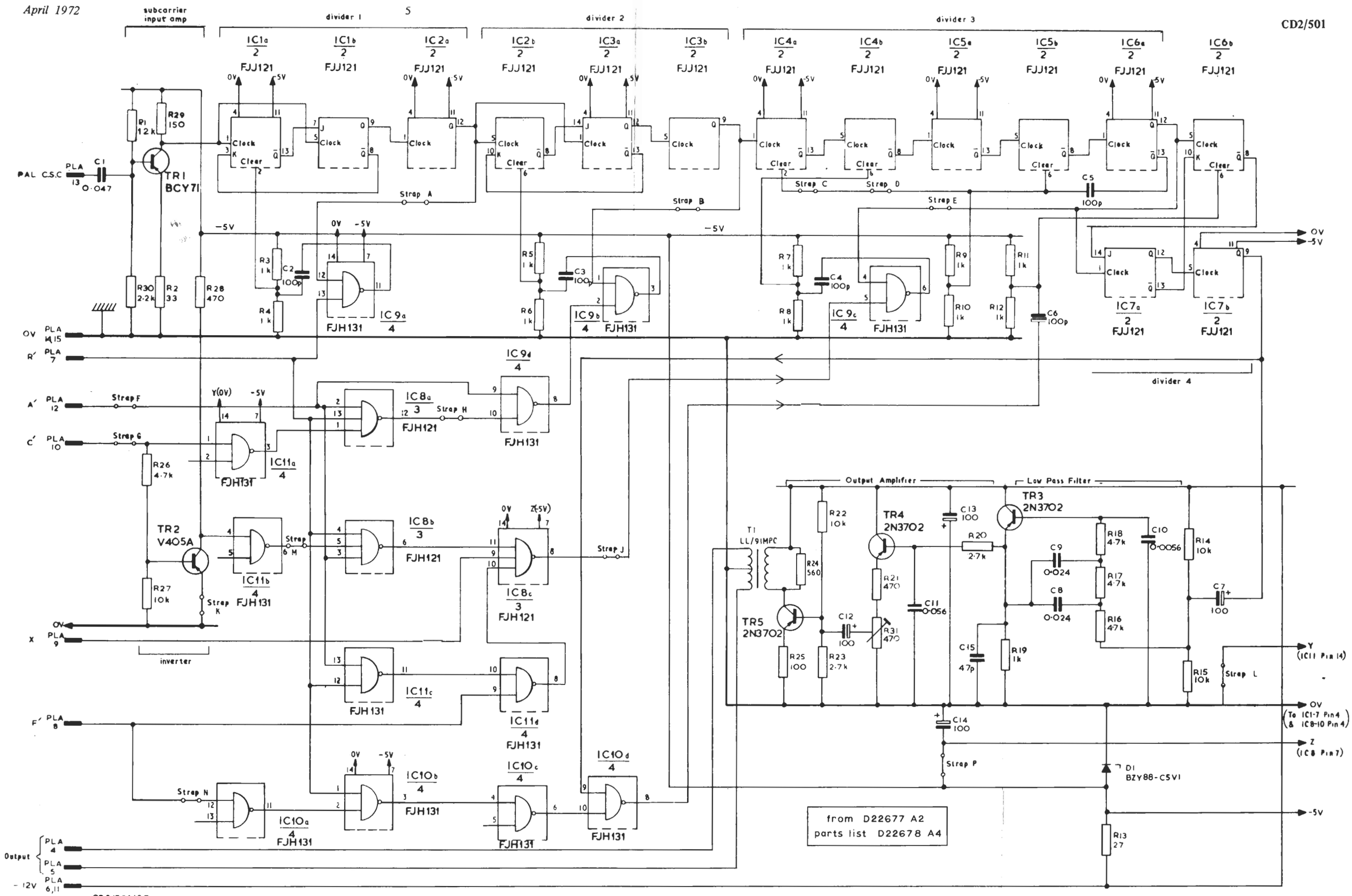

POSTIVE LOGIC CONVENTION

1	OV
0	-5V

TRANSISTOR TERMINATIONS

VIEW ON LEADS

V405A

2N3702

VIEW ON LEADS

FJJ121
FJH121
FJH131

Strap C — Denotes Wire Straps on Printed Board