TONE DECODER CD3/501

Introduction

The CD3/501 accepts the Natlock[1] tone error signal which it equalises and decodes to provide d.c. error control signals corresponding to the tone frequency originated by the associated tone coder[2]. The d.c. signals control sync pulse timing in the dependent drive unit[3] and colour subcarrier phase in the dependent digital phase shift equipment[4].

The decoder front panel carries a meter which indicates equalised tone level; a *Gain* switch; three equaliser controls *Set Gain 1542, Set 893* and *Set 1173;* a *Monitor Input* audio jack which bridges the input line, and five lamps indicating presence of the four decoded error control signals, *F, A, R, C* and *Alarm.* The *Alarm* lamp lights and relay changeover contacts are operated if any of the three conditions is met:

equalised tone level too low (below −6 dB)
equalised tone level too high (above 0 dB)
continuous error control signal decoded

The CD3/501 requires an external d.c. supply at −12V, 400 mA. This is normally supplied by the associated drive unit[3].

The decoder is constructed on three printed wiring boards accommodated in a CH1/38 (B-size) chassis, using a 15-way connector in the central position. Index peg positions used are 8 and 40, associated with the left connector position.

General Specification

Signal Input	Natlock tone error signal
Amplitude (w.r.t. 1 mW into 600 ohms)	from 0 dB to −36 dB
Impedance	600 ohms floating
Equalisation available (w.r.t. 1542 Hz)	14-dB attenuation at 892 Hz and 1173 Hz
Error Control Signal Outputs (see also Tables 1 and 2)	
Sync pulse timing	*A'*, *R'* and *F'* (nominal levels 0V and −6V)
Colour subcarrier phasing (slavelock)	*C'* (nominal levels 0, −3 and −6V)
Colour subcarrier phasing (genlock)	*genlock C'* (nominal levels 0, −6 and −3V)
Alarm	relay changeover contacts operated
Power Input	−12V at 400 mA, d.c.
Ambient Temperature Range	0°C to 45°C
Weight	1·25 kg

TABLE 1

Input Tone Frequency/Error Control Signal Outputs for Control Functions

Natlock error tone frequency (Hz)	*control function*	*Q outputs of bistables (logic levels)*				*error control signal outputs (volts)*				
		f	*a*	*r*	*c*	*F'*	*A'*	*R'*	*C'*	*genlock C'*
892	fast retard	1	0	1	0	−6	0	−6	0	0
977	retard	0	0	1	0	0	0	−6	0	0
1071	colour retard	0	0	1	1	0	0	0	−3	−6
1173	normal	0	0	0	1	0	0	0	0	0
1285	colour advance	0	1	0	1	0	0	0	−6	−3
1407	advance	0	1	0	0	0	−6	0	0	0
1542	fast advance	1	1	0	0	−6	−6	0	0	0
1689	test	1	0	0	0	−6	0	0	0	0

TABLE 2

Error Control Signal Tolerances

nominal voltage	*actual voltage tolerances*	
	binary logic	*ternary logic*
0	more +ve than −1·5	more +ve than −1·5
−3	-	from −2·5 to −3·25
−6	more −ve than −4·5	more −ve than −4·5

Operational Alignment

1. Set *Gain* switch to *Low* and the three equaliser controls fully clockwise.
2. Request *1542* Hz from the distant Tone Encoder.
   Adjust *Set Gain 1542* for a meter reading midway between the red sectors. If necessary select *High* gain.
3. Request *893* Hz from the distant Tone Encoder and adjust *Set 893* for a similar meter reading.
4. Request *1173* Hz and adjust *Set 1173* similarly.
5. Request *1542* Hz again and check Step 2. If adjustment of *Set Gain 1542* is required, repeat Steps 3 and 4.
6. Request all frequencies from *893* to *1542* Hz and if necessary trim the settings of *Set 893* and *Set 1173* for the best approach to level response and *Set Gain 1542* so that the meter reads on the centre part of the scale for all frequencies.
7. Check lamp indication for decoding appropriate to sending frequency (continuous tone). (See Table 3.)

Table 3

Lamp Indications

Frequency (Hz)	*lamps alight (continuous tone)*				
	Alarm	*F*	*A*	*R*	*C*
892	1	1	-	1	-
977	1	-	-	1	-
1071	1	-	-	-	1
1173	-	-	-	-	-
1285	1	-	-	-	1
1407	1	-	1	-	-
1542	1	1	1	-	-
1689	1	1	-	-	-

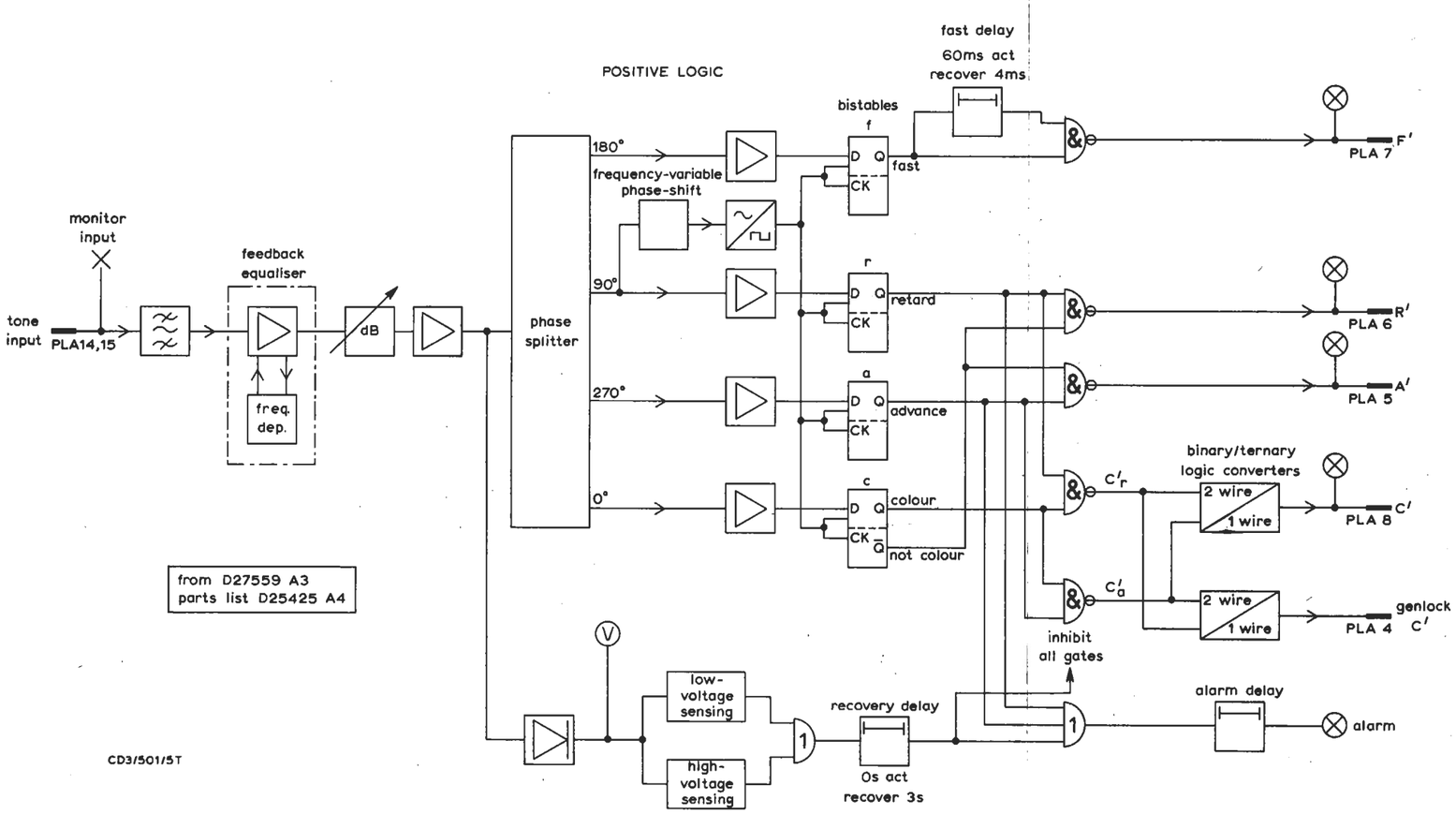


Fig. 1. Block Diagram of the Tone Decoder CD3/501

General Description

A block diagram of the CD3/501 is given in Fig. 1. The decoder performs three functions:

a) the Natlock tone error signal is filtered to remove out-of-band signals, equalised and amplified to the correct level for decoding
b) protection circuits inhibit decoding when the equalised tone level is too high or too low; an alarm circuit indicates this condition
c) tone at the correct level is decoded to provide error control signals corresponding to the tone frequency.

(a) Tone Processing

A constant-k band-pass filter, misterminated to reduce droop at band edges operates over the range 892 Hz to 1689 Hz. Filtered tone is passed to a feedback equaliser designed to correct for lines with responses falling more or less rapidly with frequency. The equalised output is passed to a switched-gain amplifier.

b) Protection and Alarm Circuits

Two outputs are taken from the switched-gain amplifier. One feeds the decoding circuits and the second is examined by under-voltage and over-voltage protection circuits. These protection circuits must be satisfied for decoding to take place; if they are not, the error control signal outputs are held at 0V (corresponding to the *normal* tone input frequency) until the input tone amplitude returns to the working range.

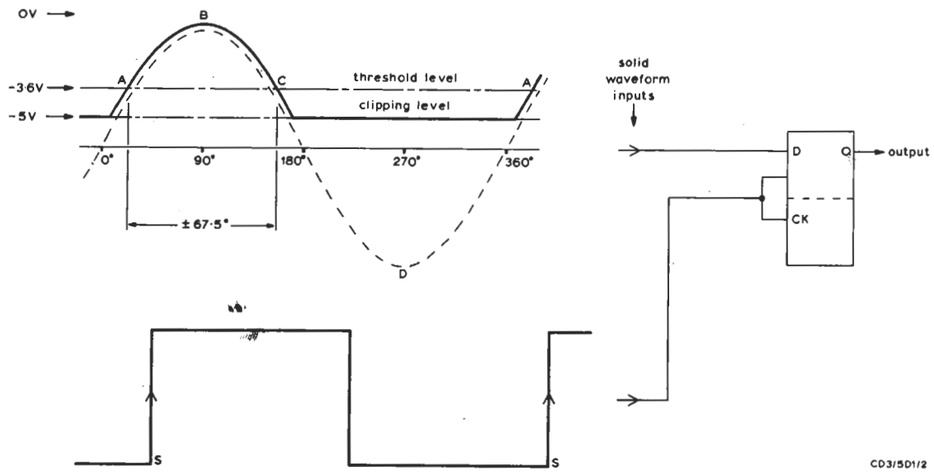
An alarm circuit is operated when the protection circuits are not satisfied or if a continuous timing or phasing error control signal is decoded (resulting from a continuous tone input). When the input signal returns to within the working range there is a recovery delay of about three seconds before decoded error signals are passed to the output.

Further protection operates in the *Fast* decoded output: a *Fast* signal must be decoded for about 60 ms before it is transferred to the unit output. This precaution gives increased immunity from erroneously generated *Fast* error signals which could have catastrophic effect on the system.

c) Decoding

Equalised tone feeds a phase-splitter network whose four outputs have relative phases of 0°, 90°, 180° and 270° over the whole tone error signal frequency range. These outputs feed the D inputs of four D-type bistables[5]. The 90° output also feeds a network whose phase shift is a function of frequency and is an integral multiple of 45° for each tone error signal frequency. The output of the frequency-variable phase-shift network feeds a Schmitt trigger circuit which generates pulses to supply the *Clock* (CK) inputs of the four bistables. Thus the *Clock* inputs are delayed in phase relative to the D inputs by an angle proportional to tone frequency.

The D bistable has the property that its Q output assumes the logic value of the D input at the positive edge of the clock pulse and maintains that value until the next clock pulse. This property is used in the CD3/501 to give a Q output of 1 whenever a clock



Bistable Q output is: 1 if S occurs during ABC, i.e. within ±67.5° of B
0 if S occurs during CDA

Fig. 2. Operation of the D-type Bistable

pulse occurs within ±67·5° of the positive-peak voltage of the waveform at the D input. (See Fig. 2.) This method of decoding is level-sensitive because the ±67·5° tolerance is determined by the positions of the threshold-crossing points on the D-input waveform. (The four reference phases are clipped below the threshold level to avoid reverse-biasing the D inputs.)

Each tone error signal frequency can switch one o two bistables to give a 1 output. But, because each bistable responds to a different group of three frequencies, the logically-combined outputs from the four bistables indicate unambiguously a specific frequency. The diagrams in Fig. 3 summarise this information on the decoding technique.

The outputs from the four bistables are inverted in logic gates to generate the error control signals A'. R' and F', C_a' and C_r' in binary logic. The logic gates are also the point at which inhibit signals from the protection circuits are applied.

The colour burst phase error control signal is required in ternary logic form as C' and as its complement, *genlock* C'. Hence two binary-to-ternary logic converters are used.

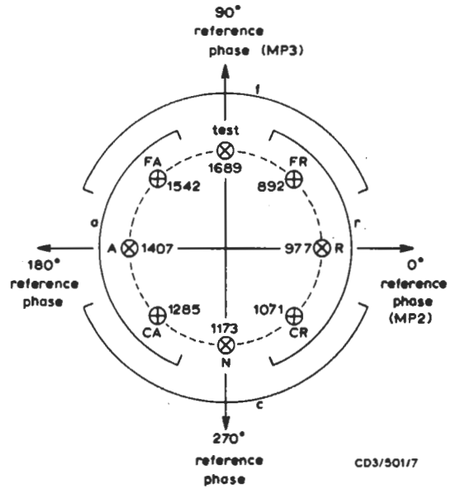


Fig. 3(a). Operation of the Phase Discriminator in the CD3/501

1. The phase of each error signal frequency (from the frequency-variable phase-shifter) is shown on the dotted locus, relative to the four reference phases generated for each input tone.
2. The four arcs, labelled f, a, c, r indicate the phases over which a logic 1 will be generated by the associated bistable.
3. The decoder output control-functions FA, CR, etc., related unambiguously to the error signal frequencies 1542 Hz, 1071 Hz, etc., are shown adjacent to that frequency.

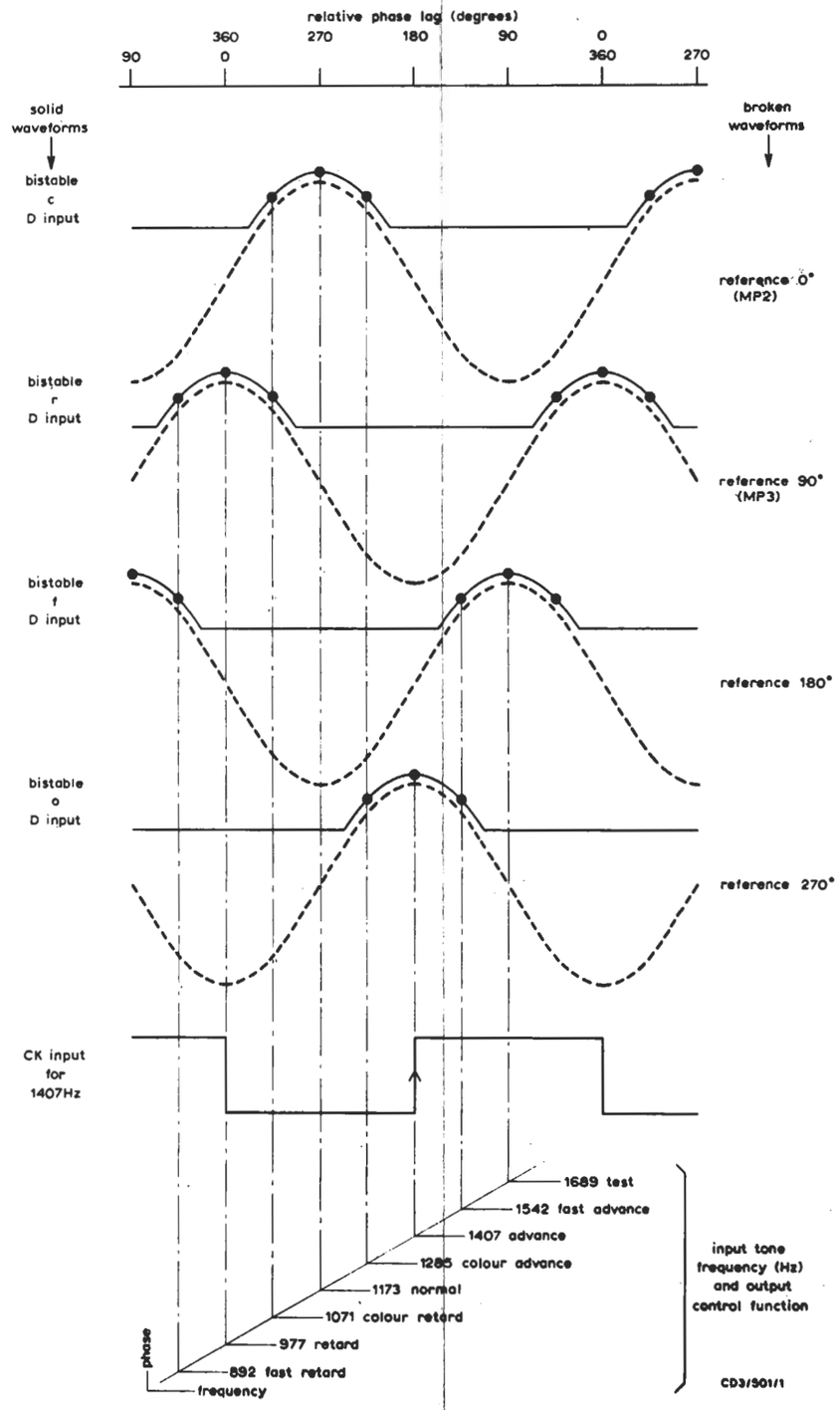


Fig. 3(b). Waveforms in the Phase Discriminator (showning as an example the clock-pulse phase for a 1407-Hz input)

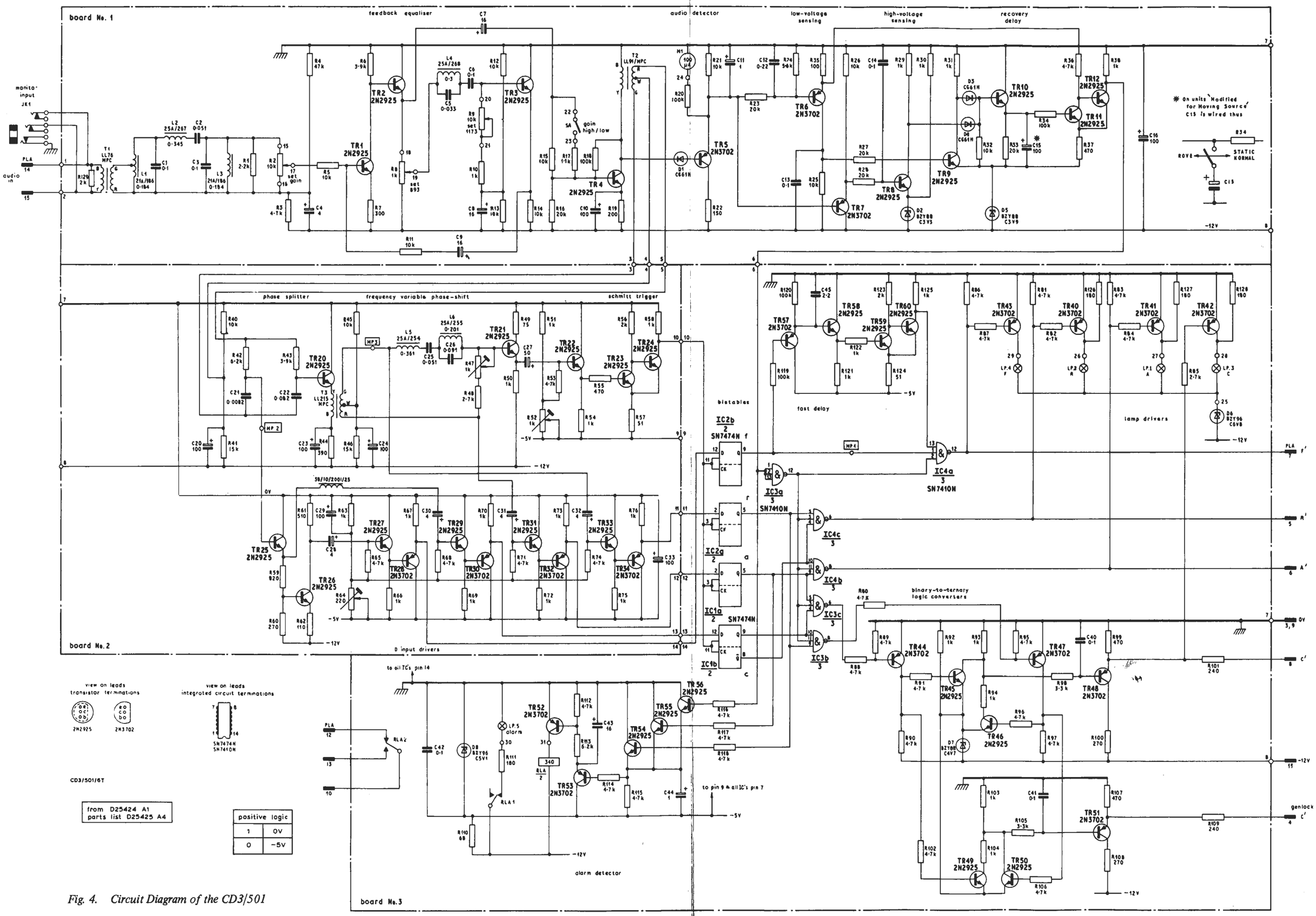


Fig. 4. Circuit Diagram of the CD3/501

Circuit Description

The circuit diagram of the CD3/501 is shown in Fig. 4. The description which follows relates to unit layout on printed wiring boards.

Printed Wiring Board 1

L1, L2, L3, C1, C2 and C3 form the input band-pass filter of 1·5 kilohms nominal impedance. The input is tapped down L1 and this, with R129, gives an input impedance of 600 ohms. The filter response is shown in Fig. 5.

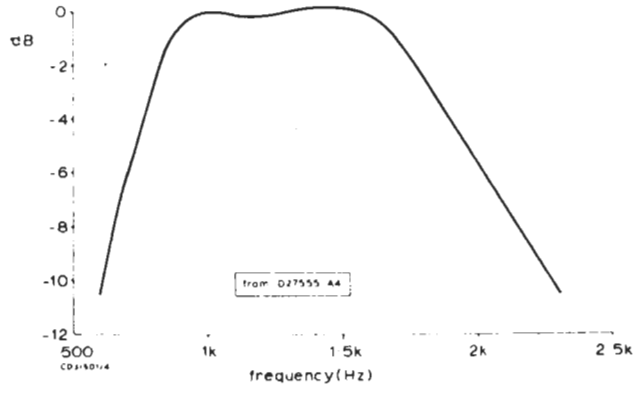


Fig. 5. Response of the Band-pass Filter in the CD3/501

TR1 is the equalising amplifier with emitter followers TR2 and TR3 isolating the frequency-dependent section. The feedback is zero at about 1542 Hz: L4 and C5 have a high impedance in parallel resonance, and the gain control R2 labelled *Set Gain 1542* is adjusted at this frequency. Maximum feedback, occurring at 892 Hz, is caused by the low impedance of L4 and C6 in series resonance, is adjusted by R8, labelled *Set 893.* R9, labelled *Set 1173,* adjusts the mid-range response at 1173 Hz. The controls are not completely independent. Equaliser responses for three combinations of control settings are shown in Fig. 6.

TR4 is an amplifier with a switched gain control (which operates by changing the effective source resistance) giving an increase in gain of 18 dB in the *High* position. TR4 feeds the phase-splitter network (on Board 2) via T2 and direct from the collector it feeds the detector for the meter and level-sensing circuits.

The detector TR5, of the so-called infinite-impedance type, charges the capacitor C11 and the meter indicates the voltage developed. This same voltage drives the low-voltage and high-voltage sensing detectors TR6, TR9 and TR7, TR8. D1 protects TR5 against base-emitter breakdown.

Under normal condition with specified signal levels the meter reads between about 45 and 75% of full scale and the circuit conditions are as follows. TR6 and TR9 (low-voltage sensing) are conductive with D3 and TR10 cut off. TR7 is conductive but not sufficiently to pull down the base of TR8 to the cut-off point. D4 is therefore cut off. In the Schmitt trigger TR11, TR12 transistor TR11 is cut off and TR12 is conducting. Thus a low-level (−5V) or logic 0 is fed to Board 3 where it drives the alarm detector. The logic 0 is also inverted in IC3a to apply a 1 to the decoder output gates.

Under abnormal or fault conditions, if the detector output from TR5 is low (meter reading less than about 35 to 45% of full scale) TR6 ceases to conduct, TR9 cuts off, D3 conducts and TR10 rapidly charges C15. The rise in potential across C15 operates the Schmitt trigger and TR12 cuts off. A high level (0V) or logic 1 is therefore passed with negligible delay to the alarm detector and inverting gate on Board 3. If the signal becomes too high (meter reading greater than about 75 to 85% of full scale) TR8 cuts off, D4 conducts and again C15 is charged by TR10.

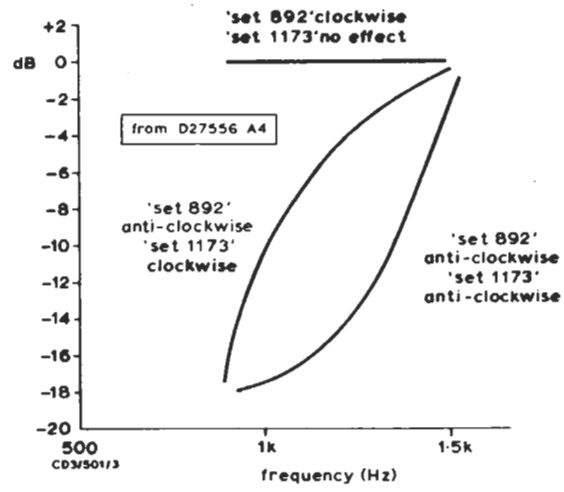


Fig. 6. Response of the Equaliser in the CD3/501

When the signal returns to normal TR10 cuts off, C15 discharges and after about three seconds the Schmitt trigger reverts to normal and a logic 0 is passed to Board 3. This three-second delay increases immunity to intermittent or incorrect input signals.

Printed Wiring Board 2

The centre-tapped transformer T2 in TR4 collector circuit (Board 1) feeds two phase-shifter networks R42, C21 and R43, C22. The first network feeds monitor point MP2 and, via an emitter follower TR25, the inverter stage TR26. The second network feeds T3 via emitter follower TR20. T3 has the ratios 1 : 1+1, chosen to give lagging reference phase outputs:

90° at MP3
270° at T3 (R)

both equal in amplitude to the reference 0° at MP2.

Reference 180° is available at TR26 collector.

The output signal from the frequency-variable phase-shift network L5, L6, C25, C26, R47 and R48 is passed by emitter followers TR21 and TR22 to the Schmitt trigger TR23, TR24. R52 adjusts the bias on TR22 thereby altering the triggering phase of the Schmitt. TR22-24 are fed from the −5V supply to suit the bistable requirements.

Reference phase signals from four identical D-input drivers, TR27, TR28; TR29, TR30; TR31, TR32; TR33, TR34 feed the D inputs of the bistables. The n-p-n stage in each driver enables the d.c. component of the output signal to be adjusted by R64. The p-n-p stage presents the correct driving impedance to the bistable.

Printed Wiring Board 3

This board accommodates the decoder bistables and output gates, two binary-to-ternary logic converters, the alarm detector and four lamp drivers. All integrated circuit gates use NAND logic in which the output is 1 unless all inputs are at level 1.

The four bistables labelled *f, r, a, c* deliver logic level outputs in accordance with the relative phases at their inputs, as explained under *Decoding* in the **General Description.**

When a *Fast* tone frequency is present at the unit input, bistable *f* generates a level 1 output which is passed by two routes to NAND gate IC4a. One route is direct (MP1) and the other via the *fast delay.* TR57 (normally on when a *Fast* tone is not incoming) is turned off by the level 1 from bistable *f.* C45 discharges through R120 until, after about 60 ms, TR58 conducts and the Schmitt trigger TR59, TR60 operates to turn off TR60. The level 1 output, delayed by 60 ms relative to the 0-to-1 input transition, is passed to the second input of NAND gate IC4a. The third input receives a 1 from the inhibit-inverting gate IC3a and the output from IC4a is the *Fast* error control signal F'. A 1-to-0 transition input to the *fast delay* (generated when a *Fast* tone stops) suffers a delay of only 4 ms through the *fast delay.*

Gates IC4c and IC4b deliver the inverted outputs of bistables *r* and *a* as R' and A' error control signals direct to the output, when bistable *c* gives a 1 from its Q output. Gates IC3c and IC3b provide outputs of colour burst phase error control signals C_a' and C_r' in binary-logic form. These are coded into ternary logic in converter TR44-48 to provide the C' error control signal. Intermediate signals are taken to a second converter which provides the *genlock* C' error control signal.

In the logic converters, a colour error signal of −5V from gates IC3c or IC3b bottoms one transistor in each of the pairs TR45, TR46 and TR49, TR50. When the bistables deliver signals corresponding to *Colour Advance* tone to the gates the outputs are −5V ($C_a' = 0$) and 0V ($C_a' = 1$). The −5V input to TR44 turns it on, bottoming TR45 whose collector goes to about −6V. This signal is passed to the C' output on PLA8 via the low-pass filter R98, C40 and emitter follower TR48. TR46 and TR47 are both cut off.

The converse applies to bistable outputs resulting from the *Colour Retard* tone input. Outputs from IC3c and IC3b are 0V ($C_a' = 1$) and −5V ($C_r' = 0$) respectively. The −5V input to TR47 turns it on and bottoms TR46. The −3V potential at the junction of R93 and R94 is passed to the C' output. TR44 and TR45 are cut off.

Signals to the *genlock* C' output on PLA4 are obtained from TR49 and TR50 via emitter follower TR51. When TR44 is turned on by a −5V signal, corresponding to the *Colour Advance* tone input, TR49 is also turned on (and TR50 cut off). The *genlock* C' output voltage is −3V from the junction R103, R104. When TR47 is turned on by a decoded *Colour Retard* tone input, TR50 is also turned on (and TR49 cut off) to feed −6V to the *genlock* C' output.

Gates IC3c and IC3b give 0V outputs for all tone inputs other than *Colour Advance* and *Colour Retard* respectively. When both outputs are at 0V then all transistors in the logic converters are cut off and the output signal from both C' and *genlock* C' is also 0V.

For specified input tone, the alarm detector emitter followers TR54-56 are cut off. However, if either the input tone level is such that the low or high voltage-sensing protection circuits on Board 1 are energised, or if level 1 outputs from bistables *a* or *r* recur more rapidly than is required to maintain synchronism in a Natlock[1] system then the appropriate emitter follower conducts, turning off TR53. C43 discharges, cutting off TR52 and releasing the relay RLA to give *Alarm* indication on LP5.

Four lamps LP1-4 monitor the presence of −5V signals (present only when correction is taking place) on each of the error control signal outputs A', R', C' and F' respectively.

Alignment

EQUIPMENT AND SIGNALS REQUIRED

Double-beam oscilloscope with input adding and subtracting facilities

Natlock Tone Test Equipment, EP14L/503

Feed of PAL subcarrier 1V p–p into 75 ohms.

TEST PROCEDURE

Details are given for the alignment of the frequency-variable phase shifter and the decoding circuits. A complete test schedule is contained in Reference 6.

a) Frequency-variable phase shifter

1. Select *Low Gain* on the CD3/501. Connect the tone output from the EP14L/503 to PLA14, PLA15. Turn *Set 893* and *Set 1173* fully clockwise. Adjust *Set Gain 1542* to give 10V p–p on TR4 collector. Trigger the oscilloscope from *MP2*. Put one probe on *MP2* and the other on *MP3*. Check that *MP3* waveform lags *MP2* by 90° by noting the zero crossings.
2. With both probes on *MP3* adjust the oscilloscope for equal gain on both channels. Move one probe to the base of TR21 and add the inputs. Adjust L6 for minimum signal. (This adjusts the signals to be equal in amplitude with 180° relative phase shift.)
3. Select *1689* Hz on the EP14L/503 and subtract the inputs on the oscilloscope. Adjust L5 for minimum signal. (This adjusts the signals to be equal in amplitude and phase.)
4. Move the probe from *MP3* to *MP2* and add the oscilloscope inputs. Select *1408* Hz on the EP14L/503.
   Adjust R47 for minimum signal.

b) Decoding and Gating Circuits

1. Switch the oscilloscope to alternate trace. Trigger the oscilloscope from pin 10 on Board 2. Attach one probe to pin 10 and the other to the base of TR21.
   Adjust R52 so that the positive-going edge of the squarewave occurs precisely at the positive-going zero-crossing of the sinewave.
2. Remove *Strap C* in the Tone Encoder CD2/501 (part of the EP14L/503). Select *1071* Hz; (this produces an output frequency of 1026 Hz from the CD2/501 which is phase retarded by 22·5° relative to 1071 Hz by the frequency-variable phase-shifter in the CD3/501).
   Adjust *Set Gain 1542* for 10V p–p tone at TR4 collector.
   Adjust R64 so that the voltage on pin 8 of IC1b is about to change from –4·5V to –1·0V. There is some backlash on the adjustment R64 must be adjusted so that the switching is occuring in the correct sense.
   Replace *Strap C* in the CD2/501.

Modifications for Use with a Moving Source

Some units CD3/501 bear the label ***Modified for Moving Source*** and a two-position switch ***Rove/Static, Normal.*** In this case provision has been made to bypass the *recovery delay* associated with output gates inhibit (see page 3) during the *Rove* operation.

Details of the wiring changes are shown only on the circuit diagram in Fig. 4.

Details of modification and operation are given in Designs Department Technical Memorandum 10.31(70).

References

1. *Picture Source Synchronising;* Instruction P.1
2. Tone Encoder, CD2/501
3. Waveform Generator Drive Unit, GE1/520
4. Colour Subcarrier Phase Shifter, EP1L/509
5. Switching and Logic Circuits; Instruction GP.1
6. Designs Department Technical Specification 10.37(69).

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