SYNC PULSE CONVERTER CO4/503

Introduction

The CO4/503 accepts either a composite video signal or mixed sync pulses on the 625-line standard; it produces the following outputs:

(a) 625-line standard 1·5-volt negative-going line-frequency pulses, 3 μs in duration, the leading edges of which occur approximately 0·5 μs after the start of the input line-sync pulses.
(b) 625-line standard 2·0-volt negative-going field-frequency pulses, 120 μs in duration, the leading edges of which occur at the start of the second input broad pulse.
(c) 405-line standard 2·0-volt mixed sync pulses (four outputs).
(d) 405-line standard 2·0-volt mixed blanking pulses.

The levels quoted are for outputs terminated in 75 ohms.

The CO4/503 comprises eleven units constructed on CH1/12A chassis, with index-peg positions given in Table 1, together with an AM4/506A and a PS2/503A mounted in a double panel PN3/23.

TABLE 1

Unit	*Index-peg positions*
1	10 and 14
2	10 and 16
3	10 and 18
4	10 and 20
5	10 and 22
6	10 and 24
7	10 and 26
8	10 and 28
9	10 and 30
10	10 and 11
11	9 and 19

General Description

A simplified block diagram of the CO4/503 is given in Fig. 1. Line and field pulses derived from

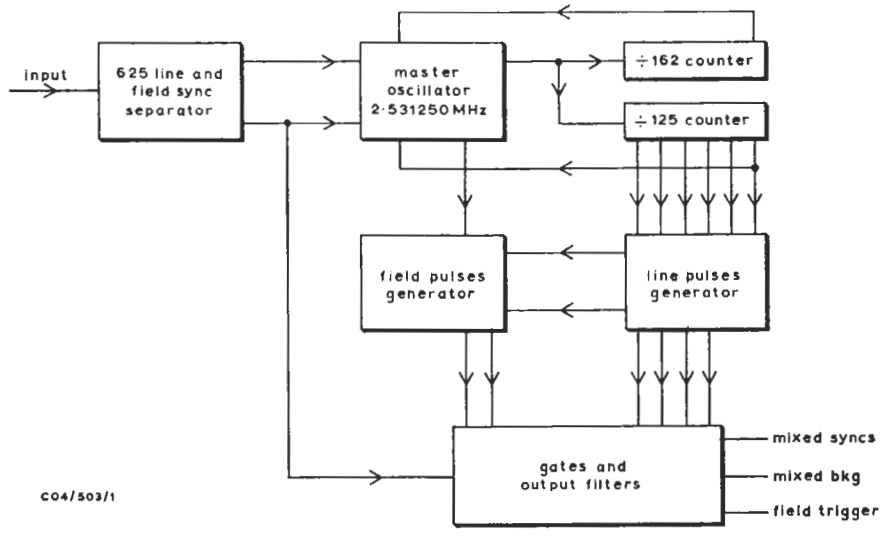


Fig. 1 Simplified Block Diagram of the CO4/503

the 625-line input signal are fed to a master oscillator operating at 2·531250 MHz. This frequency is 162 times 625 line frequency and 125 times 405 twice-line frequency. The output of the oscillator is fed to a divide-by-162 counter and to a divide-by-125 counter. The output of the divide-by-162 counter and the 625 line frequency pulses are compared for phase and the resulting d.c. signal controls the frequency of the master oscillator.

The 625 field frequency pulses and the output of the divide-by-125 counter are used to produce field trigger pulses with a duration in the range approximately 0 μs to 50 μs. If the duration of these pulses is at either end of its range, a small disturbance in the timing of the input signal causes the field trigger pulses to occur in the wrong 405 half-line period thus causing a momentary loss of interlace and perhaps jitter. The field trigger pulses are used to control the phase of the master oscillator which in turn controls the duration of the field trigger pulses in order to minimise jitter of the output waveforms.

Outputs of the divide-by-125 counter and a further divide-by-2 counter are used to produce line-sync-and-front-porch pulses, line blanking pulses and broad pulses.

A self-stopping divide-by-28 counter is switched on by field trigger pulses to count broad pulses for 14 lines. Outputs of this counter are used to gate the field signals into the mixed sync and mixed blanking outputs.

Line sync pulses are produced by gating line-sync-and-front-porch pulses and broad pulses. Thus the broad pulses are the only source for the line-sync timing edges throughout the output mixed sync pulse waveform.

Detailed Description

Fig. 2 is a more detailed block diagram of the CO4/503. The input signal is fed, in unit 1, via a simple sync separator to a 625 line-frequency blocking oscillator and to a field-sync separator circuit. The natural period of the blocking oscillator is sufficient to prevent double-triggering during the field interval. The field sync signal triggers a 1·4-ms monostable multivibrator.

The output of the master oscillator in unit 2 is squared and fed to a divide-by-162 counter in units 3 and 4. It is also fed to a divide-by-125 counter in units 5 and 6. The master oscillator frequency is 2·531250 MHz and the output frequencies of the counters are 625 line frequency and 405 twice-line frequency respectively.

The output pulses of the divide-by-162 counter are used in unit 2 to sample the output of a 625 line frequency sawtooth generator driven from unit 1. The sampled pulses of sawtooth signal are fed via a low-pass filter, which removes the alternating component, to the master oscillator. This d.c. signal controls the frequency of the master oscillator.

The divide-by-125 counter is arranged as three similar divide-by-5 counters. Some waveforms of the second and third divide-by-5 counters, shown in Fig. 3, are fed to unit 7 where they are fed to bistable circuits to produce line-sync-and-front-porch pulses, line blanking pulses and broad pulses.

A field trigger pulse fed to unit 11 triggers a bistable circuit which in turn starts a self-stopping divide-by-28 counter. Waveforms found in this unit are shown in Fig. 4.

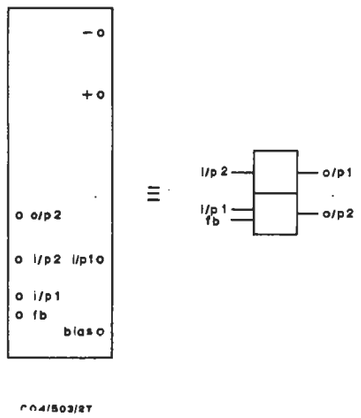
Line-sync-and-front-porch pulses are gated with field sync pulses in unit 8. The resulting waveform is gated with broad pulses to produce mixed sync pulses in such a way that the line sync timing edges are all taken from the broad pulses. This is also shown in Fig. 4.

Line blanking pulses and field blanking pulses are gated together in unit 9 to produce mixed blanking pulses.

625 field-frequency pulses and the 405 twice-line frequency output pulses of the divide-by-125 counter are fed to a bistable circuit in unit 4. This produces field trigger pulses, the duration of which lies in the range approximately 0 μs to 50 μs. If the pulse duration is at either end of this range, small disturbances in the timing of the 625-line input signal can cause the trigger pulse timing to change by a 405 half-line period. This results in a momentary loss of interlace. To overcome this possible fault, two circuits in units 2 and 4 are used to generate pulses if the field trigger pulse is either too short or too long. These pulses are fed to a bistable circuit in unit 2 which changes the natural frequency of the master oscillator. Because the master-oscillator phase discriminator operates at 625 line frequency, rather than at 2·53125 MHz, the phase shift at the lower frequency to correct for a change in the natural frequency of the oscillator is an appreciable portion of 64 μs. This is sufficient to change the duration of the field trigger pulses to the centre of its range.

text continued on page 7
see page 5 for Fig. 3
see page 6 for Fig. 4

notes
1. component modules (bistable circuits UN1/535 and amplifiers UN1/534) in units 3,4,5,6,7 and 11 are numbered from front of unit
2. bistable circuit UN1/535 connections are as shown below (from component side)



CO4/503/ST

Fig. 2 Detailed Block Diagram of the CO4/503

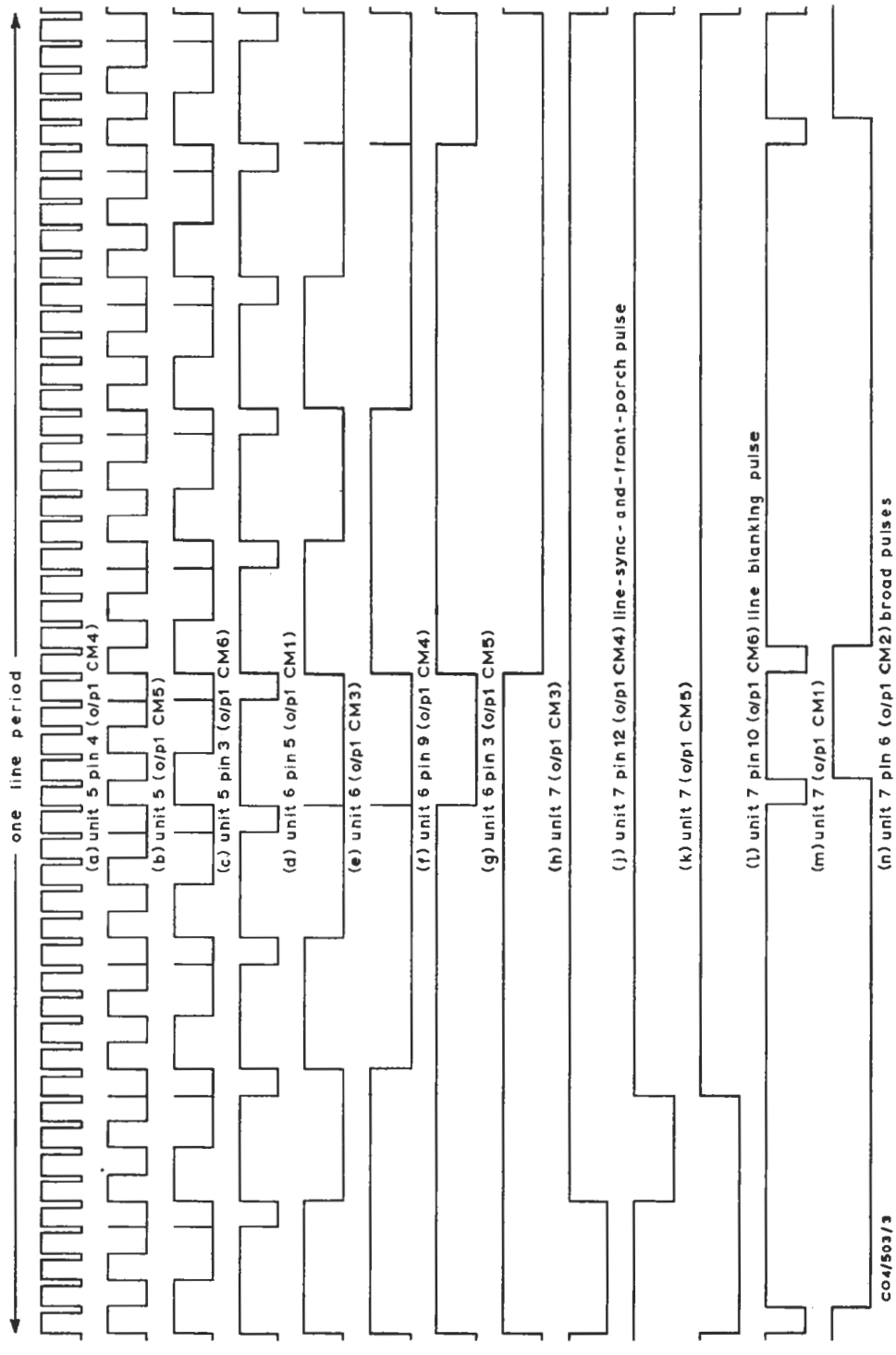


Fig. 3 Generation of Line-frequency and Twice-line-frequency Waveforms

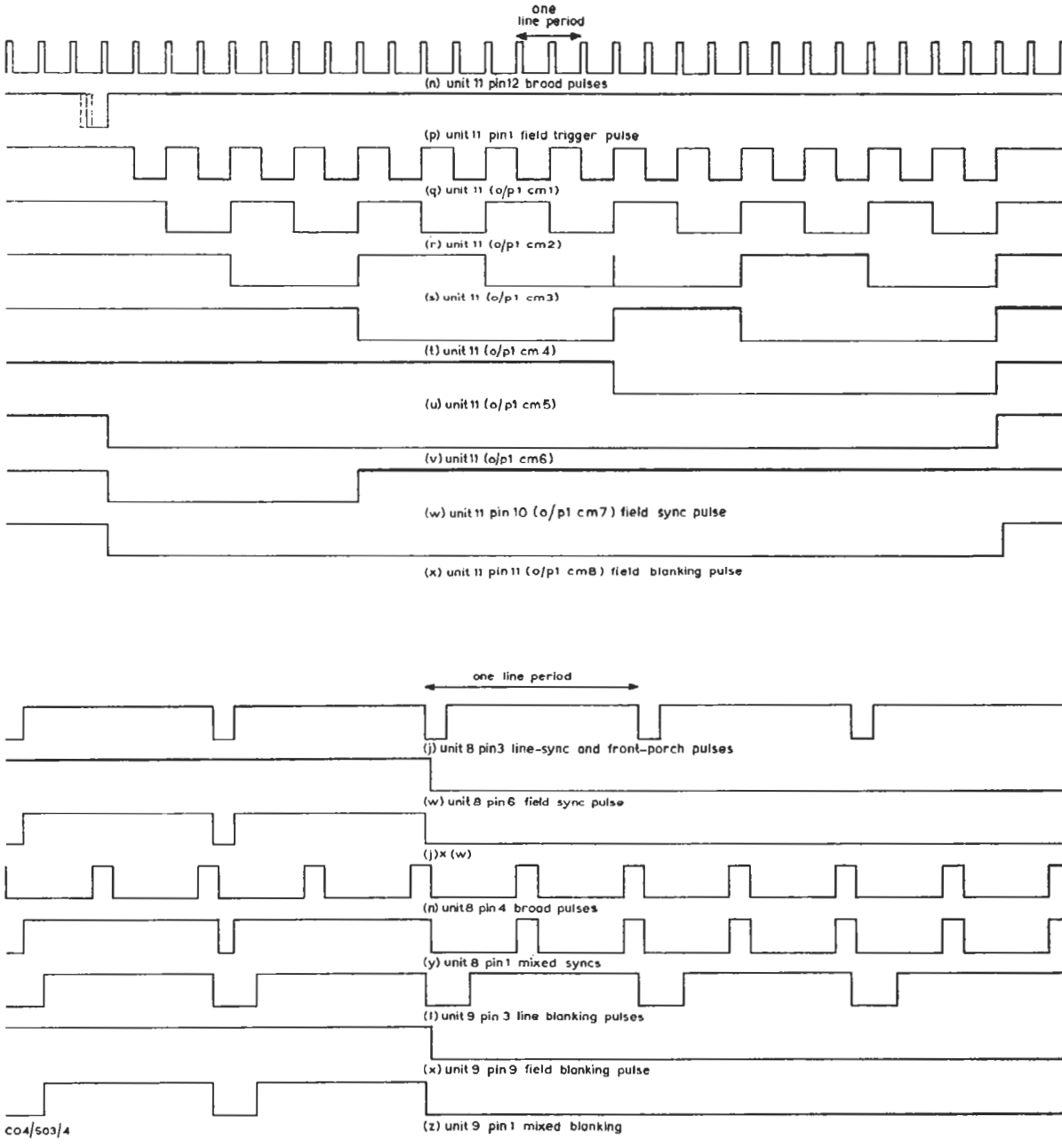


Fig. 4 Generation of Field Waveforms and Gating of Output Waveforms

Circuit Description

Unit 1

The circuit of unit 1 is given in Fig. 5. The input signal is d.c. restored at the base of transistor TR1 via the base-emitter diode junction. Clipping of the positive-going excursion of the input waveform in this transistor produces positive-going sync pulses at the collector. These pulses which have an amplitude of 7 volts p-p are fed to a line-frequency blocking oscillator and to a field-sync separator circuit.

The output waveform of the field-sync separator circuit, shown in Fig. 6, triggers a 1·4 ms monostable multivibrator at the start of the second broad pulse. The output of the multivibrator is a positive-going pulse.

The blocking oscillator circuit of transistor TR3 has a natural period of about 75 μs. This is sufficient to give positive-going output pulses at line frequency without double triggering during the field sync interval.

Unit 2

The circuit of unit 2 is given in Fig. 7. The master oscillator comprises a common-base stage TR3 and an emitter follower TR4 with a series tuned circuit connected between their emitters. The tuned circuit comprises the inductance of L2 and the capacitance of C13 and D3. The capacitance of diode D3 varies with the voltage fed to it from the phase discriminator.

Positive-going pulses fed to the base of transistor TR2 cause it to conduct and discharge capacitor C7. Capacitor C7 charges via resistor R8 to give a sawtooth waveform shown in Fig. 8.

The rectangular waveform fed to pin 11 is differentiated and inverted to produce positive-going pulses at the collector of transistor TR1.

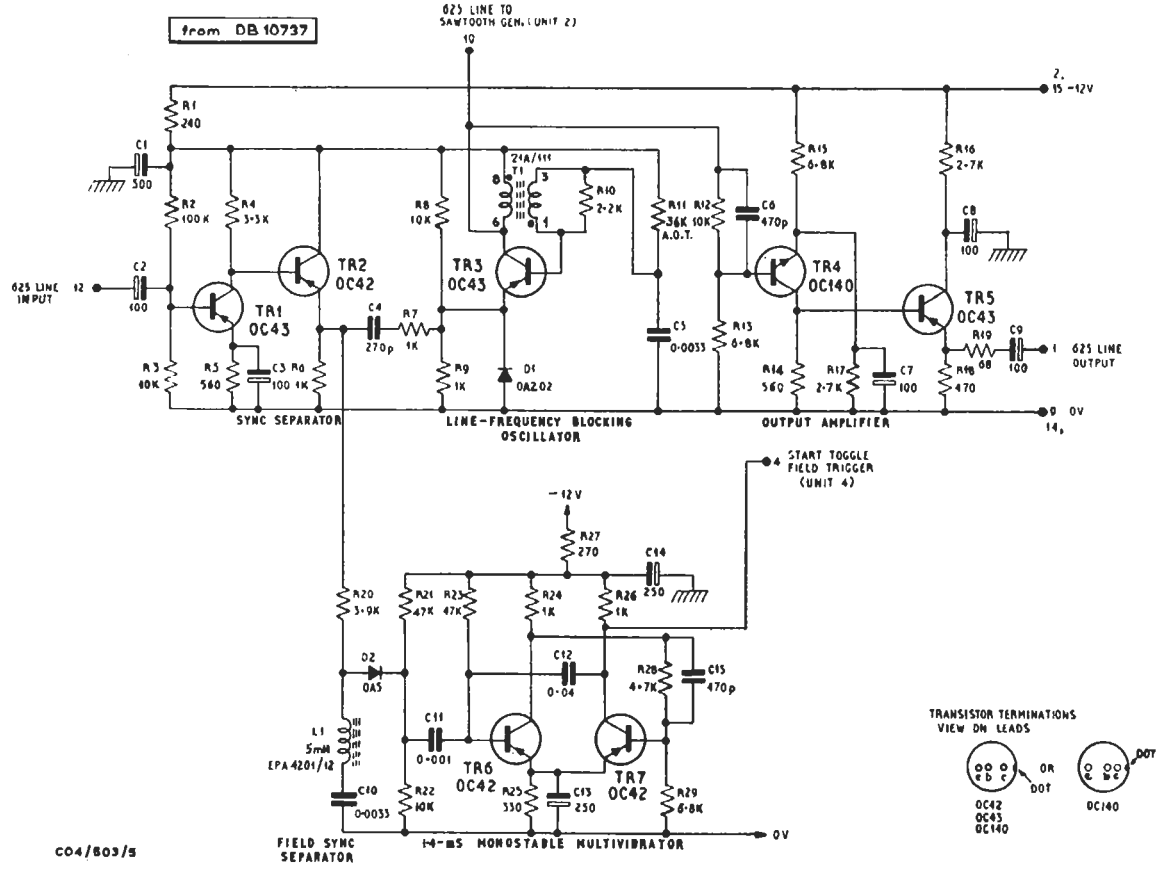


Fig. 5 Circuit of Unit 1

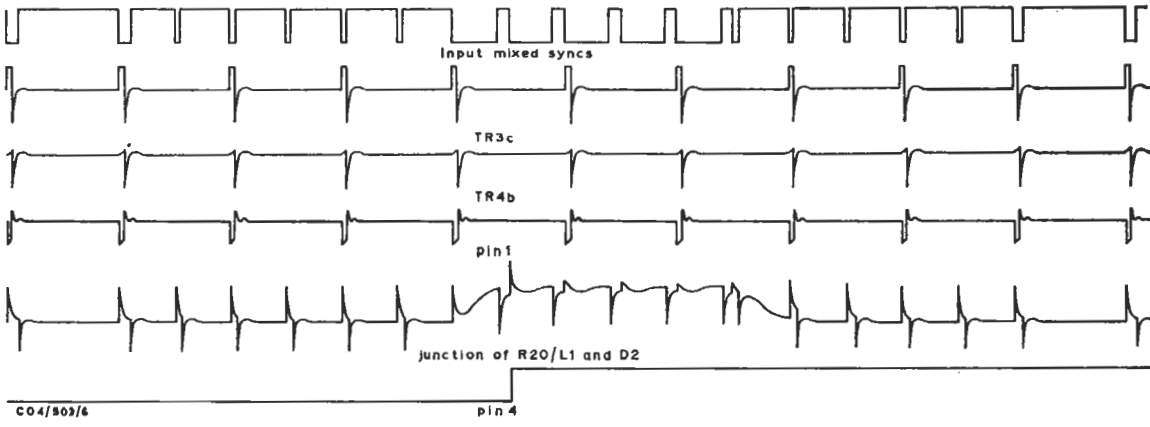


Fig. 6 Waveforms in Unit 1

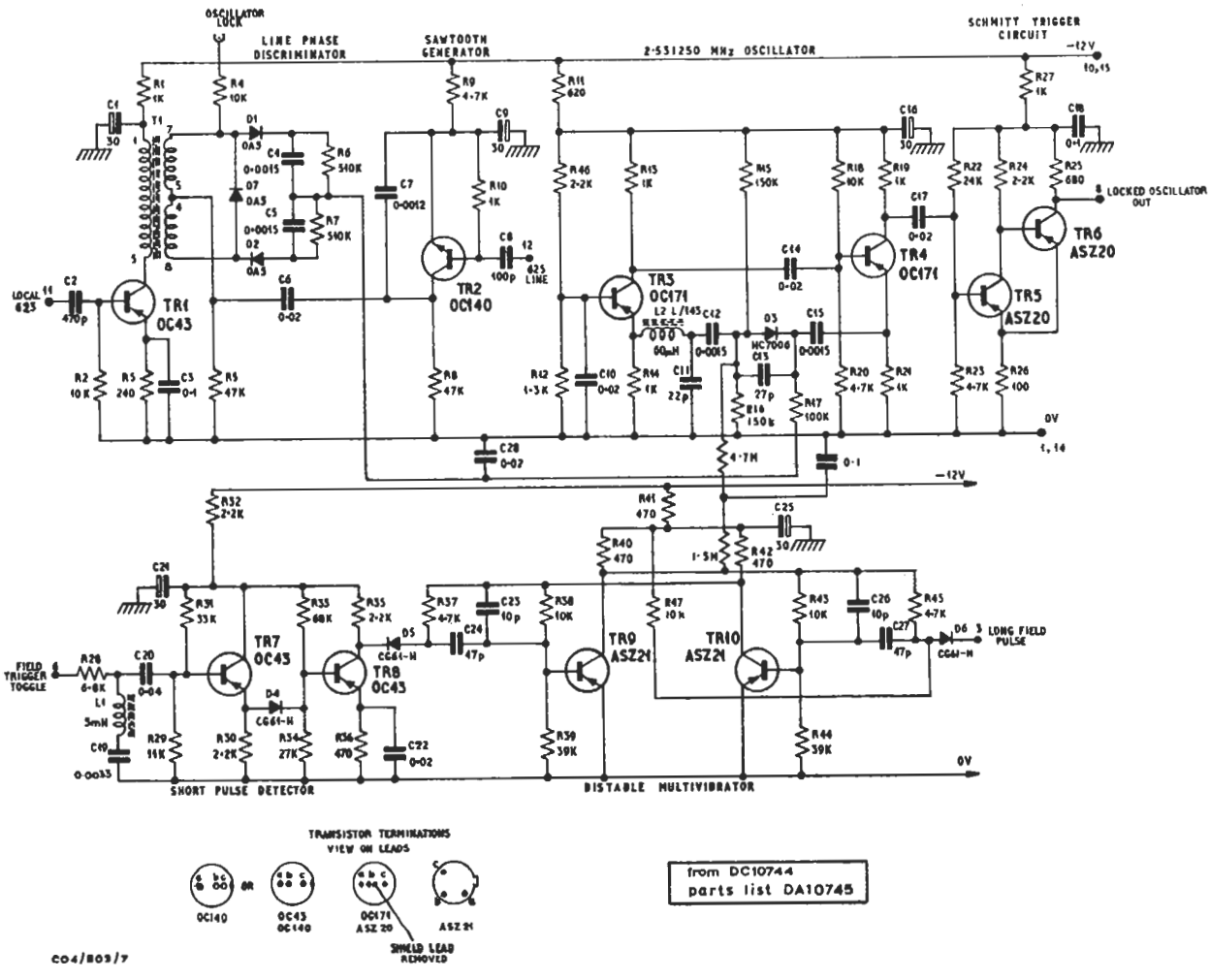


Fig. 7 Circuit of Unit 2

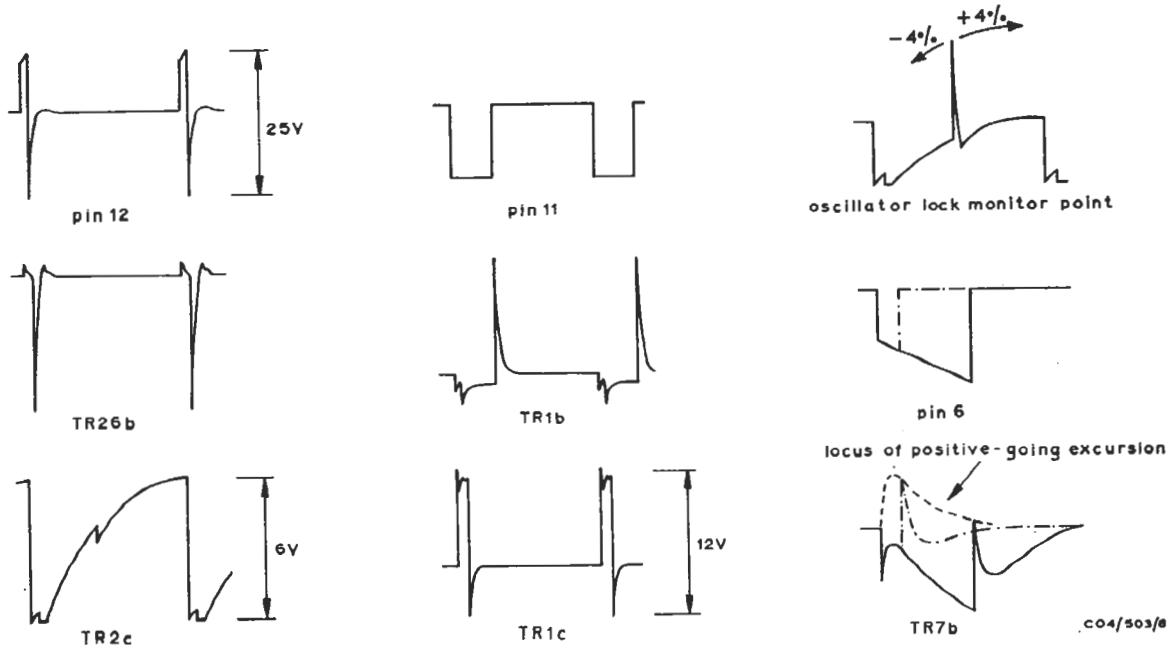


Fig. 8 Waveforms in Unit 2

These pulses in the secondary circuit of the transformer forward bias diodes D1 and D2 for the duration of the pulse. During this period the junction of resistors R6 and R7 is connected to the output of the sawtooth generator. The alternating component of the sampled pulses is filtered out to provide a d.c. signal to control the frequency of the master oscillator. The output of the master oscillator is fed to a Schmitt trigger circuit.

Field trigger pulses with a maximum duration of approximately 50 μs are fed via pin 6 to a circuit similar to the field-sync separator circuit of unit 1. Fig. 8 shows how the excursion of the positive-going transition of the pulse varies with the input pulse duration. This waveform at the emitter of transistor TR7 causes diode D4 to conduct at the end of input pulses which are less than about 7 μs in duration. Transistor TR8 inverts the pulses conducted by diode D4 to trigger a bistable circuit which includes transistors TR9 and TR10.

The bistable is triggered into the opposite state by pulses from unit 4 if the field trigger pulses are too long. For field trigger pulses of medium duration this bistable circuit can be in either state. This behaviour is summarised in Table 2.

Unit 3

Unit 3 which comprises six bistable circuits UN1/535 connected as shown in Fig. 2 forms part of the divide-by-162 counter.

Unit 4

The circuit of unit 4, given in Fig. 9, contains three bistable circuits UN1/535 which form part of the divide-by-162 counter.

A bistable circuit which includes transistors TR2

TABLE 2

Duration of pulse at pin 6 (μs)	*Trigger pulses at:*		*State of bistable circuit*
	D5	*D6*	
0—7	yes	no	TR9 conducting and TR10 cut off
7—36	no	no	the same as its previous state
36—50	no	yes	TR9 cut off and TR10 conducting

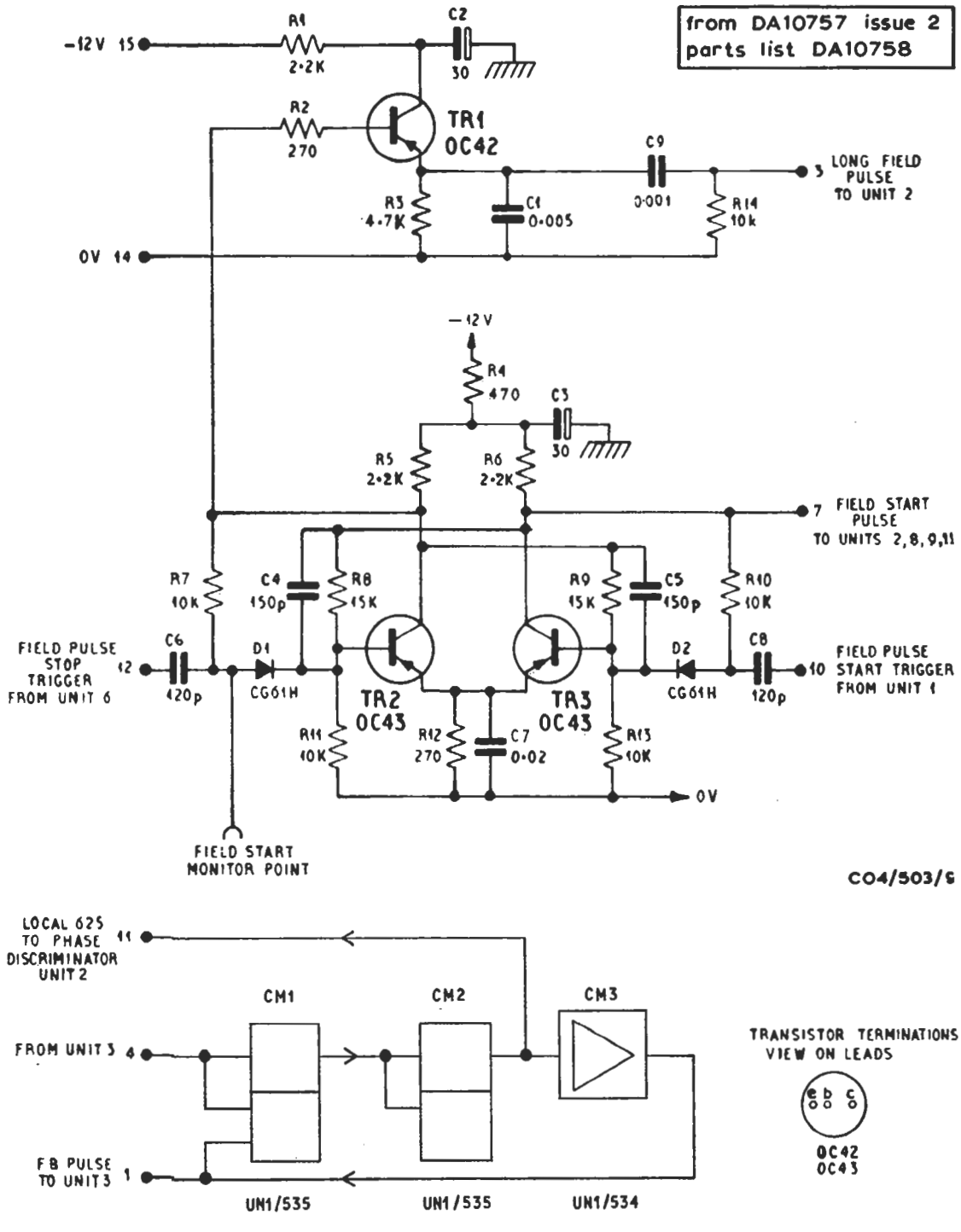


Fig. 9 Circuit of Unit 4

and TR3 is fed with 625 field-frequency pulses and with 405 twice-line-frequency pulses. The outputs are normal and inverted field trigger pulses. The positive-going field trigger pulses are fed via emitter follower TR1 to a pulse shaping network. During

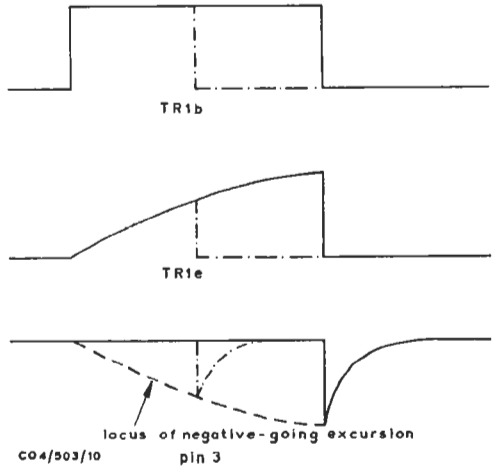


Fig. 10 Waveforms in Unit 4

the pulse, transistor TR1 is cut off and capacitor C1 discharges through resistor R3. At the end of the pulse, capacitor C1 is much more rapidly recharged through the transistor. The negative-going transition at the emitter is clipped because the transistor is normally bottomed. This is shown in Fig. 10. The signal at the emitter is differentiated by capacitor C9 and resistor R14 to give a negative-going pulse which occurs at the trailing edge of the input pulse and has an amplitude which increases with the duration of the input pulse.

Unit 5

Unit 5, which comprises five bistable circuits UN1/535 and one feedback pulse amplifier UN1/534 connected as shown in Fig. 2, forms part of the divide-by-125 counter.

Unit 6

Unit 6, which comprises four bistable circuits UN1/535 and two feedback pulse amplifiers UN1/534 connected as shown in Fig. 2, forms part of the divide-by-125 counter.

Unit 7

Unit 7 comprises six bistable circuits UN1/535 connected as shown in Fig. 2 to form the line-sync-and-front-porch pulse generator, the line blanking generator and the broad pulse generator.

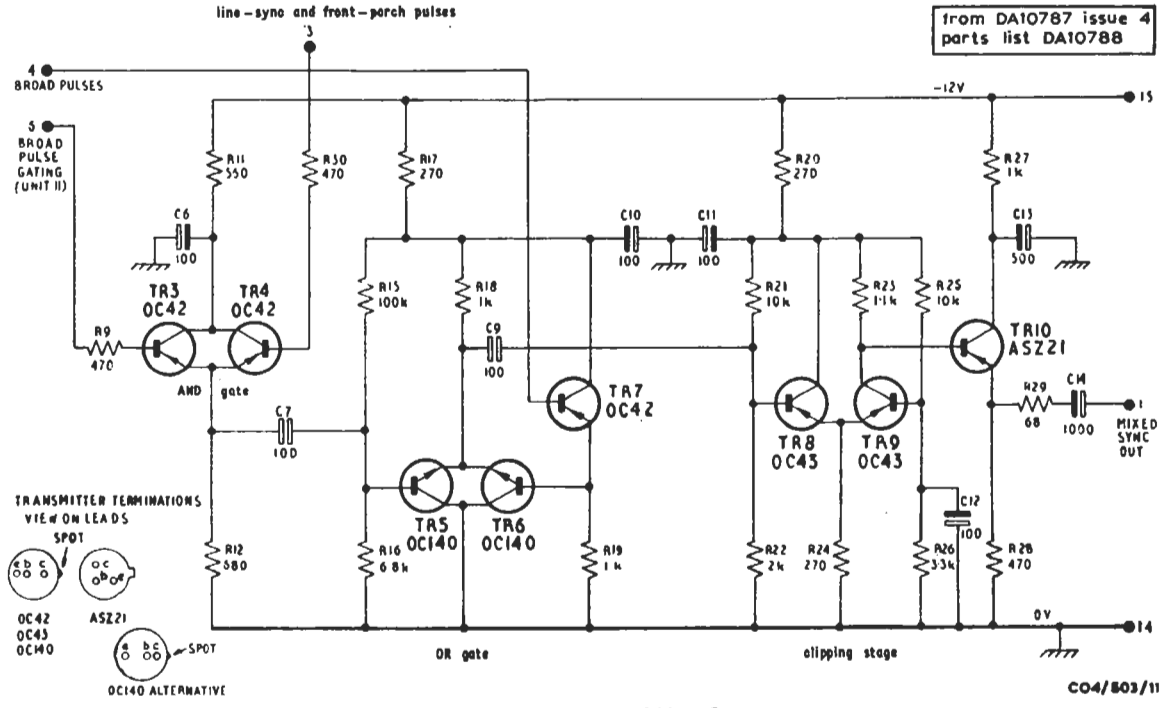


Fig. 11 Circuit of Unit 8

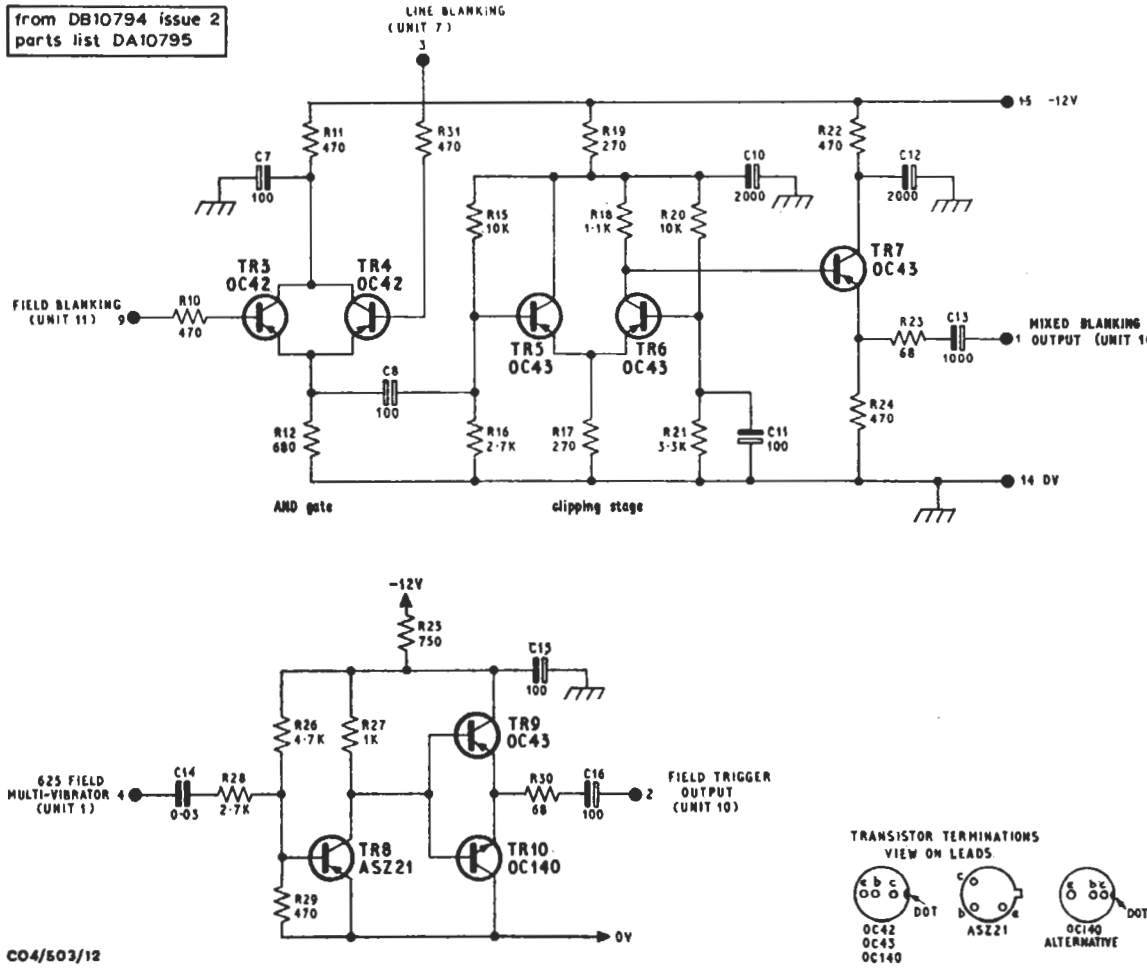


Fig. 12 Circuit of Unit 9

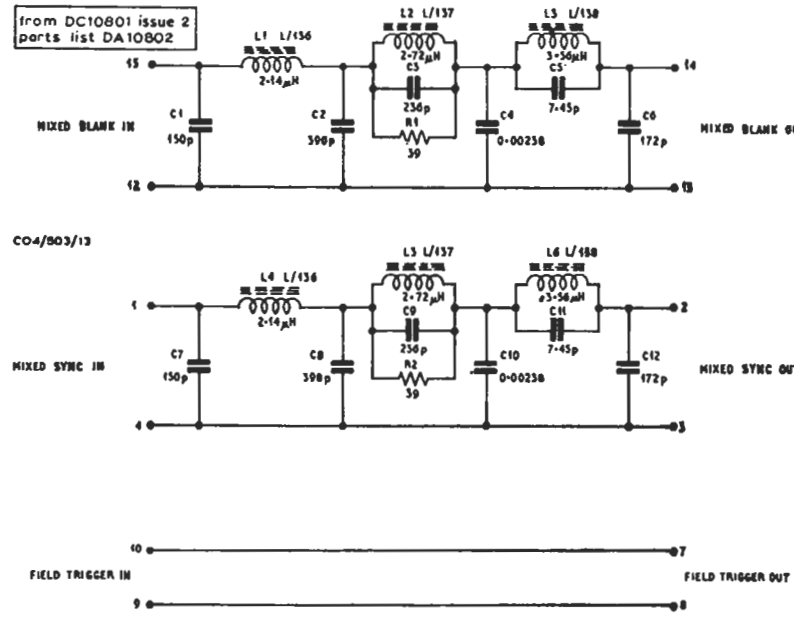


Fig. 13
Circuit of Unit 10

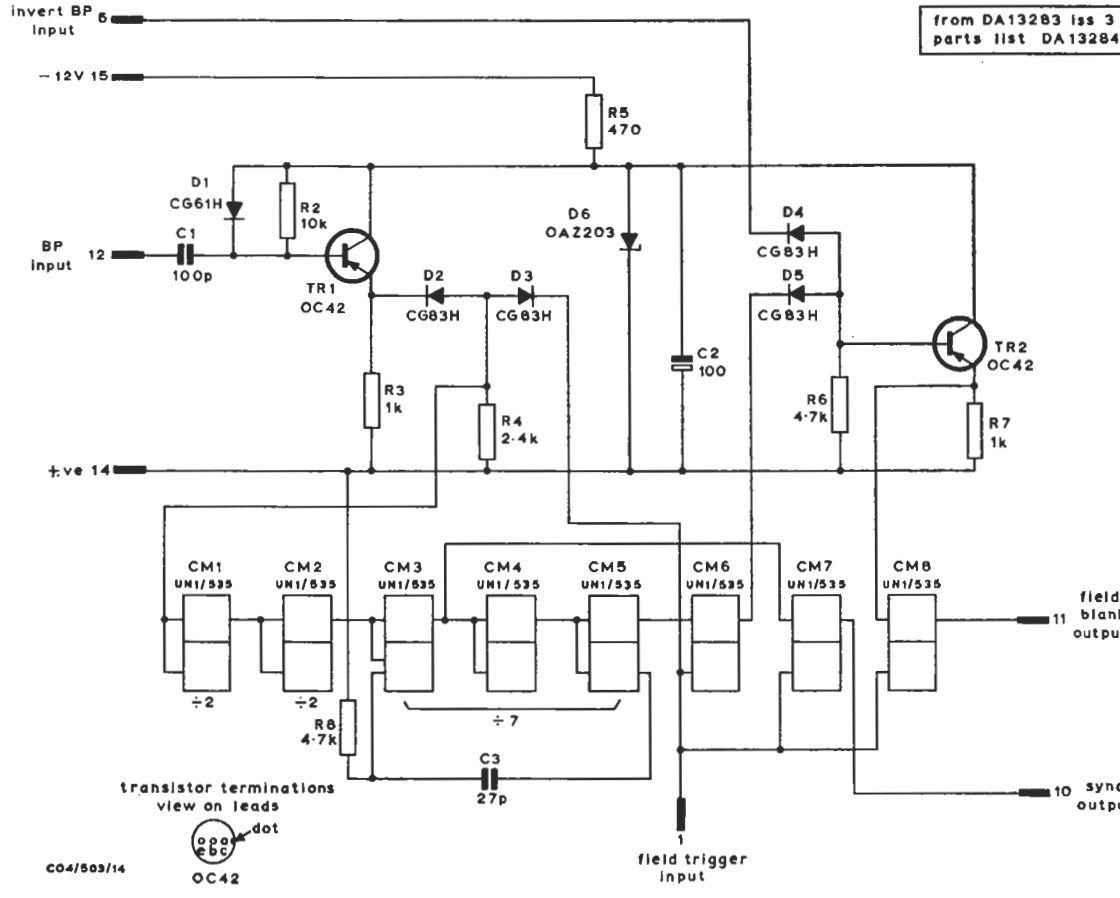


Fig. 14 Circuit of Unit 11

Unit 8

The circuit of unit 8 is given in Fig. 11. The output amplifier clips the signal thus improving the rise-time as well as removing spurious signals.

Unit 9

The circuit of unit 9 which is given in Fig. 12 also contains an output clipping amplifier similar to that in Unit 8.

Unit 10

The circuit of unit 10 which is given in Fig. 13 comprises two 4-MHz low-pass filters to increase the rise-times of the outputs to their proper value.

Unit 11

The circuit of unit 11 which is given in Fig. 14 includes seven bistable circuits UN1/535. The waveforms found in this circuit are given in Fig. 4.

Maintenance

In addition to the block diagram and waveforms already given the following table of transistor terminal voltages may be found useful in maintaining the CO4/503. The measurements given in Table 3 are made using an Avo Model 8 on the 10-volt range or the 25-volt range for voltages greater than 10 volts. The measurements are taken with no input signal and with unit 2 removed for measurement of any UN1/535.

TABLE 3

Unit and Transistor	*Terminal Voltages* Emitter	Base	Collector
Unit 1			
TR1	−0·6	−0·8	−5·6
TR2	−5·5	−5·6	−9·7
TR3	−0·6	+3·5	−9·7
TR4	−3·0	−3·9	−0·1
TR5	−0·1	−0·1	−11·3
TR6	−2·4	−2·6	−6·1
TR7	−2·4	−1·4	−9·9
Unit 2			
TR1	0	0	−12·0
TR2	−11·8	−11·7	−0·1
TR3	−2·6	−2·7	−4·8
TR4	−2·6	−2·3	−4·6
TR5	−0·6	−0·5	−0·9
TR6	−0·6	−0·9	−2·0
TR7	−9·3	−8·9	−11·5
TR8	−8·6	−8·7	−8·6
TR9	0	−0·4	−0·3
TR10	0	−0·4	−0·3
Unit 4			
TR1	−8·5	−8·7	−8·7
TR2 } on	−1·1	−1·4	−1·2
TR3 } off	−1·1	−0·5	−8·7

Unit and Transistor	*Terminal Voltages* Emitter	Base	Collector
Unit 8			
TR3	−0·7	−0·3	−11·4
TR4	−0·7	−0·8	−11·4
TR5	−0·9	−0·8	0
TR6	−0·9	−4·4	0
TR7	−4·4	−4·5	−8·8
TR8	−2·1	−2·2	−9·4
TR9	−2·1	−2·1	−2·4
TR10	−2·1	−2·4	−7·6
Unit 9			
TR3	−1·2	−0·3	−11·1
TR4	−1·2	−1·3	−11·1
TR5	−2·5	−1·9	−9·1
TR6	−2·5	−2·0	−3·1
TR7	−3·0	−3·1	−9·0
TR8	0	−0·3	−0·2
TR9	−0·2	−0·2	−6·4
TR10	−0·2	−0·2	0
Unit 11			
TR1	−5·1	−5·2	−6·2
TR2	−1·0	−1·2	−6·2

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