TONE DECODERS DM1/1A–E

General Description

These decoders accept a tone input of a specified frequency and provide an output which switches to about −24 volts d.c. from almost 0 volts when the input rises above a predetermined level.

The DM1/1A and DM1/1B are employed together, operating at frequencies 200 Hz apart, in each of the sound automatic monitors MN2M/4A and MN2M/6A. The decoders are tuned to different pairs of frequencies, depending on the cut-off frequencies of the links to be monitored, as shown in a table with the circuit diagram on page 3. The two associated decoders have their gains clamped by commoning their a.g.c. lines. The DM1/1A and B have also been installed in network switching arrangements.

The DM1/1C, D and E are modified versions intended for continuity monitoring and programme identification in the Open University (Radio) distribution network. Each may be used to operate a 24-volt relay from its switching output circuit. Normally they are tuned to function at 7·6, 7·8 and 8·0 kHz respectively. They differ from the DM1/1A and B in having better frequency discrimination, no a.g.c., longer operate and release delay times, and they present a balanced high input impedance which can be bridged directly across a programme chain.

Each unit comprises a printed circuit board on a chassis CH1/12A. The DM1/1A and DM1/1C have indexing pegs at positions 25 and 28; the DM1/1B and DM1/1D have pegs at positions 1 and 32; and the DM1/1E has pegs at positions 49 and 81.

Circuit Description, DM1/1A and B

General

Each decoder is in two main sections. The first section is a three-stage amplifier, tuned to one of the monitoring-tone frequencies, *A* or *B*, and having amplified a.g.c. derived from its output after rectification. The rectified output of the amplifier is applied via a level-setting control to the second section of the decoder, comprising a Schmitt trigger circuit which includes a transistor switch in the output of the unit.

Operation

TR1 to TR3 form a three-stage amplifier tuneable to the monitoring-tone frequencies by means of C6 and the core of T1 and C10 and the core of T2. The output from T2 is rectified by the cascade voltage-doubler C12, D1, D2 and C13, and the d.c. voltage across C13 is used to control the gain of the amplifier. When this exceeds the voltage drop across D3, TR8 conducts and lowers the voltage at the junction of R24 and R5, reducing TR2 base current and current gain. For the normal working input range of −38 to −22 dB, the level on T2 secondary (pin 4 on the board) changes by 0·2 dB.

The overall time-constants required for successful operation of the units preclude the use of high *Q* circuits in the tuned stages, and in consequence the discrimination against operation of one unit by a signal at the frequency of an associated decoder, 200 Hz off, is only about 8 dB in decoders tuned to the higher tone frequencies used. This figure is well within the range of the a.g.c. and, with this discrimination alone, tone *A* would operate unit *B* but for the fact that their a.g.c. lines are clamped by connecting together PLA pin 12 on the two units. This maintains equal gains in both units irrespective of the input tone frequency, provided the setting-up procedure described later has been carefully carried out. Frequency discrimination which may occur elsewhere in the monitoring chain may have the effect of reducing the safety margin of operation, and therefore it is important that the two units work together correctly as a pair. However, in later monitors, these decoders are fed through AM1/35 units which provide supplementary discrimination that improves the safety margin.

TR6 and TR7 form a trigger circuit and output switch. With no input to the unit, C13 is discharged and the low negative voltage out of the compound pair TR4 and TR5 causes the base of TR6 to be biased off relative to the emitter voltage developed across D5. When an input causes a voltage across C13, TR6 conducts at a point depending on the setting of RV1 and TR7 also conducts. Feedback via R20 and C15 accelerates this action and the output terminal PLA pin 13 changes from almost zero volts to nearly −24 volts.

Circuit Description, DM1/1C, D and E

This circuit differs from that of the DM1/1A and B as follows:

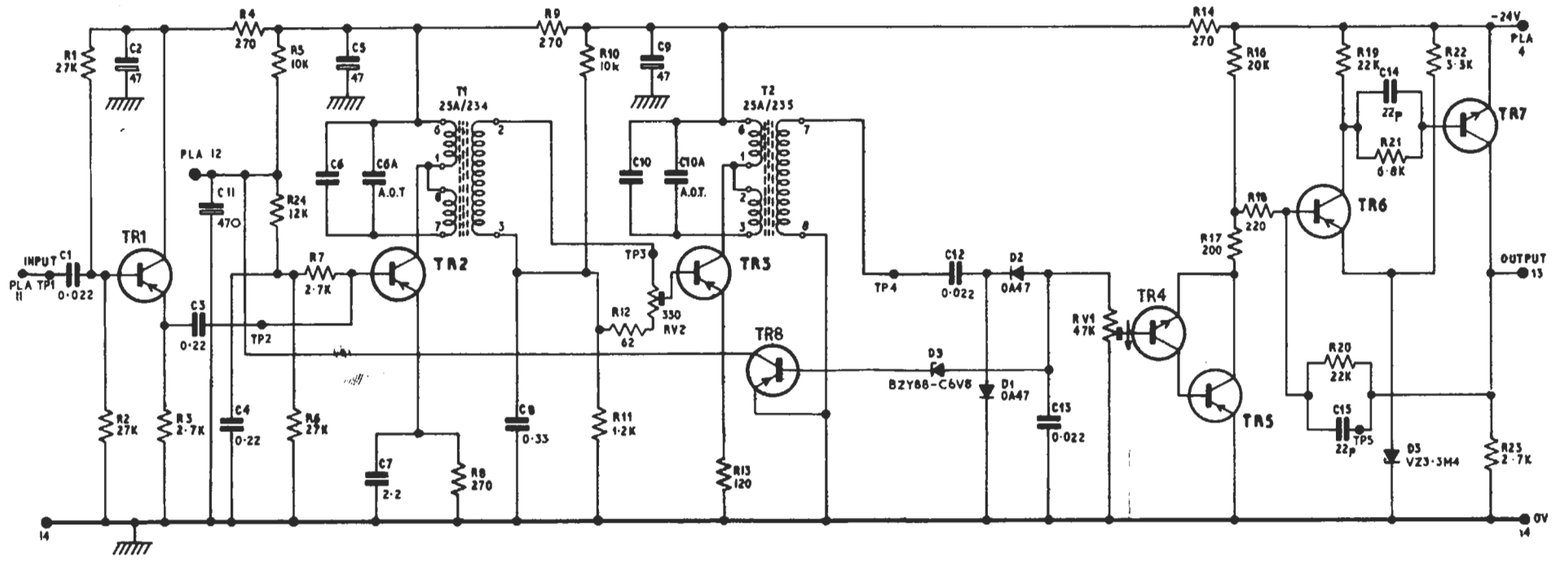
(a) A transformer precedes the first transistor TR1 and, with two series resistors, provides a balanced high-impedance input to the unit. The transformer secondary with C17 in parallel is tuned, and together with a reduced value of C1 coupling to TR1 base, this produces greater discrimination in favour of the signals to be detected. The discrimination against signals 200 Hz off exceeds 20 dB.

(b) The a.g.c. circuit used in the DM1/1A and B, including a transistor and diode, has been omitted.

(c) A resistor and capacitor, R25 and C16, have been added between the reservoir capacitor C13 and TR4 to increase the operating and release delay times of the output switching action.

(d) The voltage rectified after tuned transformer T2 is fed to pin 8 on the multiway connector PLA, from which it can be applied to separate equipment (e.g. an ME1/6 measuring the tone level detected by the decoder).

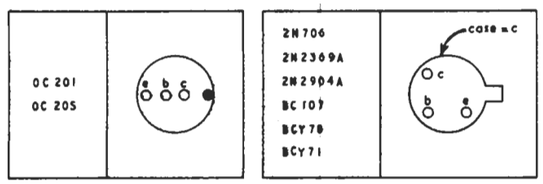
continued on page 4



from DI7310 A3
parts list DI7311 A4

TP INDICATES TEST POINTS ON PRINTED BOARD

TRANSISTOR TERMINATIONS
VIEW ON LEADS

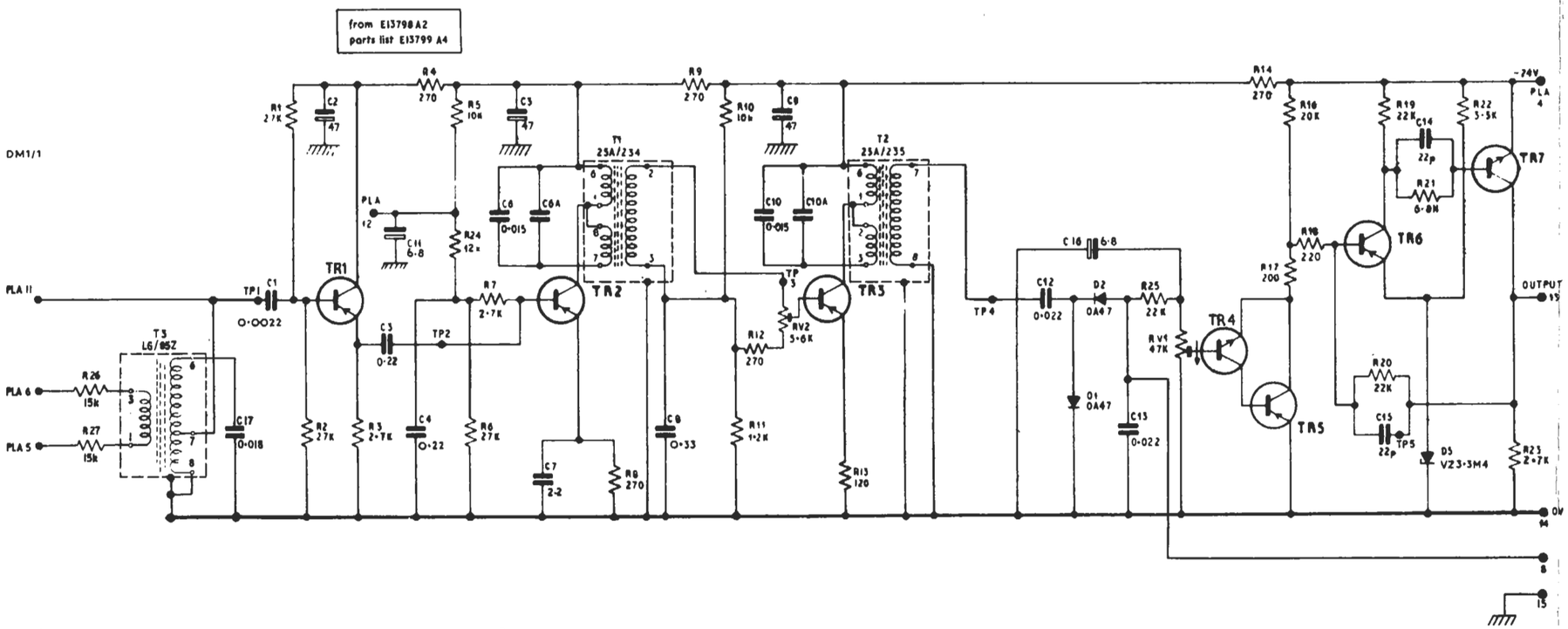


LINE f_{co}	DECODER A f_{res}	C6	C6A	C10	C10A	DECODER B f_{res}	C6	C6A	C10	C10A
8kHz	7·6kHz	0·015	A.O.T.	0·015	A.O.T.	7·8kHz	0·015	A.O.T.	0·015	A.O.T.
9kHz	8·6kHz	0·012	A.O.T.	0·012	A.O.T.	8·8kHz	0·012	A.O.T.	0·012	A.O.T.
10kHz	9·6kHz	0·01	A.O.T.	0·01	A.O.T.	9·8kHz	0·01	A.O.T.	0·01	A.O.T.
11kHz	10·6kHz	0·0082	A.O.T.	0·0082	A.O.T.	10·8kHz	0·0082	A.O.T.	0·0082	A.O.T.
13kHz	12·6kHz	0·0056	A.O.T.	0·0056	A.O.T.	12·8kHz	0·0056	A.O.T.	0·0056	A.O.T.
15kHz	14·6kHz	0·0039	A.O.T.	0·0039	A.O.T.	14·8kHz	0·0039	A.O.T.	0·0039	A.O.T.

TR	pre 1975	1975
1, 2, 5, 6 & 8	OC 201	2N2904A
3	OC 205	BCY 70
4	2N 706	2N2369A
7	BC107	

Circuit of DMI/IA and B (above)

Circuit of DMI/IC, D and E (below)



DECODER	FREQUENCY	C6A & C10A
DMI/IC	7·6kHz	0·0022
DMI/ID	7·8kHz	0·0012
DMI/IE	8·0kHz	open circuit

TR	pre 1975	1975
1, 5, 6	OC 201	2N2904A
3	OC 205	BCY70
4	2N 706	2N2369A
2	BCY 71	
7	BC 107	

Adjustment and Testing, DM1/1A and B

Power Supply

The unit requires a supply of 24 volts connected to PLA pin 14 (positive) and PLA pin 4. The total current consumption is 40 mA.

Adjustment

1. Apply tone at the intended operating frequency of the decoder, accurate to ±10 Hz, to PLA pins 11 and 14, via a 1:1 ratio repeating coil. Set the input to the decoder at −60 dB.
2. Connect an oscilloscope or meter to indicate the signal level at board test pin 4. Set RV2 at maximum (fully clockwise) and adjust the cores of T1 and T2 for maximum level at test pin 4. Whenever this voltage exceeds 2 volts p-p, reduce the tone input. Disconnect the level indicator.
3. Connect an Avometer 8 across C13. Set RV1 to maximum. Raise the tone input until the output at PLA pin 13 switches. The voltage across C13 should then be −3·2 ±0·3 volts, and the input for this condition should be as follows, according to the operating frequency:

−63 to −68 dB at	7·6 or	7·8 kHz
−63 to −68 dB at	8·6 or	8·8 kHz
−63 to −68 dB at	9·6 or	9·8 kHz
−63 to −68 dB at	10·6 or	10·8 kHz
−66 to −72 dB at	12·6 or	12·8 kHz
−68 to −73 dB at	14·6 or	14·8 kHz

Some early units, if unmodified, may require more input.

4. Connect the Avometer 8, on its 2·5-volt range, across PLA pins 12 and 14. Increase the input tone to −30 dB. Adjust RV2 to obtain −1 volt at PLA pin 12. Reduce this negative voltage if possible by readjusting the cores of T1 and T2. Adjust RV1 again to obtain −1 volt.
5. Measure the voltage across C13, which should be about 7 volts.
6. Connect the Avometer, on its 25-volt range, to the slider of RV1 and PLA pin 14. Adjust RV1 to obtain −4·5 volts on its slider. Confirm that the output switching circuit has operated (i.e. PLA pin 13 is at almost −24 volts).

Test Procedure

As a check on the proper functioning of the circuit, the following measurements may be made.

1. Apply an input of −20 dB at the operating tone frequency of the unit and reduce the input until the output switching circuit releases (i.e. PLA pin 13 switches to about 0 volts). Note the input level at which this occurs.
2. Change the frequency of the tone by 200 Hz to the other frequency of the pair.
3. Increase the input level until the output switching circuit just operates again. The required increase, which gives a measure of the discrimination of the tuned circuits, should exceed:

15·0 dB at	7·6 or	7·8 kHz
14·0 dB at	8·6 or	8·8 kHz
11·0 dB at	9·6 or	9·8 kHz
10·0 dB at	10·6 or	10·8 kHz
8·0 dB at	12·6 or	12·8 kHz
6·0 dB at	14·6 or	14·8 kHz

4. Connect the DM1/1A and DM1/1B, in a pair, together with their a.g.c. lines (PLA pin 12 on each) linked. Apply an input of tone A to both units, raising the input from a low level, and check that the output of the DM1/1A has switched when the input is −38 dB and that output of the DM1/1B has not switched at −22 dB.
5. Repeat operation 4 using tone B and check that the DM1/1B operates but not the DM1/1A.

Adjustment, DM1/1C, D and E

Power Supply

The unit requires a supply of 24 volts connected to PLA pin 14 (positive) and PLA pin 4. The total current consumption is about 35 mA.

Adjustment Procedure

1. Set RV2 to maximum and RV1 to minimum (i.e. both fully clockwise).
2. Apply tone at the intended operating frequency of the decoder, accurate to ±5 Hz, via a 1:1 ratio repeating coil to PLA pins 5 and 6. Ensure that the tone source is terminated correctly, and set the input to the decoder at −40 dB.
3. Connect an oscilloscope or meter to indicate the signal level at board test pin 3. Adjust the cores of T3 and T1 for maximum level at this point.
4. Reduce the input tone to −53 dB. Move the level indicator to test pin 4. Adjust the core of T2 for maximum level at this point.
5. Connect an Avometer 8, on its 25-volt d.c. range, to PLA pins 8 and 14. Trim the cores of T3, T1 and T2 to obtain maximum meter reading.
6. Bring RV1 to maximum. The output switching circuit should operate (so that PLA pin 13 changes from almost 0 volts to nearly −24 volts). Check the switching with a lamp, meter or relay between PLA pins 13 and 14.
7. Reduce the input tone level so that the output switching circuit releases. Raise the input again and find the minimum level at which the output switches. This should be between −60 and −53 dB.
8. Connect the Avometer 8, on its 25-volt d.c. range, to PLA pins 8 and 14. Set the input tone level to −40 dB. Readjust the cores of T1 and T2 slightly to ensure they are set for maximum amplification, and then adjust RV2 to obtain a reading of −5·0 volts on the meter.
9. Adjust RV1 so that the output at PLA pin 13 switches when the input level is raised to −40 dB from a lower level (or so that it switches at a level 5 dB to 10 dB below the nominal level of the tone to which the decoder must respond in use).

Installation and Operation, DM1/1C, D and E

These decoders are capable of energising an external 24-volt miniature relay of the S.T.C. series 250 (enclosed) type or the completely sealed variety. A reversed-biased diode of suitable type (e.g. an OA202) should be connected across the relay coil to absorb the voltage peak when the energising current is cut off.

In use these decoders should be set to a sensitivity greater than necessary to respond to the nominal level of the received tone to allow for variations in transmission equivalent. An excessive sensitivity will increase the susceptability to spurious operation due to programme break-through when a sending-end filter is not employed. In practice the sensitivity may be set 5 dB or 10 dB greater than the nominal tone level (usually −35 dB), depending on the function of the decoder.

When the decoders are used on a circuit employing automatic monitors MN2M/3 to 6, or MN2M/3A to 6A, it is recommended that the sending-end filter should have a cut-off frequency of 7·25 kHz or less. The decoders will then operate satisfactorily at a sensitivity of −50 dB, permitting a tone level of −45 dB.

Modified Operating Delay, DM1/1C, D and E

Originally C16 was 50 μF, a value chosen so that the output switching operate and release delay times were about 2 seconds. But subsequently this amount of delay was found unwanted and C16 has been changed to 6·8 μF, reducing the operate and release delay times to about 0·25 second.

WWM(X) 12/67
Revised DPEB 3/72
Revised DPEB 5/75