TONE GENERATOR GE1/3

General Description

The GE1/3 contains two separate fixed-frequency audio oscillators each comprising an *LC* oscillator stage followed by a tuned amplifier stage. Across each amplifier output are transistor switches controlled by NAND gates whose inputs are derived from 0-volt or −24-volt d.c. signals. When one or both of the switches are open, the generated tone or tones are taken to a tuned bandpass transformer output stage.

The unit was designed for use in sound automatic monitor MN2M/3 or MN2M/5. In this application the 0-volt or −24-volt input signals are supplied by processing amplifiers in the monitor. The generated tone frequencies are spaced 200 Hz apart and are positioned a little below the cut-off frequency of the transmission link being monitored.

The unit consists of a printed circuit board on a chassis CH1/12A, with indexing pegs at positions 22 and 27.

Circuit Description (Fig. 1)

The circuits of the first stages TR1 and TR3 of the two oscillators are similar to that of the OS2/5 described in Instruction T.10 Appendix D. The oscillator outputs are amplified by transistors TR2 and TR4, which have flatly tuned transformers T1 and T2 in their collector circuits.

One or more of the resistors R5 to R9 and R20 to R24 can be short-circuited as a means of fine oscillator-frequency adjustment. This facility is not used in some applications of the GE1/3 and it is now common for all these resistors to be short-circuited by straps.

When the GE1/3 is used in an automatic monitoring system, the two oscillator frequencies *A* and *B*, set by adjusting L2 and L4, differ by 200 Hz. The two operating frequencies used depend on the cut-off frequency of the link being monitored, as shown in the table at the bottom of Fig. 1.

The secondary of transformer T1 is connected via the tone-A level control RV1 and isolating pad R33, R39 and R40 to the base of output transistor TR9. A transistor switch, TR6, controlled by NAND gate TR5, D1, D2 and D5, is connected across R33. The secondary of T2 is similarly connected to TR9 base, via RV2, R37, R38 and R40. Transistor switch TR8, controlled by a second gate, TR7, D3, D4 and D6, is connected across R37.

Considering the first gate, if 0 volts (or an open circuit) is applied to both PLA pin 12 and circuit board pin 17, then current flows via R34 through D1 causing TR5 to conduct and produce a potential of almost −24 volts at its collector. This switches TR6 into a conducting state which short-circuits R33 and eliminates the tone from TR1. However, if −24 volts is applied to PLA pin 12 or board pin 17, D2 or D5 conducts and the junction of R34 with D1 takes up a potential which is insufficiently positive relative to −24 volts to cause D1 and TR5 (both silicon semiconductors) to conduct. TR6 is then cut off and the tone from TR1 reaches TR9.

The second gate, including TR7, controls TR8 and the tone from TR3 in the same way.

If there is a link between circuit board pins 11 and 18 (as when the GE1/3 is used in an MN2M/3 or MN2M/5), then when TR5 conducts because the inputs to D2 and D5 are 0 volts or open circuit, the resulting potential of almost −24 volts at TR5 collector is applied to the second gate through D6 and cuts off TR7 and TR8. Thus, with this link, when the tone from TR1 is cut off, the tone from TR3 is an automatic output, but if −24 volts is applied to PLA pin 12 the tone from TR1 is obtained, and if −24 volts is applied to PLA pins 12 and 11 both tones are obtained.

Adjustment and Testing

Power Supply

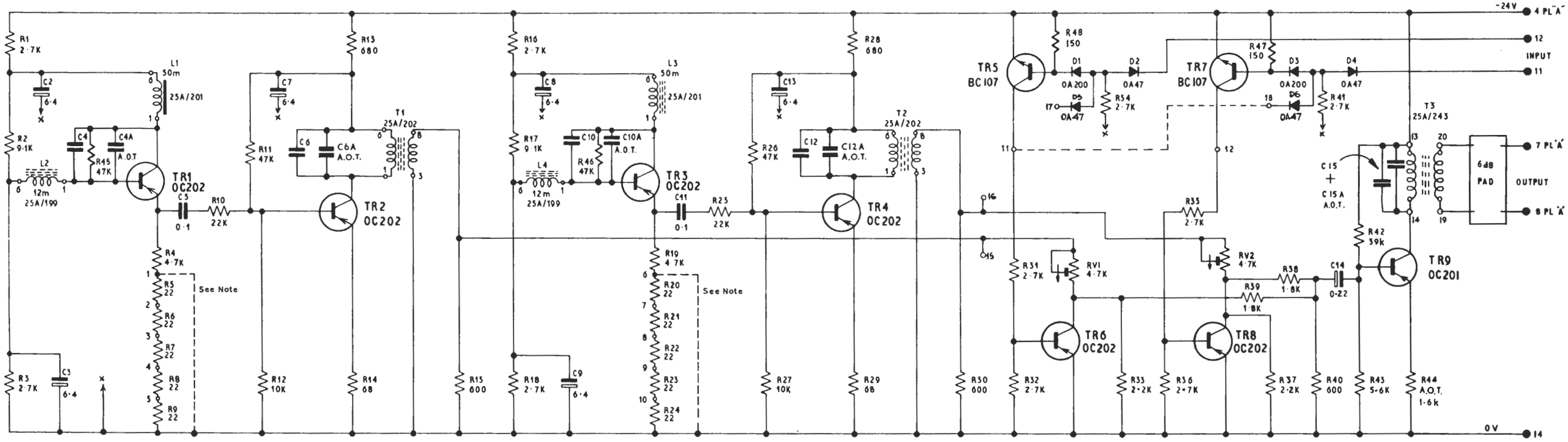
The unit requires a supply of 24 volts d.c. connected to PLA pin 14 (positive) and PLA pin 4 (negative). The total current consumption is 65 ±10 mA

Test Apparatus Required

Oscilloscope
Frequency counter
A.C. test meter ATM/1 (AD mode)

Adjustment

1. Check that the frequency-determining capacitors C4, C6, C10, C12 and C15 have already been fitted (and if necessary adjusted in value by added capacitors) as specified in the table below Fig. 1. If there is a strap between board pins 11 and 18 (or between 12 and 17), temporarily open-circuit this.
2. Apply −24 volts (relative to PLA pin 14) to PLA pin 12.
3. Connect an oscilloscope to board pin 15 and the positive side of C9. Adjust RV1 to obtain maximum displayed waveform and check that this is substantially sinusoidal.
4. Substitute a counter for the oscilloscope at board pin 15 and adjust the core of L2 to obtain the mean frequency between the tones A and B specified for the unit. Remove the counter.
5. Connect the oscilloscope (or the high impedance input of an ATM/1) to the junction of R38 and R39. Set RV1 to obtain 400 mV peak-to-peak on the oscilloscope (or −15 dB on the ATM/1).
6. Connect the input of the ATM/1 and a 600-ohm termination (in or external to the ATM/1) to PLA pins 7 and 8. Adjust the core of T3 for maximum signal reading on the ATM/1.
7. Restore the counter to board pin 15. Reset the core of L2 so that the counter indicates the required tone-A frequency plus 10 Hz. Note the output level in 600 ohms read on the ATM/1 at PLA pins 7 and 8. (The frequency is set 10 Hz high when the unit is exposed for adjustment so that it will be within its limits when the unit is mounted with other equipment.)
8. Connect the oscilloscope or ATM/1, as in step 5, to the junction of R38 and R39. Check the level of the signal present. Remove the −24 volts from PLA pin 12. The signal should cut, confirming that the gate operates.
9. Apply −24 volts to PLA pin 11.
10. Connect the oscilloscope to board pin 16. Adjust RV2 to obtain maximum displayed waveform and check that this is substantially sinusoidal.
11. Substitute the counter at board pin 16 and adjust the core of L4 so that the counter indicates a frequency 10 Hz above the required tone B. Remove the counter.
12. Adjust RV2 to obtain the same voltage at the junction of R38 and R39 as in steps 5 and 8.
13. Connect the ATM/1 (with 600 ohms internal or external termination) to PLA pins 7 and 8. The output level of tone B should be close to that of tone A noted in step 7, within say 0·5 dB.



Note: optional bias resistors R5-9 and R 20-24 normally short-circuited

from D17426 A2
parts list D 17427 A4

GE1/3/1TA

LINE f CO*	C4	C4A	C6		f. RES. A	C10	C10A	C12		f. RES. B.	C. 15	C. 15A	f. RES A/B
8 KHz	0·0068	330 PF	0·0056		7·6 KHz	0·0068		0·0056		7·8KHz	0·039	2200 PF	7·7 KHz
9 KHz	0·0056		0·0047		8·6 KHz	0·0056		0·0047		8·8 KHz	0·033	2000 PF	8·7 KHz
10 KHz	0·0033	390 pf	0·0027		9·6KHz	0·0033	100 pf	0·0027		9·8 KHz	0·022	5100pF	9·7 KHz
11 KHz	0·0027	330	0·0022		10·6 KHz	0·0027	100	0·0022		10·8 KHz	0·018	4700pF	10·7 KHz
13 KHz	0·0018	330	0·0015		12·6 KHz	0·0018	180	0·0018		12·8 KHz	0·015	2700pF	12·7 KHz
15 KHz	0·0015	100	0·0012		14·6 KHz	0·0015		0·0012		14·8KHz	0·01	1800pF	14·7 KHz
	0·0056	820 pF	0·0056		8·0 kHz	0·0056	820pF	0·0056		8·0 kHz	0·033	0·0068	8·0kHz

o — INDICATES TEST POINTS ON PRINTED BOARD

Fig.1. Circuit of GE1/3

*Relates to sound automatic monitor systems using GE1/3

14. Apply −24 volts to PLA pin 12, as well as pin 11. The output at PLA pins 7 and 8 should increase by about 3 dB. (The ATM/1 must be in the AD condition for this check.)
15. With −24 volts on only PLA pin 12, check that RV1 varies the output from about −10 to −20 dB. Repeat this check with −24 volts on PLA pin 11 and varying RV2. If necessary, select a new value of R44 so that the upper end of the output range is about −10 dB. Set RV1 and RV2 so that each tone output is −15 dB.
16. Fit a strap between board pins 11 and 18 (or between pins 12 and 17) if the intended use of the unit requires this.

Test Procedure

As a check on the proper functioning of a unit which has previously been adjusted, the following tests may be made.

1. Apply −24 volts to PLA pins 11 and/or 12 and confirm that tone A and tone B are obtained at PLA pins 7 and 8 as follows:

PLA-11	*PLA-12*	*PLA-7 & PLA-8*
0 V	−24 V	Tone A
−24 V	0 V	Tone B
−24 V	−24 V	Tones A and B
0 V	0 V	No tone, or tone B if board pins 11 and 18 are strapped, or tone A if board pins 12 and 17 (D5) are strapped.

2. If a counter is available, check that tones A and B have the correct frequencies, within ±10 Hz, when the unit is mounted with associated equipment and has warmed up under normal operating conditions.
3. Using an ATM/1, arranged internally or externally to present a load of 600 ohms, check that the output of each tone is separately at the required level. This is nominally −15 dB at PLA pins 7 and 8, but a different level may be required from the GE1/3 in a particular system. The levels of tones A and B are set by RV1 and RV2 respectively.

Voltage Measurements

The voltages shown in Table 1 are typical values, measured between the emitter of the transistor and the 0-volt line, using an Avometer Model 8 on its most suitable range.

TABLE 1

Transistor	*Emitter Volts*
TR1, TR3	3
TR2, TR4	1
TR9	2·5

WWM(X) 12/67
Revised DPEB 3/72