WAVEFORM GENERATOR DRIVE UNITS

GE1/520 and GE1/520A

Introduction

These drive units are used in picture source synchronising[1] systems to generate, from a stable crystal oscillator, waveforms at twice-line and field frequencies on the 625-line standard.

Both units are used in Natlock systems and the GE1/520A additionally provides fast-genlock operation. The drive units comprise the following units which are mounted in the order given from left to right in a PN3/23 chassis:

PS2/36	Power Supplier
OS2/505,A	Oscillator (4·429 687 5 MHz)
UN17/504	Control Unit
UN17/501	Variable Divider (GE1/520)
or UN17/522	Variable Divider, Genlock(GE1/520A)
UN17/502	Fixed Divider
UN17/503	Picture and Field Unit

General Specification

Signal Inputs

Mixed Syncs	2 V p-p	
Error Control Signals	*A′*, *R′*, *F′*	0 V: do nothing
	XF′ (A version only)	−6 V: change count
Frequency Control	from UN17/509	

Signal Outputs

Oscillator, f_{NAT}	4·429 687 5 MHz, 1 V p-p into 75 ohms
Twice-line, f_{2L}	31·250 kHz, 1 V p-p into 75 ohms
50 CPS, f_F	50 Hz squarewave, 2 V p-p into 75 ohms

Oscillator

Stability	better than 2 parts in 10^7
Warm-up time	2 hours to achieve stability
Oven temperature	50°C

Controls

Local/Remote (UN17/504)	gives manual or automatic control of f_{2L} and f_F output phase and frequencies
Advance/Retard (UN17/504)	with *Local* selected, gives manual *Advance* or *Retard* changes of 1 part in 5 600 to f_{2L} and f_F outputs
Frequency Control (OS2/505,A)	gives 10 to 50 Hz variation of f_{NAT}
Frequency Control (rear panel)	gives 2 to 8 Hz variation of f_{NAT}

Power Input

Mains	200 to 250 V, 200 mA, a.c. (fused at 1 A)
Battery (OS2/505,A only)	−12 V or −18 to −28 V, 1·25 A max. (each fused at 2·5 A)

Power Output	
from Mains input	−12 V, 2 A, d.c. (fused at 4 A)
Operating Temperature	−10°C to +45°C ambient (GE1/520) 0°C to 45°C ambient (GE1/520A)
Weight	11 kg (24 lb)
Connectors	
Mixed Syncs 50 CPS Twice-line Oscillator	PL259 sockets
Monitor	4-mm sockets
External Control (error signals)	XLR-5-31 socket (GE1/520) Painton series 159, 11-pole socket (GE1/520A)
Frequency Control (from UN17/509)	XLR-4-31 socket
Battery	XLR-4-32 plug
Oscillator Link	PO No. 1 (Musa) U-link

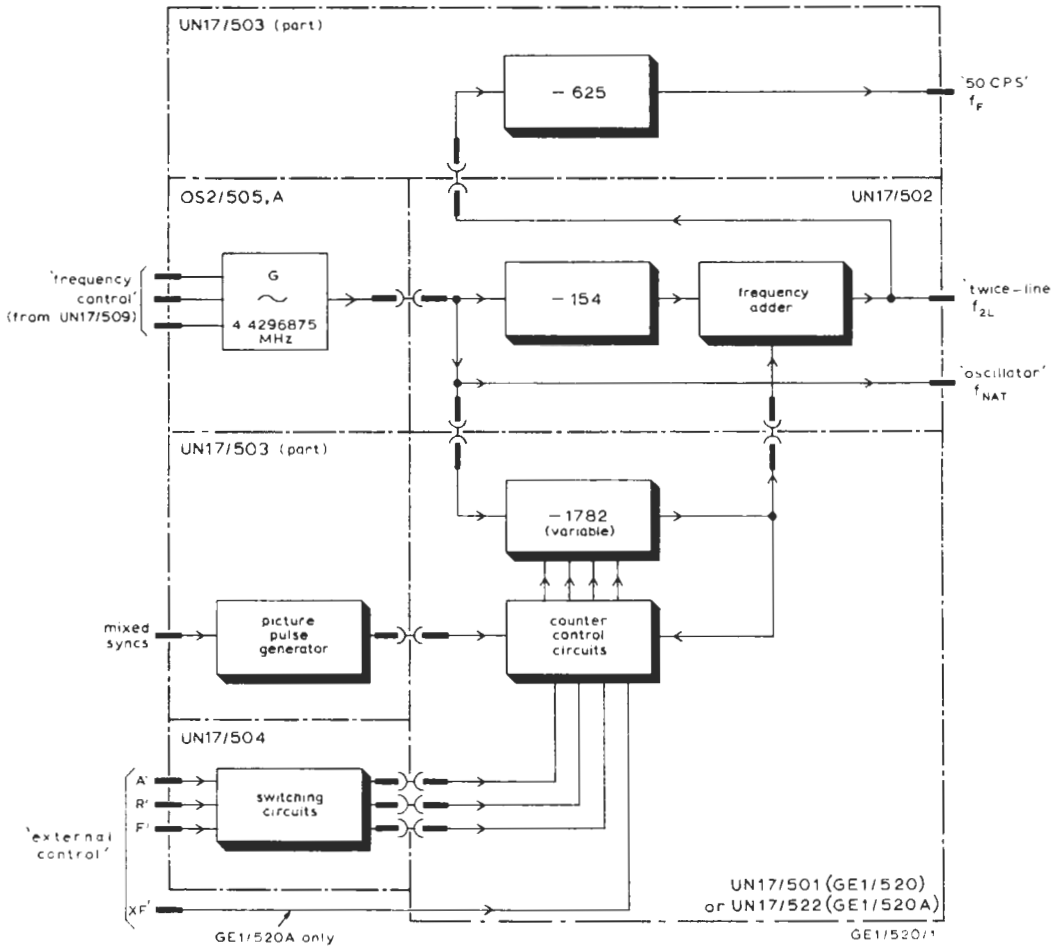

Fig. 1. Simplified Block Diagram of the Drive Units

General Description

A simplified block diagram of the GE1/520 is shown in Fig. 1. The output of the stable crystal oscillator is fed to two counter circuits, one in the Fixed Divider unit and the other in the Variable Divider unit. The output frequencies of these counters are added in a modulator which has an output filter tuned to the sum frequency. The various frequencies, under normal operating conditions, are shown in Table 1.

TABLE 1

Output	*Frequency (f)*	*f as a function of f_0*	*f as a multiple of line frequency*
Oscillator	4·4296875 MHz	f_0	$\frac{3^4 \times 7}{2} \times$ l.f.
÷ 154 Counter	28·7642 kHz	$f_0/154$	$\frac{3^4}{2^2 \times 11} \times$ l.f.
÷ 1782 Variable Counter	2·4858 kHz	$f_0/1782$	$\frac{7}{2^2 \times 11} \times$ l.f.
Filter	31·2500 kHz	$f_0/154 + f_0/1782$	$\frac{81 + 7}{2^2 \times 11} \times$ l.f. $= 2 \times$ l.f.

The ratio of the divide-by-1782 counter is controlled either manually or automatically by the application of error signals derived from an Error Signal Generator[2,3,4]. In both Drive Units the ratio can be changed to divide-by-1778 or divide-by-1786 and this changes the output frequency of the counter by approximately 5·6 Hz. The twice-line frequency output of the Drive Unit changes by the same amount. This change in frequency corresponds to a change in timing of a driven sync pulse-generator of one field in about 112 seconds.

Also in both Drive Units the ratio can be changed to either divide-by-1781 or divide-by-1783 for one of the 99 (approx) counts in each picture period. This method of digital phase control[5] produces a shift **of** approximately 0·2 degrees per picture period. This corresponds to a change in timing of a driven sync pulse-generator of 18 ns per picture period.

In the GE1/520A only, the ratio can also be changed to divide-by-1708 or divide-by-1864 and this changes the output frequency by approximately 108 Hz. The twice-line frequency output of the Drive Unit changes by the same amount. This change in frequency corresponds to a change in timing of a

driven sync pulse-generator of one field in about 6 seconds. Table 2 shows the relation between the modes of operation of the Drive Units, the input signals and the counter ratios in the Variable Divider.

The A' and R' error signals may be fed also to an Oscillator Correction Unit UN17/509 which is used with the Drive Units to correct the oscillator frequency during Advance and Retard modes of operation.

Fig. 2 shows a more detailed block diagram of the GE1/520 and Fig. 3 of the GE1/520A.

Table 2

Mode of Operation	*Counter Ratio*	*Input Signals (V)*			
		A'	R'	F'	$*XF'$
*Extrafast Retard	1864	0	−6	−6	−6
Fast Retard	1786	0	−6	−6	0
Retard	1782 1783 (once a picture)	0	−6	0	0
Normal	1782	0	0	0	0
Advance	1782 1781 (once a picture)	−6	0	0	0
Fast Advance	1778	−6	0	−6	0
*Extrafast Advance	1708	−6	0	−6	−6

*Applicable only to GE1/520A

Test Schedule

The Test Schedule for the Power Supplier PS2/36 is given under that code.

APPARATUS REQUIRED

Avometers Model 8 (two).

Tektronix oscilloscope Type 533A with Type H plug-in unit.

Video oscillator.

Electronic counter to read 5 MHz with 8-figure readout. (see *Modifications to Test Procedure).*

Extender Unit CH1A/3

12-volt and 24-volt supplies capable of delivering 2 amps.

If an 8-figure electronic counter is not available, the test procedure may be modified (as described later) to omit the steps using the counter and to substitute simple comparisons with Network line-frequency. If such comparisons are made it is necessary to check that Network pulses are being derived from an accurately aligned Drive Unit.

If difficulty is experienced due to the lack of a counter, the Drive Unit should be returned either to Equipment Department or to Calibration Section at Television Centre.

TEST PROCEDURE

(a) Oscillator OS2/505,A

1. Remove units UN17/501 (or UN17/522), UN17/502 and UN17/503.
   Remove the *Oscillator Link* U-link from the rear of the Drive Unit. Connect the input of the electronic counter to the lower *Oscillator Link* coaxial plug and connect the output of the video oscillator to the upper plug.
   Switch on and allow one hour for the Oscillator oven to reach its operating temperature.
2. Vary the internal trimming capacitor with the front panel control (OS2/505A) or with the special tool provided (OS2/505) and measure the range of frequency control available. The range should be 10 to 50 Hz.

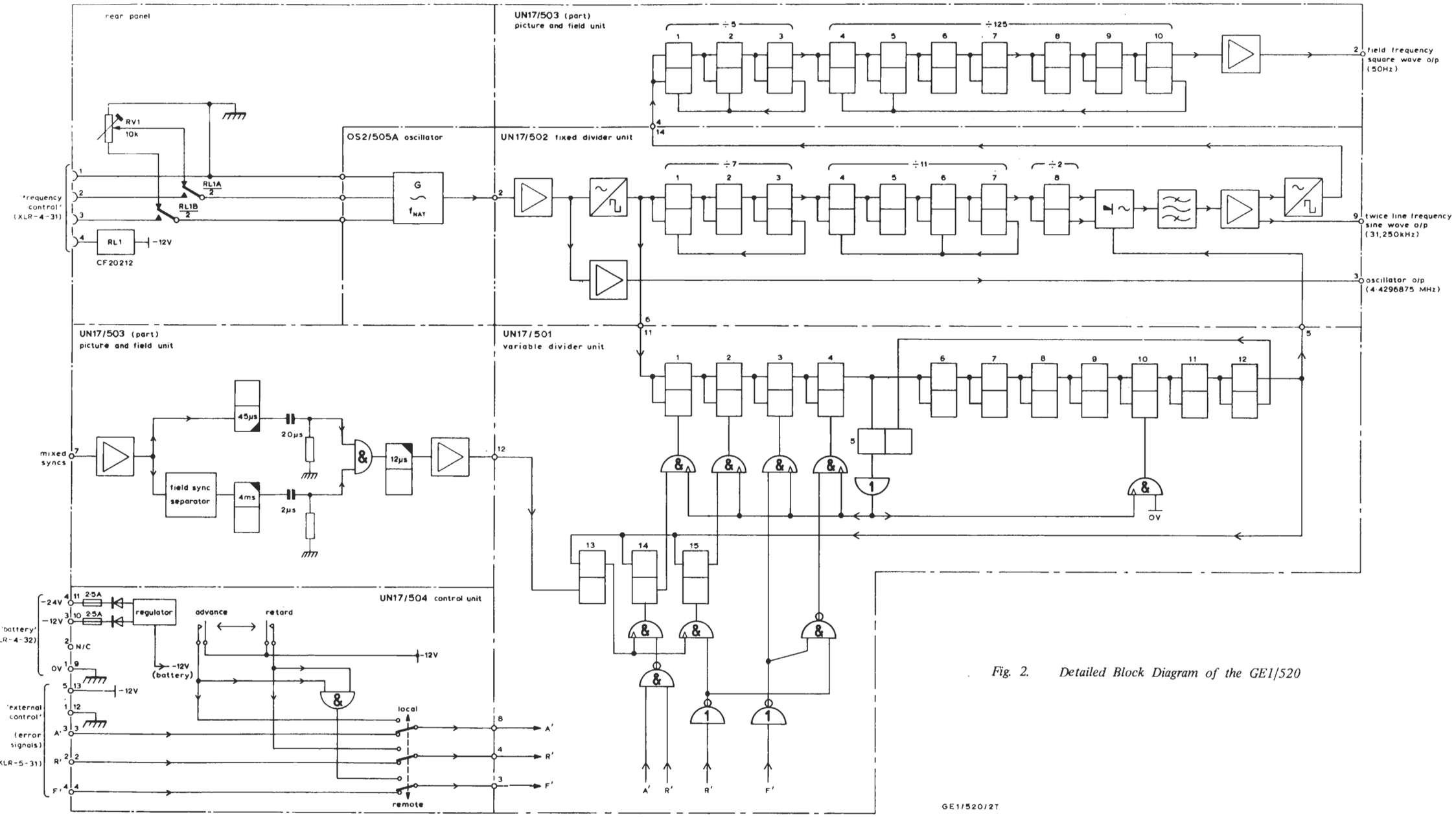

Fig. 2. Detailed Block Diagram of the GE1/520

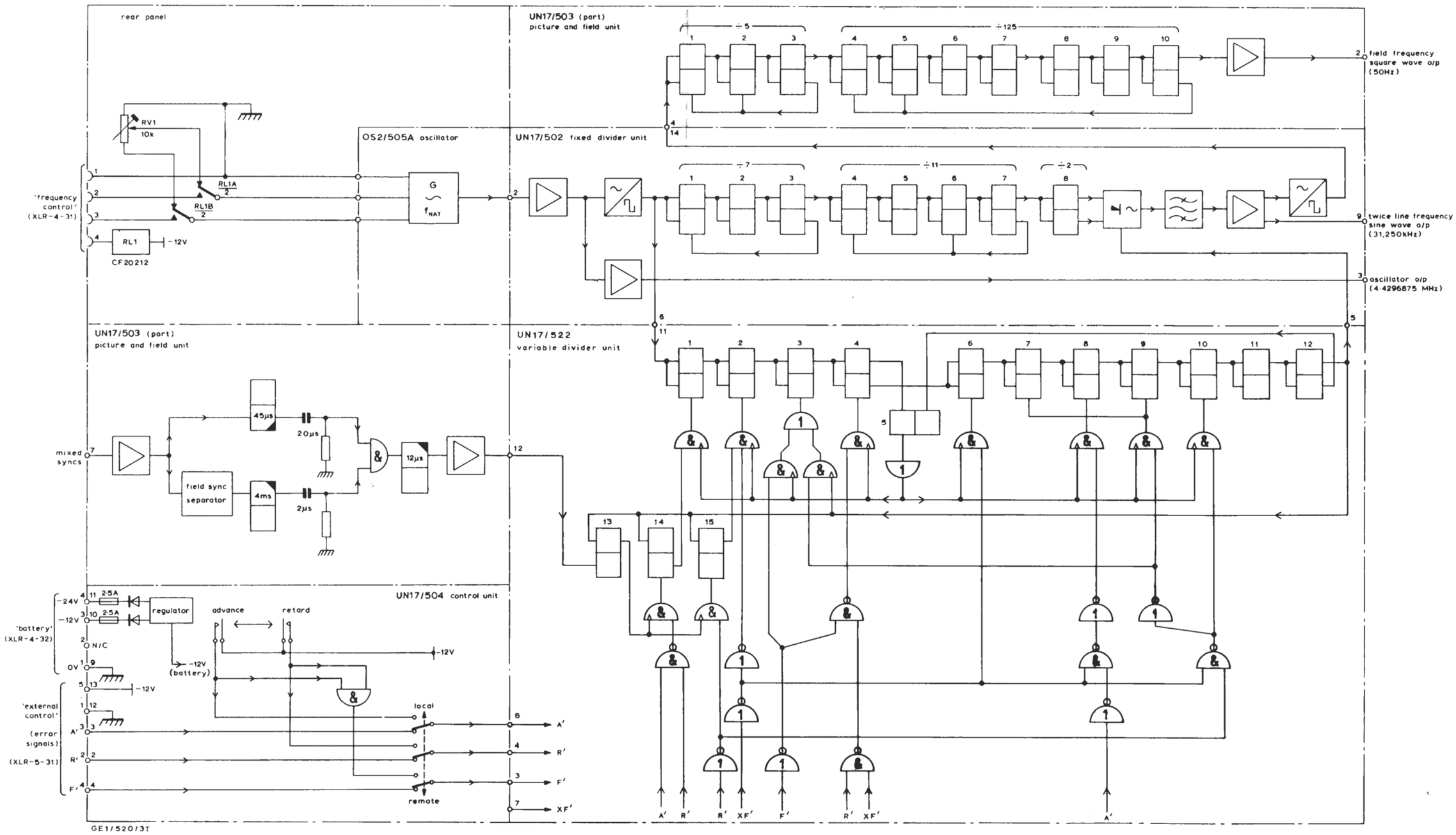

Fig. 3. Detailed Block Diagram of the GE1/520A

At each end of this range vary the rear panel *Frequency Control* and measure the range of control available. These ranges should be 2 to 8 Hz.

3. Set the *Frequency Control* to its mid-point. Adjust the frequency of the oscillator to 4·4296875 MHz using the front-panel control or the internal trainıng capacitor.
   Check that the output voltage of the socillator is not less than 300 mV p-p

(b) Fixed Divider UN17/502

4. Replace the UN17/502 using the Extender Unit. Turn the variable resistor RV2 fully clockwise. Set the output frequency of the video oscillator to 4.5 MHz.
   Adjust the output level of the video oscillator so that 1 volt p-p across 75 ohms is produced at the *Oscillator* output socket at the rear of the Drive Unit. The output level required from the video oscillator should be not greater than 250 mV p-p.
   Remove the video oscillator and electronic counter connections and replace the *Oscillator Link*.
   Adjust resistor RV2 to give 1 volt p-p at the *Oscillator* output socket.
5. Measure the frequencies at the Q terminals of the Bistable Units (see Figs 2. or 3. The correct values are shown in Table 3.

Table 3

Bistable No.	*Frequency (kHz)*	*Period (μs)*
3	632·8125	1·58
7	57·5284	17·38
8	28·7642	34·76

(c) Variable Divider UN17/501 or UN17/522

6. Replace the UN17/501 (or UN17/522) and observe the waveform at pin 6 of the UN17/502. The amplitude of this waveform should be not less than 1·5 volts p-p and the rise time of the positive-going transitions should be not more than 60 ns.
7. Check that the frequency of the signal at pin 5 of the UN17/502 is 2·4858 kHz.
   Turn the *Set Twice-line Level* control RV1 to its midpoint.
   Connect the inputs to the counter and the oscilloscope to pin 9 of the UN17/502 and terminate the *Twice Line* socket at the rear of the Drive Unit in 75 ohms.
   Check that the frequency at this point is 31·250 kHz.
   Adjust the cores of the inductors L1 to L5 successively for maximum output.
   Adjust the *Set Twice-line Level* control to give an output of 1 volt p-p. Increase the gain of the oscilloscope and, using the vertical shift control, explore the whole of the twice-line frequency waveform for crosstalk signals; these should have an amplitude less than 2 mV p-p.

(d) Picture and Field Unit UN17/503

8. Replace the UN17/502 in position and plug in the UN17/503 using the Extender Unit.
   Connect a 75-ohm termination to the *50 C.P.S.* socket at the rear of the Drive Unit and connect the oscilloscope and counter inputs to pin 2 of the UN17/503.
   The frequency at this point should be 50 Hz and the waveform should be a square wave with an amplitude not less than 2 volts p-p.
9. Connect a feed of mixed sync-pulses to the *Mixed Sync* socket at the rear of the drive Unit and observe the waveforms at pins R and X on the UN17/503.
   The waveform at pin R should be a positive-going field-frequency pulse with an amplitude of 6 volts and a duration of 750 μs. The leading edge of this pulse should coincide with the leading edge of the second broad pulse.
   The waveform at pin X should be a negative-going line-frequency pulse with an amplitude of 4 volts and a duration of 18 μs. The leading edge of this pulse should have an exponential shape.
   Disconnect the feed of mixed sync-pulses.

(e) General

10. Transfer the Extender Unit from the UN17/503 to the UN17/501.
    Trigger the oscilloscope from the output of Bistable Unit No. 12 in the UN17/501 and check that Bistable UNits Nos. 2, 4 and 10 are reset by the feedback pulse.
11. Connect the terminated input of the counter to the *Twice-line* socket at the rear of the Drive Unit.
    Switch to *Remote* on the UN17/504.
    Simulate a Fast Advance input signal by connecting pins 3 and 4 of the *External Control* socket to a source of −6 volts.
    Check that Bistable Units Nos. 2, 3, 4 and 10 are reset by the feedback pulse
    Check that the *Twice-line* frequency is 31·2556 kHz.
    Switch to *Local* and *Advance* on the UN17/504.
    Check that Bistable Units Nos. 2, 3, 4 and 10 are reset by the feedback pulse.
    Check that the *Twice-line* frequency is 31·2556 kHz.
12. Simulate a Fast Retard signal by connecting pins 2 and 4 on the *External Control* socket to a source of −6 volts.
    Switch to *Remote* on the UN17/504.

Check that Bistable Units Nos. 2, 3 and 10 are reset by the feedback pulse.
Check that the *Twice-line* frequency is 31·2444 kHz.
Switch to *Local* and *Retard* on the UN17/504.
Check that Bistable Units Nos. 2, 3 and 10 are reset by the feedback pulse.
Check that the *Twice-line* frequency is 31·2444 kHz.

13. (GE1/520A only) Simulate an Extrafast Advance signal by connecting pins 3, 4 and 6 on the *External Control* socket to a source of −6 volts.
Switch to *Remote* on the UN17/504.
Check that Bistable Units 3, 6, 8 and 10 are reset by the feedback pulse.
Check that *Twice-line* frequency is 31·3577 kHz.
14. (GE1/520A only) Simulate an Extrafast Retard signal by connecting pins 2, 4 and 6 on the *External Control* socket to a source of −6 volts.
Switch to *Remote* on the UN17/504.
Check that Bistable Units 3, 6, 7, 8 and 9 are reset by the feedback pulse generated 16 input-pulse periods after the Variable Divider output goes negative, and that Bistable Unit 3 is reset again when the Variable Divider output goes positive.
Check that *Twice-line* frequency is 31·1407 kHz;
15. Reconnect the feed of mixed sync-pulse.
Observe the waveform at pin 12 on the UN17/501 (or UN17/522) which should be a positive-going picture-frequency pulse with an amplitude of not less than 7·5 volts and a duration of not more than 9 μs.
Observe the waveform at one of the outputs of Bistable Unit No. 13 while triggering the oscilloscope from pin 12. This waveform is a pulse at picture-frequency and with a variable duration which does not exceed 402·2 μs.
16. Trigger the oscilloscope from the Q1 terminal of Bistable Unit No. 13. Observe the waveform at the Q1 terminal of Bistable Unit No. 5. Adjust the horizontal shift of the oscilloscope to keep the positive-going edge of the waveform in the centre of the display and expand the trace by *X 50.*
Remove the connections to the *External Control* socket.
Connect the probe of the oscilloscope to the Q1 terminal of Bistable Unit No. 1.
Apply −6 volts to pins 2 and 3 in turn of the *External Control* socket. Check that in each instance the positive-going edges of the waveform after the feedback pulse advance to the left of the tube face by 226 ns which is half the period of the waveform. This effect can best be observed by watching the first positive-going edge after the feedback pulse.
17. Transfer the probe of the oscilloscope to the Q1 terminal of Bistable Unit No. 2.
Apply −6 volts to pin 3 of the *External Control* socket.
The positive-going edges of the waveform after the feedback pulse should be retarded toward the right of the trace of 226 ns.

Modifications to Test Procedure

If an 8-figure electronic counter is not available omit the frequency measurements in steps 2, 3, 5, 7, 11 and 12 of the Test Procedure.

Use the twice-line frequency output of the Drive Unit under test to drive a sync pulse-generator. Feed the mixed sync-pulses from the driven generator to the sync input of a picture monitor switched to external syncs. Feed the video input of the picture monitor with a signal derived from a known accurately aligned Drive Unit. Some Network signals may be suitable.

Adjust the frequency of the Oscillator OS2/505, as in step 5, to produce a stationary picture. Check that the rate of drift is less than one line in 320 seconds.

Apply simulated error signals and mixed sync-pulses to the Drive Unit and measure the relative drifts. Table 4 gives the relative rates of drift in the various operating modes.

Table 4

Mode of operation	*Drift Rate*
Fast retard	One field upwards in 112 seconds
Retard	One line from right to left in 142 seconds
Normal	Zero
Advance	One line from left to right in 142 seconds
Fast advance	One field downwards in 112 seconds.

Table 5 shows the rates of drift in the Retard and Advance modes after correction has been made for the effect of inaccurate timing of the oscillator.

Table 5

Drift rate (seconds per line)	
in normal operating mode	*in Advance and Retard operating modes*
320	98·5 and 255
400	105 and 220
500	110 and 198
600	115 and 186
800	120 and 173
1000	124 and 166
∞	142 and 142

Further Information

The warm-up time may be shortened by monitoring the crystal oven current. This varies between about 1·2 amps (cold) and about 220 mA (hot). The 24-volt battery regulator circuit consumes about 30 mA unloaded and its output voltage varies between about 9 volts (cold) and 12 volts (hot).

References

1. *Picture Source Synchronising;* Instruction P.1
2. Error Signal Generator (PAL) GE1L/532
3. Error Signal Generator (PAL) Four-way GE1M/540
4. Error Signal Generator (Genlock) GE1M/568
5. *Digital Methods of Controlling Frequency and Phase;* Instruction GP.3

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