WAVEFORM GENERATOR DRIVE UNITS
GE1L/537 and GE1L/537A

Introduction

The Drive Units GE1L/537 and GE1L/537A form part of the Natlock system as installed in Common Clock[1] areas. They are used to provide a twice-line frequency signal for a sync-pulse generator from an external feed of Natlock reference frequency signal.

Each Drive Unit accepts signal feeds of Natlock reference frequency, local and reference 12·5-Hz squarewaves (related to PAL-picture phase) and Natlock tone error signal. The units operate in one of two automatically selected modes:

- When all signal inputs are present the *Decoder* mode is selected and provides a single feed of twice-line frequency which is fully controlled in both frequency and phase by error control signals A', R', and F' decoded from the Natlock tone error signal. These error signals are provided as outputs together with the decoded colour error control signal C'.
- When Natlock tone error signal is not connected the *Comparator* mode is selected to provide a twice-line frequency signal controlled only in frequency by *Fast* error control signals generated in the unit by comparison of the 12·5-Hz squarewaves. These error signals are provided as outputs but the colour error signal C' is not.

In addition, as an alternative to these modes, the GE1L/537A can accept externally-switched error control signals A'_g, R'_g, F'_g and XF' from a genlock error signal generator[2] to provide fast-genlock operation[3].

The Drive Units require an external mains supply and comprise the following four units mounted from left to right in a PN3A/13E rear-interconnection panel:

Power Supplier	PS2/13F
Fixed Divider Unit	UN17/502
Variable Divider Unit (GE1L/537)	UN17/501
or Variable Divider Unit, Genlock (GE1L/537A)	UN17/522
Tone Decoder and Pulse Comparator Unit	UN17/518

A PN3A/23 chassis guide and screen should be mounted between the Power Supplier and Fixed Divider Unit.

The front panel of the UN17/518 carries four lamps:

Routed	(green)	a *Tone* line is connected to the Drive Unit
Tone	(green)	Tone is present on the line
Time Error	(amber)	A' or R' error control signals are being detected within the UN17/518
Colour Error	(amber)	C'

General Specification

Signal Inputs (can be reduced by 6 dB)

Natlock reference frequency (4·429 687 5 MHz, nominal)	1 V p-p
Local 12·5-Hz squarewave	1 V p-p
Reference 12·5-Hz square	1 V p-p
Natlock tone error signal	0 dB (w.r.t. 1 mW into 600 ohms)

Imput Impedances

Natlock reference frequency	about 1 kilohm
Local 12·5-Hz squarewave	75 ohms
Reference 12·5-Hz squarewave	about 1 kilohm
Natlock tone error signal	600 ohms, balanced

Signal Outputs

Twice-line frequency (31 250 Hz nominal)	1 V p-p
Error control signals (Table 1 gives voltage tolerances)	
a) A', R', F' (binary logic)	0 V and −6 V (nominal
b) C' (tenary logic	0 V, −3 V and −6 V (nominal)

Table 1

Nominal Voltage(V)	*Actual Voltages (V)*	
	binary logic	*ternary logic*
0	more +ve than −1·5	more +ve tnan −1·5
−3	–	from −2·5 to −3·25
−6	more −ve than −4·5	more −ve than −4·5

Output Impedance
Twice-line frequency 75 ohms

Power Input 200 to 250 V a.c., fused at 150 mA on PS/13F

Ambient Temperature Range 0°C to 45°C

Weight 4.5 kg

Connectors

Pulses	coaxial, BNC 50-ohm sockets
Monitor	4-mm sockets
Error Output	Painton series 159, 11-pole socket and free plug
Tone Line Input	Cannon XLR-3-32 plug
Mains	Cannon XLR-LNE-32

General Description

A block diagram of the Drive Units is given in Fig. 1

Each Drive Unit provides twice-line frequency controlled in frequency and phase by error control signals A', R' and F' generated within the Drive Unit by either the tone decoder or the timing comparator (both in the UN17/518). These error signals are also made available at a panel connector, together with the decoded colour error signal C'. Thus connection can be made if required to an associated oscillator correction unit[4] and digital phase shifter[5].

Decoder and Comparator Unit UN17/518

The unit can operate in one of two modes. With all signal inputs connected, the centre-tapped earth in the output circuit of the associated tone encoder[6] is detected in the UN17/518 and the Natlock error tone is decoded to provide error control signals A', R', F' and C' corresponding to tone frequency as shown in Table 2. These signals are routed to the *Error Output* socket.

In the GE1L/537 the A', R' and F' signals are normally looped via the free plug to the Variable Divider Unit UN17/501. The colour error signal C' is normally connected to the appropriate digital phase shifter either direct or via an Error Inverter unit[7] for Natlock genlock operation[1]. In the GE1L/537A

Table 2

Tone Frequency (Hz)	*Error Control Function*	*Error Control Signals (V)*				*Lamp Indication**
		F'	A'	R'	C'	
892	fast retard	−6	0	−6	0	time error
977	retard	0	0	−6	0	time error
1071	colour retard	0	0	0	−3	colour error
1173	normal	0	0	0	0	
1285	colour advance	0	0	0	−6	colour error
1407	advance	0	−6	0	0	time error
1542	fast advance	−6	−6	0	0	time error

*Lamp indication is for a continuous tone input.

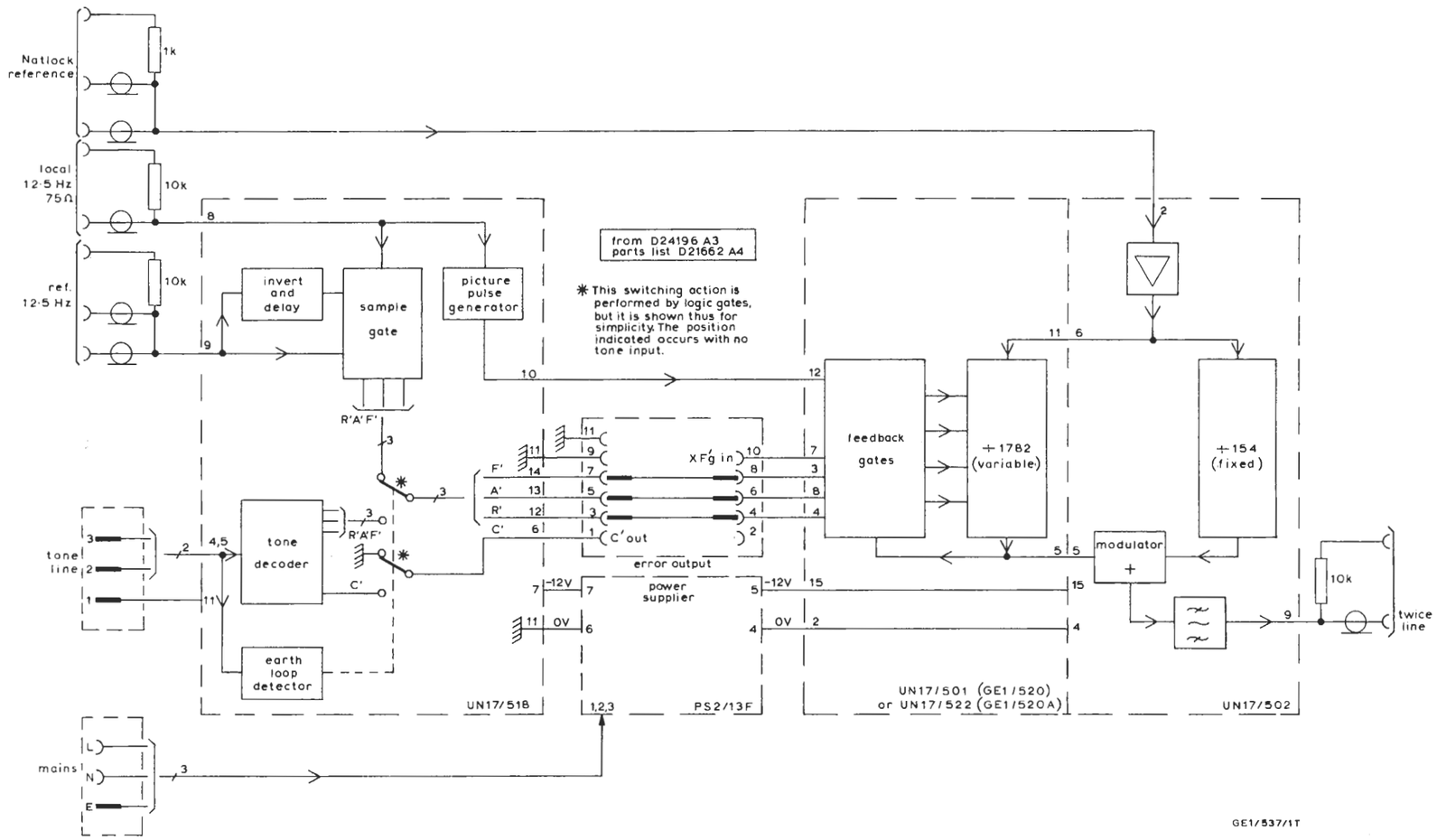

Fig. 1. Block Diagram of the Waveform Generator Drive Units GE1L/537 and GE1L/537A

(when used for fast genlock) the error signals A'_g R_g, F_g and XF_g are generated in the associated genlock error signal generator[2] and routed to the Drive Unit by remote switching to provide manual/automatic control and slavelock/fast-genlock operation.

When the Natlock error tone line is not connected, the earth-loop is not detected and the timing of local and reference 12·5-Hz squarewaves is compared by a sampling gate to provide *Fast* sync-pulse timing error control signals as indicated in Table 3. These signals are routed by logic gates (connected to function as changeover switches) to the *Error Output* socket.

Picture pulses at 25-Hz repetition rate are generated from the local 12·5-Hz squarewave input and passed to the Variable Divider Unit where they are required for correction at *Advance* or *Retard* rates to take place

Table 3

Relative Squarewave Phase	*Error Control Function*
Local signal leads Reference signal	Fast Retard
Local signal lags Reference signal by less than 20 μs	Normal
Local signal lags Reference signal by more than 20 μs	Fast Advance

Divider Units UN17/501 (or UN17/522) and UN17/502

Natlock reference frequency is fed to two counter circuits, one in the Fixed Divider and one in the Variable Divider. The outputs from these counters are combined in a modulator which has an output filter tuned to the sum frequency of 31 250 Hz (twice-line frequency).

In both Drive Units the ratio of the divide-by-1782 counter in the Variable Divider is determined by the combination of error control signals from the UN17/518 and can be changed to divide-by 1778 or divide-by-1786 to give a shift of ±5·6 Hz in the twice-line frequency. This corresponds to a change in timing of the associated sync-pulse generator of one field in about 112 seconds.

Also in both Drive Units the ratio can be changed to either divide-by-1781 or divide-by-1783 for one of the 99 (approx) counts in each picture period of gating the counter with picture-frequency pulses generated in the UN17/518. This method of digital phase control (see Instruction GP.3) produces a change in timing of the associated sync-pulse generator of about 18 ns per picture period.

In the GE1L/537A only the ratio can also be changed to divide-by-1708 or divide-by-1864 and this changes the output frequency of the Variable Divider by approximately ±108 Hz. The twice-line frequency output of the Drive Unit changes by the same amount.

Continued overleaf

This change in frequency corresponds to a change in timing of a driven sync-pulse generator of one field in about 6 seconds. Table 4 shows the relation between the modes of operation of the Drive Units, the input signals and the counter ratios in the Variable Divider.

If the alignment is suspected:
Adjust the cores of L1 to L5 successively for maximum twice-line output, then readjust RV1 to give 1 V p-p output.

6. The Variable Divider output (pin 5) should have the frequency 2·486 kHz. If a fault is

Table 4

Error Control Function	*Applied Voltage to Error Output socket*				*Twice Line Output*		
	R' pin 4	*A' pin 6*	*F' pin 8*	**XF' pin 10*	*f (kHz)*	*τ (μs)*	*Feedback pulse gated to bistables*
Fast Advance	0	−6	−6	0	31·255 6	31·994 3	2, 3, 4, 10
Fast Retard	−6	0	−6	0	31·244 4	32·005 7	2, 3, 10
*Extrafast Advance	0	−6	−6	−6	31·355 7	31·890 1	3, 6, 8, 10
*Extrafast Retard	−6	0	−6	−6	31·140 7	32·112 4	3 (twice), 6, 7, 9

* A-version only

Maintenance

(a) Power Supplies

1. Adjust the output voltage from each board of the PS2/13F to be 12·0 V.

(b) Fixed Divider Input

2. Monitor the *Natlock Osc* signal on the UN17/502 front panel using a high-impedance probe: the signal should be a 1-V p-p sinewave of nominal frequency 4·429 687 5 MHz.

(c) Normal Operation

3. Remove the *Error Output* connector.
Monitor the *Twice Line Output* signal on the rear panel: it should be a 1-V p-p sinewave of 31 250 Hz. Output amplitude is adjusted by RV1 in the UN17/502.
If the output frequency is incorrect check the Fixed and Variable Dividers:
4. The Natlock reference signal which drives both divider chains should have an amplitude (at pin 6 of the UN17/502) greater than 1·5 V p-p and a positive-transition rise time of less than 60 ns.
5. The Fixed Divider chain output from bistable 8 in the UN17/502 should have the frequency 28·764 2 kHz. Intermediate frequencies are listed in Table 5.

suspected:
Trigger the oscilloscope from the output of bistable 12 and check that bistables 2, 4 and 10 are reset by the feedback pulse from bistable 12.

(d) Controlled Operation

7. Remove the *Error Output* plug (if it has not already been removed in section 3). Use pin 9 of the socket as common and apply −6 V to pins 4, 6, 8 and 10 to simulate the error signals usually provided either by the UN17/518 or by a genlock error signal generator[2].

Table 5

Bistable	*Q Output*	
	Frequency (kHz)	*Period (μs)*
3	632·812 5	1·58
7	57·528 4	17·38
8	28·764 2	34·76

8. For the *Fast* and *Extrafast* modes (as applicable to the two versions) check that when the error signals are applied the twice-line frequency changes to the values listed in Table 5.
9 For *Advance* and *Retard* modes the Variable Divider ratio is changed by a count of one after each picture pulse time. (Picture pulses are generated in the UN17/518 from both edges of local 12·5-Hz squarewave.)
Check that 8-μs positive-going picture pulses of about 4·5 V p-p appear at pin 12 of the Variable Divider.
10. Observe the waveform at a Q output of bistable 13 in the Variable Divider while triggering the oscilloscope from pin 12. The waveform is a pulse at picture frequency and with a variable duration which does not exceed 402·2 μs.
11. Trigger the oscilloscope from the Q_1 pin of bistable 13. Observe the waveform at the Q_1 pin of bistable 5. Adjust the horizontal shift of the oscilloscope to keep the positive-going edge of the waveform in the centre of the display and expand the trace by *X 50.*
Without adjusting any controls connect the oscilloscope probe to the Q_1 output of bistable F. Apply first an *A'* then an *R'* error control signal. Check that in both cases the positive-going edges of the waveform after the feedback pulse advance to the left of the tube face by 226 ns (half the period of the waveform). This effect can best be observed by watching the first positive-going edge after the feedback pulse.
12. Transfer the probe to the Q_1 output of bistable 2. Apply −6 V to pin 6 of the *Error Output* socket to give *Advance* correction. The positive-going edges of the waveform after the feedback pulse should advance towards the left of the tube face by 226 ns (one quarter of the period of the waveform).
Apply −6V to pin 4 of the *Error Output* socket to give *Retard* correction.
The positive-going edges of the waveform after the feedback pulse should be retarded towards the right of the tube face by 226 ns.

(e) Decoder and Comparator

13. To check the *Comparator* mode move the *Tone Line Input* connector, plug in the *Error Output* connector as supplied with shorting links.
Check that the error control functions shown in Table 4 are obeyed for the given relative phase relationships of local and remote 12·5-Hz squarewave. Check that pin 1 of the *Error Output* socket stays at 0 V throughout this test.
14. Connect the output of the EP14L/503 Tone Test Equipment to the *Tone Line Input.* Do not apply mains to the EP14L/503 yet. Observe that the *Routed* lamp lights. Apply mains and check that the *Tone* lamp lights.
15. Select the frequencies listed in Table 2 (page 2) and check that the corresponding lamp indication and error control function are as given.
16. Select 1173 Hz and check that the *Twice-line Output* signal is 31 250 Hz for all states of relative squarewave phase.

References

1. *Picture Source Synchronising;* Instruction P.1, Section 3
2. Error Signal Generator (Genlock) GE1M/568
3. *op.cit.,* Section 4
4. Oscillator Correction Unit UN17/509
5. Colour Subcarrier Phase Shifter EP1L/509
6. Tone Encoder CD2/501
7. Error Inverter UN23/511

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