INSERTION PULSE GENERATOR GE2/585 AND GE2/585A

Introduction

The GE2/585 accepts a four-volt input of mixed sync pulses and provides the following outputs:

(a) Negative-going 10-μs trigger pulses on lines 12, 16, 19, 20, 325, 329, 332 and 333. The leading edge of each trigger pulse is coincident with the leading edge of the line sync pulse.

(b) Odd and even field identification signals which take the form of earth or positive d.c. potentials. The signals are not suitable for use during the equalising pulse periods before and after the field sync broad pulses.

(c) So-called dummy sync pulses each corresponding to a sync pulse 10 μs in duration.

The GE2/585A incorporates a UN16/518A sync pulse separator. The generator accepts a composite video signal and, in addition to the outputs listed previously, produces 2-μs clamp pulses timed to occur in the back porch period.

The generator operates satisfactorily in the presence of sound-in-syncs information. It is built on a CH1/12A chassis with index pegs in positions 1, 3 and 7.

Brief Specification

Input

GE2/585	4 volts p-p from 75-ohm unterminated source or 5 volts p-p from a DTL or TTL output.
GE2/585A	Composite 625-line video signal.

Outputs

Trigger pulses	5 volts amplitude, 10 ±0·1 μs duration.
Logic fan-out	24
Field identification signal level	0 or +5 volts
Logic fan-out	10
Dummy sync pulses	5 volts amplitude, 10 ±0·2 μs duration.
Clamp pulses	12 ±1 volts amplitude, 3 ±1 μs duration.

Logic Potentials

Logic 0: input	1·1 volts maximum.
output	0·4 volt maximum
Logic 1: input	2 volts minimum
output	2·6 volts minimum.

Power Requirements

GE2/585	+6 volts 130 mA.
GE2/585A	+6 volts 175 mA, +12 volts 93 mA.

Continued overleaf

Circuit Description (Figs. 1 to 3)

Fig. 1 is a circuit diagram of the GE2/585 and GE2/585A; Fig. 2 is a drawing of idealised waveforms. The letters (in parentheses) on the circuit diagram refer to the waveforms in Fig. 2.

In the GE2/585 mixed sync pulses (a) are applied to pin PLA6 and passed via inverter-buffer gates IC1a/4 and IC1b/4 to a monostable circuit IC2. The monostable is triggered by the negative-going edges of the sync pulse waveform and 10-μs pulses (b) are generated. The output from circuit IC2 is passed via two inverting gates to pin PLA8. The pulses at this point are known as dummy sync pulses.

The output of gate IC13a/2, positive-going dummy-sync-pulses, is used to trigger a monostable circuit IC3. A train of 40-μs pulses (c) is presented to a two-input NAND-gate IC1d/4. The other input to this gate is a feed of positive-going dummy-sync-pulses. The output of the gate (d) is a train of seven or eight pulses, once per field, the leading edges being coincident with alternate equalising pulses.

Pulses (d) are fed to monostable circuit IC4. The negative-going edge of the first pulse triggers the monostable circuit which produces a negative-going pulse (e) 13 lines long. The pulse is inverted in gate IC13b/2 and the negative-going trailing edge of the pulse is used to trigger monostable circuit IC5 which produces a positive-going pulse (f) one line in length. This pulse, together with a feed of positive-going dummy sync pulses is fed to NAND-gate IC6a/2. The output from this gate (g) is a single dummy sync pulse at the start of line 12. On the next, even, field the dummy sync pulse at the commencement of line 325 is generated.

The other line-trigger outputs, which are listed in the Introduction, are produced by similar circuit arrangements.

Circuit IC14 is a JK-bistable which is used to generate odd and even field identification signals. Fig. 3 shows the waveforms concerned. The negative-going edge of the 13-line pulse (e) from the output of IC4 is differentiated (r) by components C2 and R3. This pulse is applied to the S_d terminal of the bistable and sets the Q-output to a logic 1 state. A feed of pulses (d) from gate IC1d/4 is applied to the clock pulse input of IC14 and the outputs change state on every negative-going edge.

The Q and $\bar{Q}$ outputs of IC14 are available at pins PLA12 (s) and PLA20 (q) respectively. At pin PLA12 the odd field is identified by a logic 1 potential and the even field by a logic 0 potential. At pin PLA20 the even field provides a logic 1 output and the odd field a logic 0 output.

Test Schedule

Apparatus Required

Source of 625-line mixed sync pulses
Double-trace oscilloscope

Test Procedure

Note:- More detailed alignment information is given in Designs Department Specifications:
11.74(69) - GE2/585
11.83(69) - GE2/585A

1. Check that the voltage across capacitors C1 and C13 is in each instance 5·2 ±0·2 volts.
2. Check that the current load is 130 ±20 mA (GE2/585 only).
3. Check that the pulse waveform at TP10 is 10 ±0·2 microseconds in duration. Resistor R13 is selected to give this figure. For the GE2/585A the tolerance on pulse duration should be ±0·1 microseconds.
4. Check that the pulse waveform at IC3 pin 6 is 40 ±0·2 microseconds in duration. Resistor R25 is selected to give this figure.
5. Connect the oscilloscope so that the waveforms at PLA6 and TP1 are displayed. The oscilloscope must be triggered by the signal at TP1 otherwise serious errors may occur.
6. Check that the pulse at TP1 is 64 ±2 microseconds in duration. Resistor R15 is selected to achieve this figure.
7. Check that the sync pulse on line 12 and 325, at TP5, is positioned centrally within the pulse at TP1. The trailing edge of the sync pulse should be within ±5 microseconds of the centre of the pulse at TP1. Resistor R4 is selected to achieve this position.
8. Check that only one dummy sync pulse per field appears at TP5.
9. Repeat steps 5 to 8, using the positions and making the adjustments shown in Table 1, to check the other trigger pulses.

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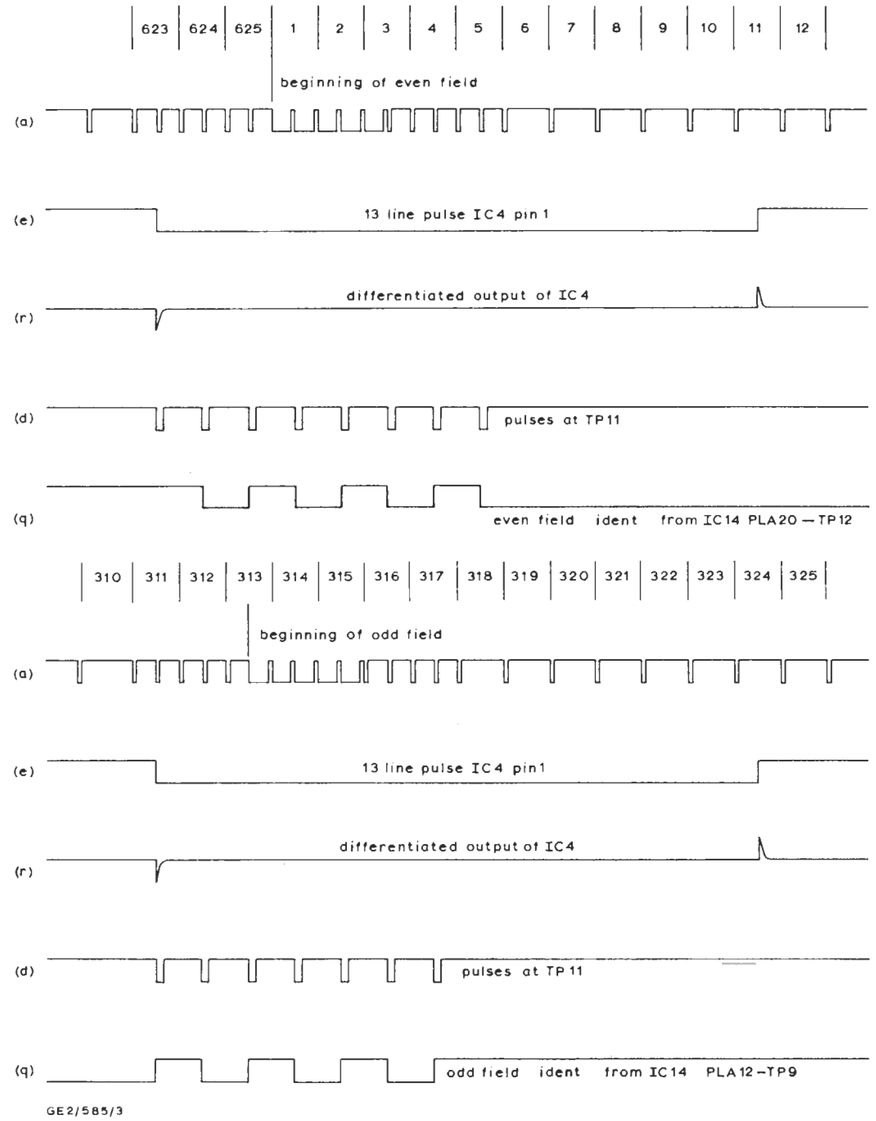
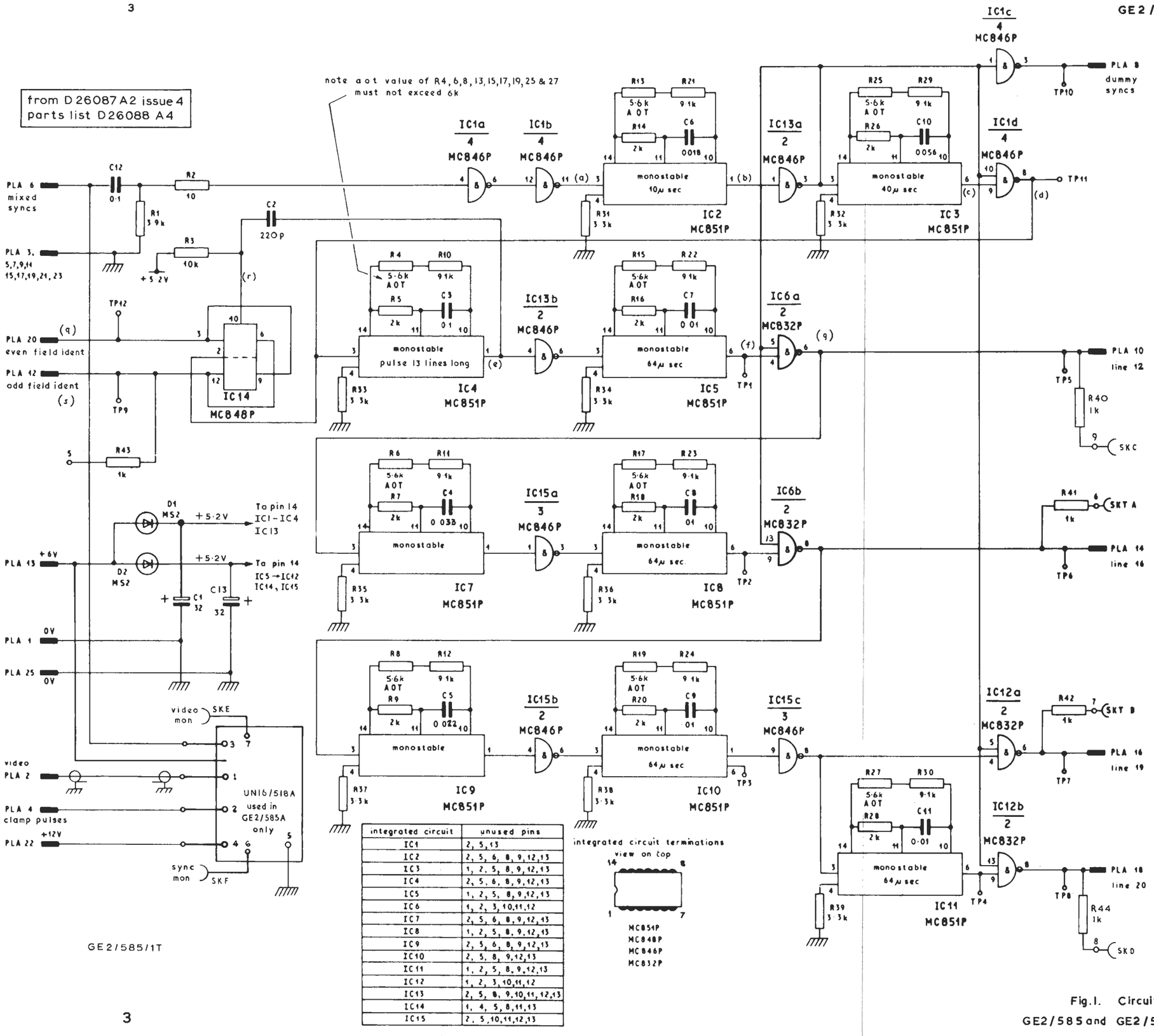


Fig. 3 ***Derivation of Field Ident Signals***

TABLE 1

Monitor point	*Make pulse duration 64 ±2μs by selecting*	*Select*	*As in step 7, check position of pulse on lines*	*Check that only one dummy sync pulse per field appears at*
TP2	R17	R6	16 and 329	TP6
TP3	R19	R8	19 and 332	TP7
TP4	R27		20 and 333	TP8



integrated circuit	unused pins
IC1	2, 5, 13
IC2	2, 5, 6, 8, 9, 12, 13
IC3	1, 2, 5, 8, 9, 12, 13
IC4	2, 5, 6, 8, 9, 12, 13
IC5	1, 2, 5, 8, 9, 12, 13
IC6	1, 2, 3, 10, 11, 12
IC7	2, 5, 6, 8, 9, 12, 13
IC8	1, 2, 5, 8, 9, 12, 13
IC9	2, 5, 6, 8, 9, 12, 13
IC10	2, 5, 8, 9, 12, 13
IC11	1, 2, 5, 8, 9, 12, 13
IC12	1, 2, 3, 10, 11, 12
IC13	2, 5, 8, 9, 10, 11, 12, 13
IC14	1, 4, 5, 8, 11, 13
IC15	2, 5, 10, 11, 12, 13

GE2/585/1T

Fig.1. Circuit of GE2/585 and GE2/585A

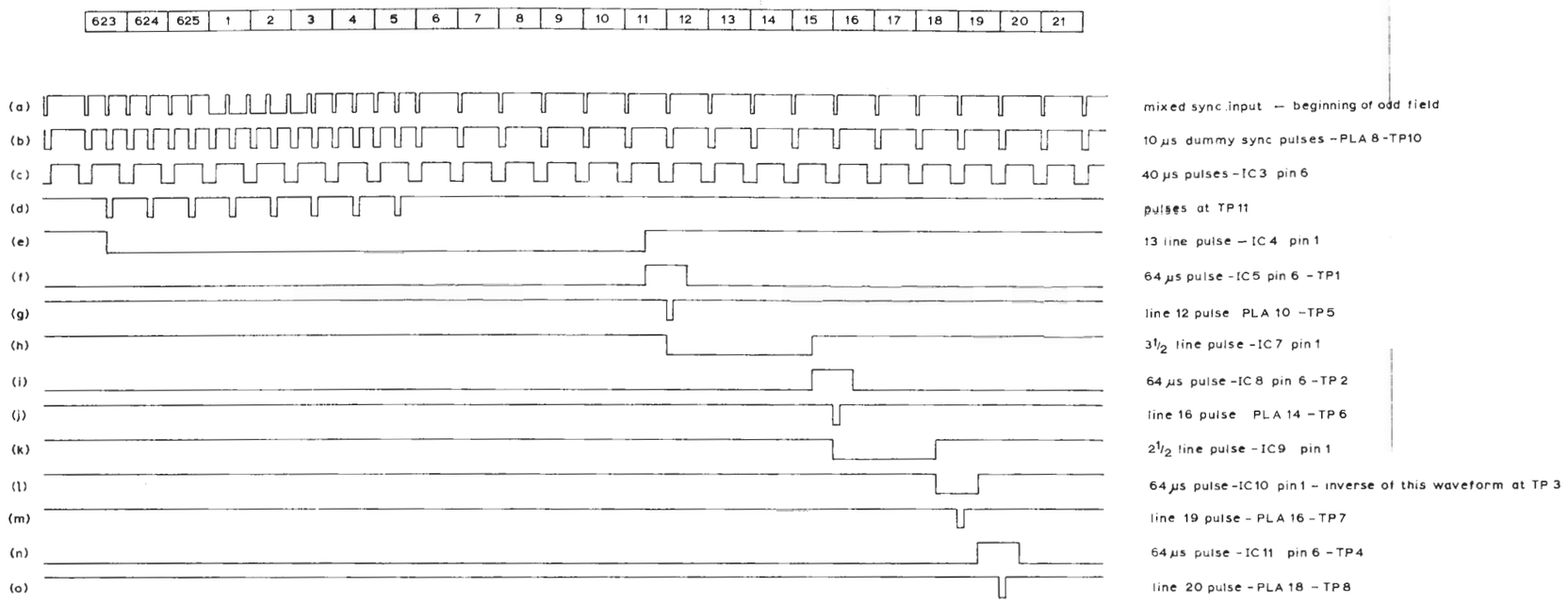


Fig. 2.
Derivation of Dummy Sync and Trigger Pulses