SECTION 25

LUMINANCE NON-LINEARITY TEST SIGNAL GENERATOR GE4/525

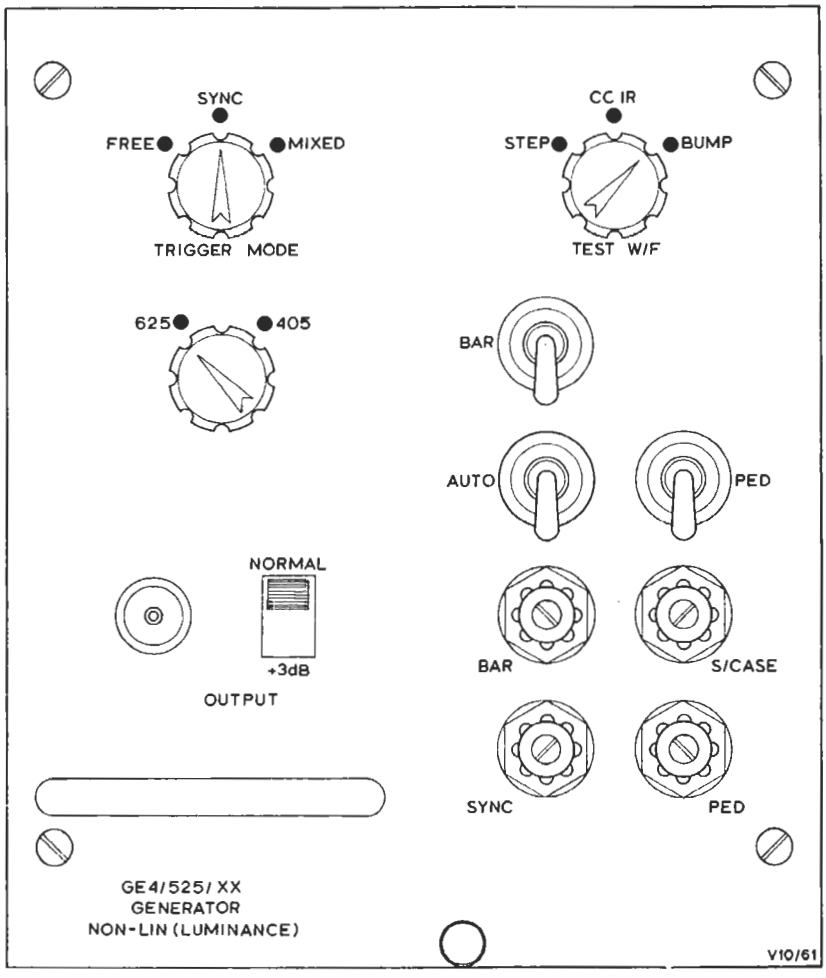

Fig. 25.1 Front Panel of the GE4/525

Introduction

The GE4/525 produces the luminance component of a colour non-linearity test signal and mixes with it an externally-supplied chrominance component. It also produces C.R.O. trigger pulses and drive pulses for a Chrominance Non-linearity Test Signal Generator GE4/526. It can operate on both 405-line and 625-line standards. For synchronising purposes it accepts mixed sync pulses, mixed blanking pulses and burst-gating pulses on both 405-lines and 625-lines.

Facilities

The layout of the controls on the front panel of the GE4/525 is shown in Fig. 25.1.

Trigger Mode Switch

(a) *Free* Not locked to incoming pulses. No field information.

(b) *Sync* Locked to incoming pulses. No field information.
(c) *Mixed* Locked to incoming pulses. Full field information.

Test Waveform Switch
(a) *Step* 5-step staircase on every line.
(b) *CCIR* Staircase on one line in four. All remaining lines either at blanking level or white level.
(c) *Bump* Every line either at blanking level or white level.

Line Standard Switch
(a) *405-lines*
(b) *625-lines*

Bar Switch
(a) *Bar off*
(b) *Bar on* On lines selected by test waveform switch

Auto Switch
(a) *Auto off*
(b) *Auto on* Switches off and on white-level bars automatically at approximately 10-second intervals

Pedestal Switch
(a) *Pedestal off*
(b) *Pedestal on* A pedestal of either polarity only on lines with staircase waveform.

Bar Amplitude
A range of 0·6 volts to 1·0 volts is provided.

Staircase Amplitude
A range of 0·5 volts to 0·8 volts is provided.

Sync Pulse Amplitude
A range of 0·2 volts to 0·4 volts is provided.

Pedestal Amplitude
A range of ±0·5 volts is provided.

Output
The output signal of the GE4/525 appears at a Musa plug on the front panel. A 3-dB attenuator enables overload tests to be carried out.

For further operational details see Instruction V.1, Part 2.

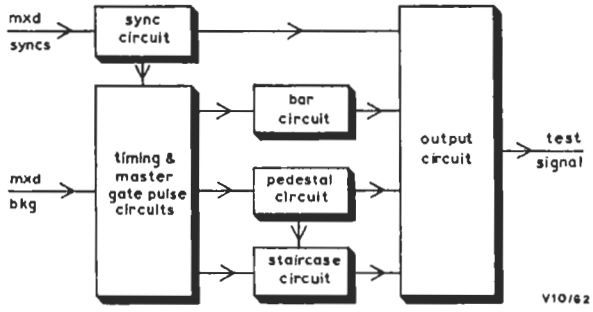

Fig. 25.2 Simplified Block Diagram of the GE4/525

General Description

A simplified block diagram of the GE4/525 is shown in Fig. 25.2. The four components of the output signal (that is sync pulses, bar, pedestal and staircase waveforms) are mixed in the output circuit. The bar, pedestal and staircase circuits are triggered on and off by pulses selected from those fed from timing-and-master-gate-pulse circuits. The sync circuit and the timing-and-master-gate-pulse circuits are driven with mixed sync pulses and mixed blanking pulses.

In the block diagrams shown in Fig. 25.3 to 25.9 the printed wiring board on which each block is located is given as well as the inter-board wiring terminal pin numbers. The numbers in circles refer to waveforms shown in Figs. 25.10 and 25.11.

Sync Pulse Circuit
A block diagram of the sync pulse circuit is shown in Fig. 25.3. In the *Mixed* trigger mode, sync pulses are fed directly to a sync pulse clipper.

In both the *Sync* and *Free* trigger modes the sync-pulse clipper is fed with pulses generated by a monostable multivibrator in a line-sync pulse generator which is triggered by the output of switch SA2.

In the *Sync* trigger mode the input sync pulses are fed to a line-frequency pulse extractor containing a monostable multivibrator. The multivibrator time constant is long enough to prevent double triggering during the field period.

In the *Free* trigger mode line-frequency pulses are generated by an astable multivibrator (line-frequency pulse generator).

In all trigger modes a negative line-sync start pulse is fed to the timing circuit and to the master gate-pulse circuit.

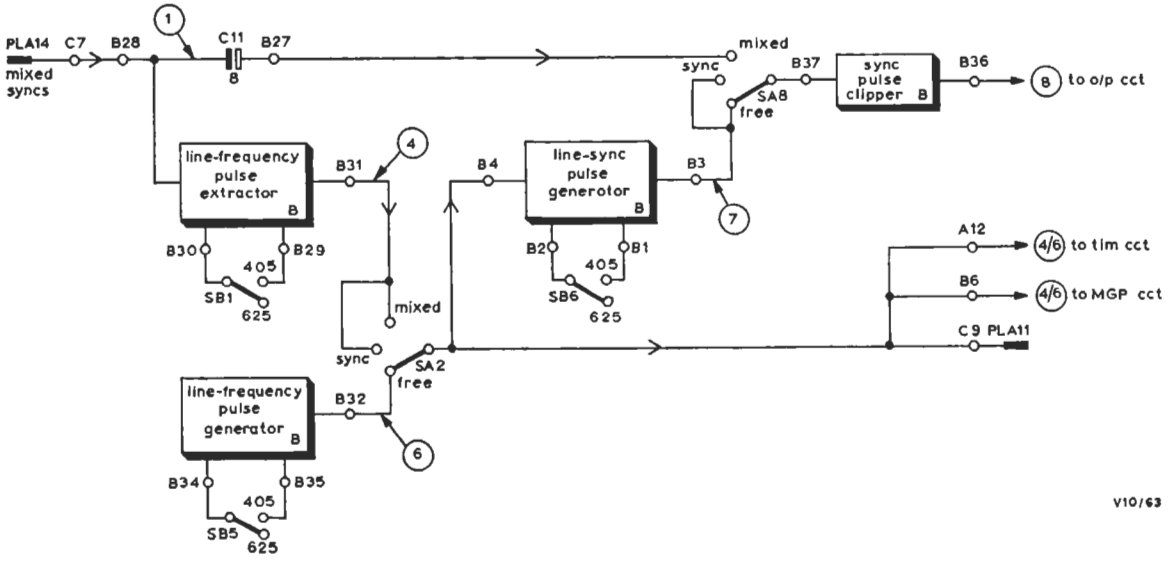

Fig. 25.3 Block Diagram of the Sync Pulse Circuit

Timing and Burst-gating Circuit

A block diagram of the timing and burst-gating circuit is shown in Fig. 25.4. Pulse waveforms used by other circuits requiring inputs with field information are produced by a mixed-mode trigger-pulse generator. These waveforms are used only in the *Mixed* trigger mode.

A modular timing-pulse generator times the transitions in the staircase waveform. It also produces alternatives for three of the outputs of the mixed-mode trigger-pulse generator for use in the *Free* and *Sync* modes.

A burst gating pulse is switched by one pole of the trigger mode switch SA7 used in conjunction with a Chrominance Non-linearity Test Signal Generator GE4/526.

Master Gate Pulse Circuit

A block diagram of the master gate pulse circuit is shown in Fig. 25.5. A monostable multivibrator (divider) has a relaxation time such that it is triggered every fourth line.

The output of this divider is fed to one input of a bistable multivibrator (master gate pulse generator) via switch SC2 (*CCIR* only): the multivibrator is thus triggered on one input at the start of every fourth line. The other input of the bistable is fed from the waveform switch SC1. In the *Step* position of this switch the bistable is inhibited by a d.c. input. In the *CCIR* position the bistable is triggered on every line giving an output pulse of one line duration in every four lines. In the *Bump* position the bistable is triggered only by pulses fed from switch SC1 which maintain the output of the bistable in the opposite state to that for the *Step* position.

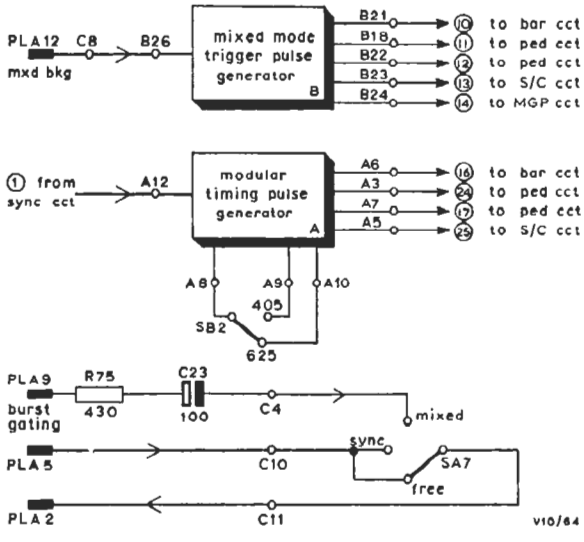

Fig. 25.4 Block Diagram of the Timing and Burst-gating Circuit

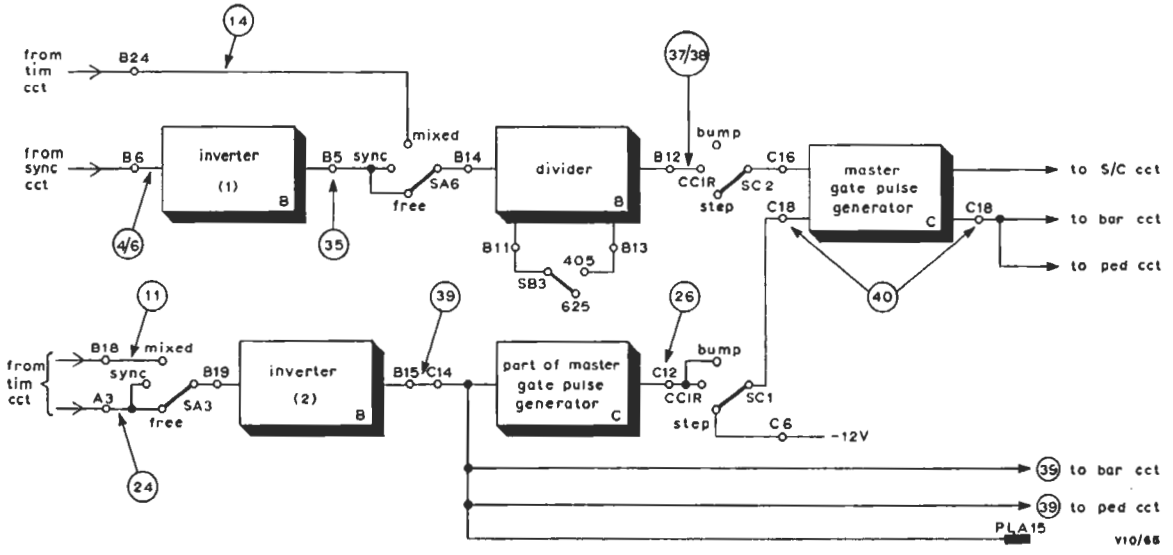

Fig. 25.5 Block Diagram of the Master Gate Pulse Circuit

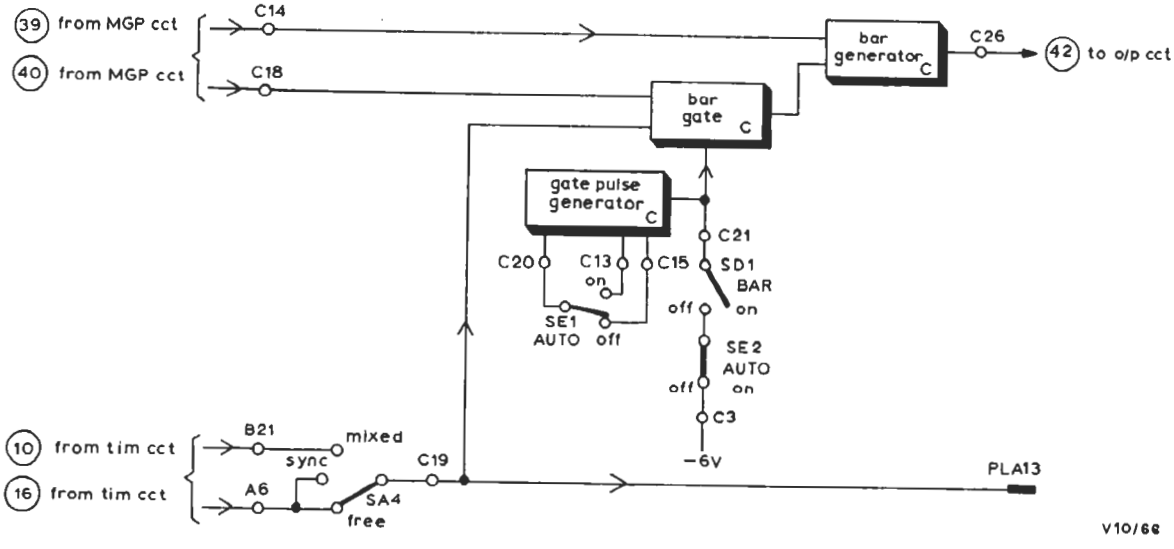

Fig. 25.6 Block Diagram of the Bar Circuit

Bar Circuit

A block diagram of the bar circuit is shown in Fig. 25.6. The bar waveform is produced by a bistable multivibrator (bar generator). The bar is switched on by the output of a bar gate the inputs of which are:

(a) positive-going pulses at the end of each blanking period which time the start of each bar
(b) an output from the master gate-pulse generator which selects bars on no lines, three lines in four or on all lines for the *Step*, *CCIR* and *Bump* waveforms respectively
(c) an output from a bump gate-pulse generator which acts as a master on-off switch for the bar-waveform trigger pulses and which on *Auto* switches these trigger pulses on and off automatically every ten seconds or so.

The bar is switched off by a feed of pulses occurring at the start of each blanking period.

Input (a) of the pedestal gate is fed to the staircase circuit if switch SC3 is in the *Bump* position.

Staircase Circuit

A block diagram of the staircase circuit is shown in Fig. 25.8. The staircase waveform is produced in a staircase generator which is driven by the output of a staircase gate to produce the steps of the waveform and by the output of a reset-pulse generator to form the trailing edge.

The inputs to the staircase gate are:

(a) trains of positive-going pulses which time the steps in the waveform
(b) mixed blanking waveform which cuts off the gate during the field blanking period in the *Mixed* trigger mode
(c) an output of the master gate-pulse generator which selects staircases on all lines, one line in four or on no lines at all for the *Step*, *CCIR* and *Bump* waveforms respectively.

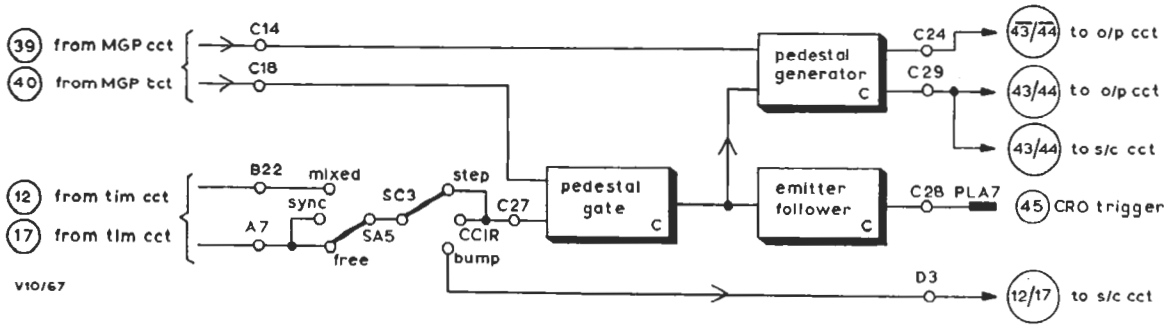

Fig. 25.7 Block Diagram of the Pedestal Circuit

Pedestal Circuit

A block diagram of the pedestal circuit is shown in Fig. 25.7. The pedestal waveform is produced by a bistable multivibrator in a pedestal generator. The pedestal waveform is switched on by the output of a pedestal gate the inputs of which are:

(a) negative-going pulses at the end of each blanking period which time the start of each pedestal
(b) an output from the master gate generator which selects pedestals on all lines, one line in four or on no lines at all for the *Step*, *CCIR* and *Bump* waveforms respectively.

The pedestal is switched off by a feed of pulses occurring at the start of each blanking period.

An output of the pedestal gate is used as a *CRO Trigger* output waveform.

When the staircase generator is not being driven (for the *Bump* waveform) it is supplied with different reset pulses to maintain the d.c. output of the staircase generator.

Output Circuit

A block diagram of the output circuit is shown in Fig. 25.9. The four components of the luminance non-linearity test signal are mixed and amplified in a two stage amplifier. At the output of the amplifier a chrominance test signal is mixed resistively with the luminance signal.

Waveforms

Some of the waveforms to be found in the GE4/525 are given in Figs. 25.10 and 25.11. The waveform reference or the connection for each of the interboard wiring pins is given in Table 1.

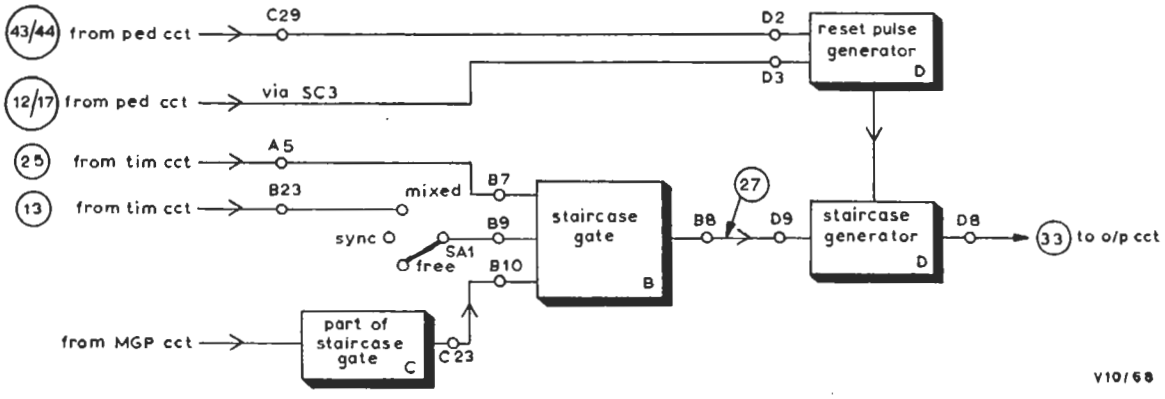

Fig. 25.8 Block Diagram of the Staircase Circuit

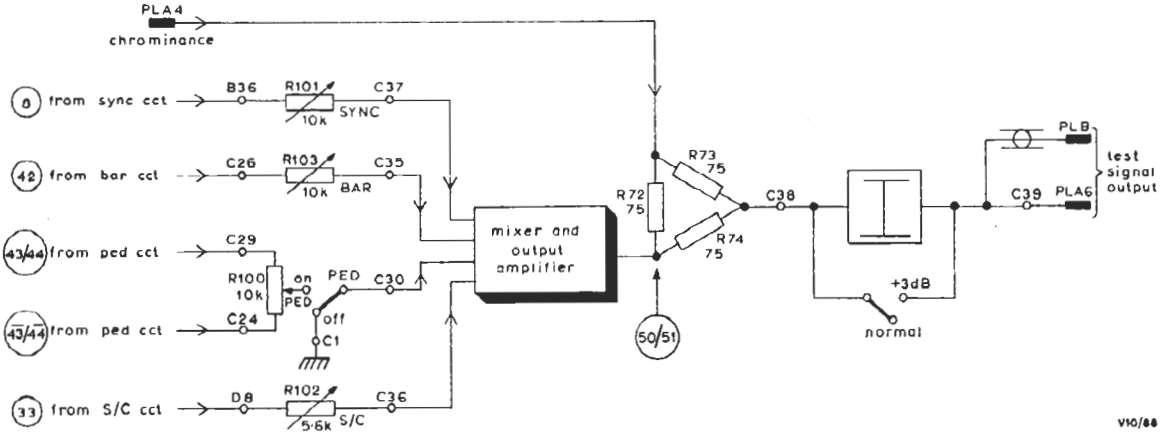

Fig. 25.9 Block Diagram of the Output Circuit

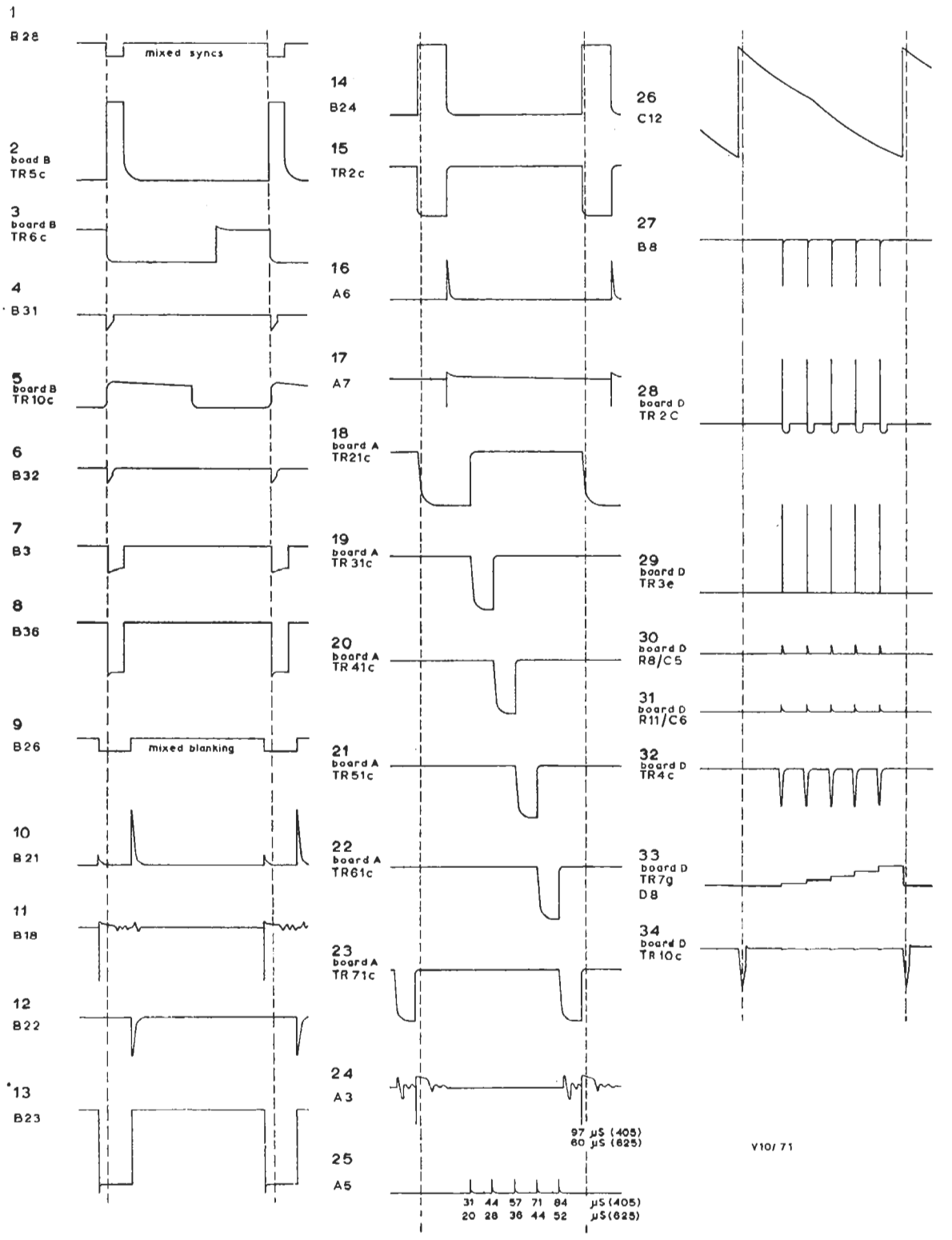

Fig. 25.10 Waveforms in the GE4/525

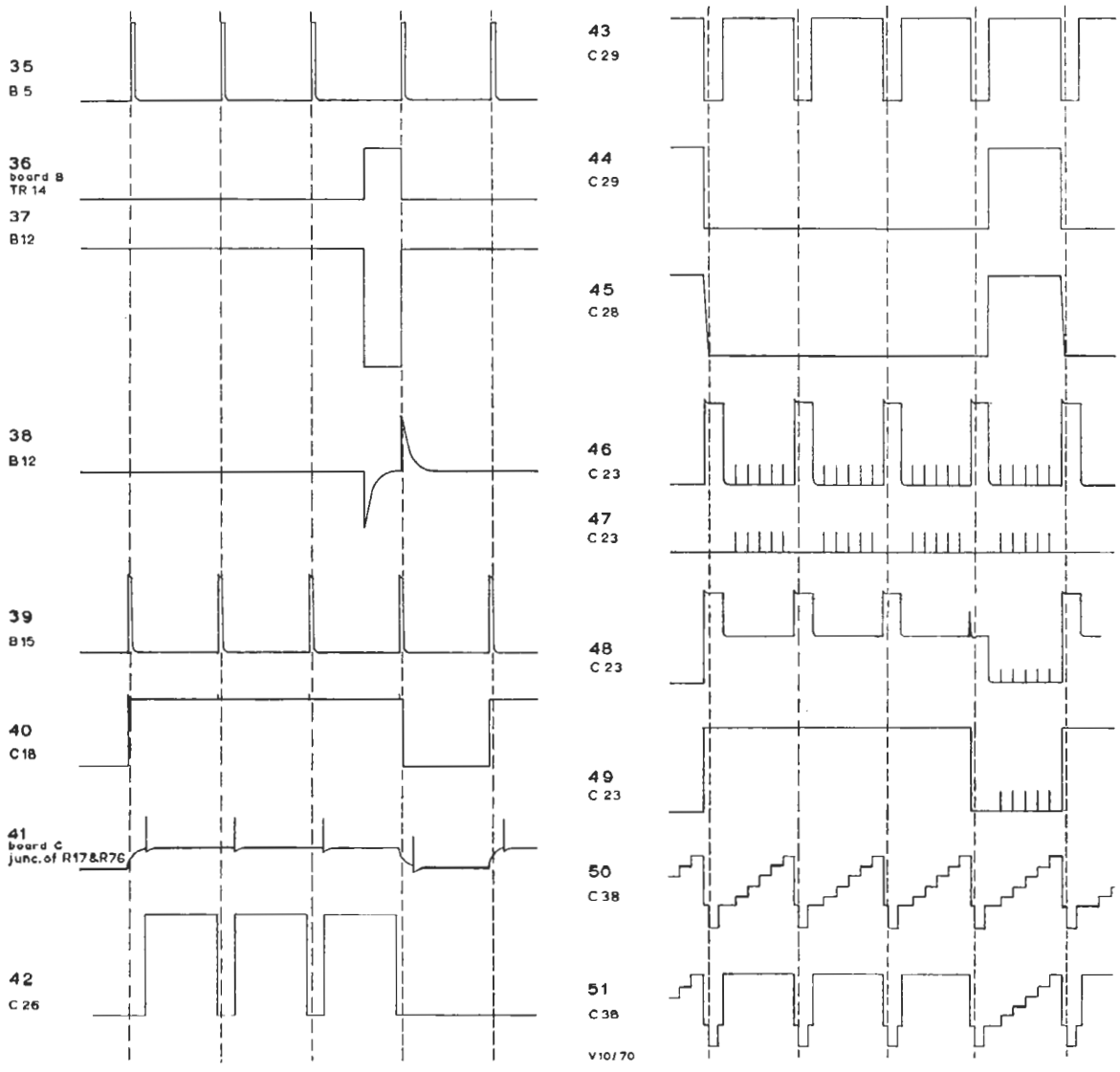

Fig. 25.11 Waveforms in the GE4/525

TABLE 1

Board: pin No. or location	*Waveform or connection*	*Typical amplitude (volts p-p)*	*Switch conditions*
Board A			
A1	+6 volts	—	—
A2	+12 volts	—	—
A3	waveform 24	1·5	Free and Sync
		7.0	Mixed
A4	0 volts (chassis)	—	—
A5	waveform 25	1·4	—
A6	waveform 16	6·0	—
A7	waveform 17	5·0	—
A8	switch SB2	—	—
A9	switch SB2	—	—
A10	switch SB2	—	—
A11	−12 volts	—	—
A12	waveform 6	2·6	Free
	waveform 4	2·6	Sync and Mixed
$TR2_c$	waveform 15	7·5	—
$TR21_c$	waveform 18	7·5	—
$TR31_c$	waveform 19	7·5	—
$TR41_c$	waveform 20	7·5	—
$TR51_c$	waveform 21	7·5	—
$TR61_c$	waveform 22	7·5	—
$TR71_c$	waveform 23	7·5	—
Board B			
B1	switch SB6	—	—
B2	switch SB6	—	—
B3	waveform 7	2·3	Free and Sync
		3·4	Mixed
B4	waveform 6	2·6	Free
	waveform 4	2·6	Sync and Mixed
B5	waveform 35	11·0	—
B6	waveform 6	2·6	Free
	waveform 4	2·6	Sync and Mixed
B7	waveform 25	1·4	—
B8	waveform 27	7·0	—
B9	waveform 13	10·0	Mixed
B10	waveform 46	2·9	Mixed: Step
	waveform 47	0·7	Free and Sync: Step
	waveform 48	4·9	Mixed: CCIR
	waveform 49	1·3	Free and Sync: CCIR
B11	switch SB3	—	—
B12	waveform 37	16·0	Step and Bump
	waveform 38	15·0	CCIR
B13	switch SB3	—	—
B14	waveform 35	11·0	Free and Sync
	waveform 14	10·5	Mixed
B15	waveform 39	11·0	—
B16	+12 volts	—	—
B17	+6 volts	—	—
B18	waveform 11	8·0	Free and Sync
		1·5	Mixed
B19	waveform 24	1·5	Free and Sync
	waveform 11	1·5	Mixed
B20	−6 volts	—	—
B21	waveform 10	8·5	Free and Sync
		5·0	Mixed
B22	waveform 12	6·0	Free and Sync
		1·6	Mixed: Step and CCIR
B23	waveform 13	10·0	—
B24	waveform 14	10·5	—
B25	−12 volts	—	—

Board: pin No. or location	*Waveform or connection*	*Typical amplitude (volts p-p)*	*Switch conditions*
B26	waveform 9 (mixed blanking)	2·0	—
B27	waveform 1 (mixed syncs)	2·0	—
B28	waveform 1 (mixed syncs)	2·0	—
B29	switch SB1	—	—
B30	switch SB1	—	—
B31	waveform 4	12·0	Free
		2·6	Sync and Mixed
B32	waveform 6	2·6	Free
		6·0	Sync and Mixed
B33	0 volts (chassis)	—	—
B34	switch SB5	—	—
B35	switch SB5	—	—
B36	waveform 8	7·0	—
B37	waveform 7	2·2	Free and Sync
	waveform 1 (mixed syncs)	1·7	Mixed
TR5c	waveform 2	12·0	—
TR6c	waveform 3	5·0	—
TR10c	waveform 5	3·4	—
TR14c	waveform 36	7·0	—
Board C			
C1	0 volts (chassis)	—	—
C2	+6 volts	—	—
C3	−6 volts	—	—
C4	burst gate pulse input	3·0	Mixed
C5	+12 volts	—	—
C6	−12 volts	—	—
C7	waveform 1 (mixed syncs)	2·0	—
C8	waveform 9 (mixed blanking)	2·0	—
C9	waveform 6	2·6	Free
	waveform 4	2·6	Sync and Mixed
C10	burst gate pulse input	3·0	Free and Sync
C11	burst gate pulse output	3·0	—
C12	waveform 40	9·5	Step
	waveform 26	16·5	CCIR
C13	switch SE1	—	—
C14	waveform 39	11·0	—
C15	switch SE1	—	—
C16	waveform 38	15·0	CCIR
C17	not used	—	—
C18	waveform 40	9·5	CCIR
C19	waveform 16	6·0	Free and Sync
	waveform 10	5·0	Mixed
C20	switch SE1	—	—
C21	−11 volts	—	Bar or Auto off
	−6 volts	—	Bar on
	square-wave with 20s period (−6 volts and −11 volts)	—	Auto on
C22	not used	—	—
C23	waveform 46	2·6	Mixed: Step
	waveform 47	0·8	Free and Sync: Step
	waveform 48	4·9	Mixed: CCIR
	waveform 49	2·5	Free and Sync: CCIR
C24	waveform 43 inverted	8·0	Step
	waveform 44 inverted	8·0	CCIR
C25	not used	—	—
C26	waveform 42	8·0	Bar on: CCIR and during mark of Bump waveform

Board: pin No. or location	*Waveform or connection*	*Typical amplitude (volts p-p)*	*Switch conditions*
C27	waveform 17	5·0	Free and Sync: Step and CCIR
	waveform 12	1·6	Mixed: Step and CCIR
C28	waveform 43	8·0	Step
	waveform 45	8·0	CCIR
C29	waveform 43	8·0	Step
	waveform 44	8·0	CCIR
C30	waveform 43 (may be inverted)	less than 8·0	Step: Pedestal on
	waveform 44 (may be inverted)	less than 8·0	CCIR: Pedestal on
C31	not used	—	—
C32	not used	—	—
C33	not used	—	—
C34	not used	—	—
C35	waveform 42	less than 8·0	CCIR and during mark of bump waveform
C36	waveform 33	less than 8·0	Step and CCIR
C37	waveform 8	less than 7·0	—
C38	waveform 50	1·4	Step
	waveform 51	1·4	CCIR: Bar on
C39	waveform 50	1·0	Step: Attenuator normal
	waveform 51	1·0	CCIR: Bar on: Attenuator normal

Board: pin No. or location	*Waveform or connection*	*Typical amplitude (volts p-p)*	*Switch conditions*
junction of R17 and R76	waveform 41	7·0	CCIR
Board D			
D1	−6 volts (source)	—	—
D2	waveform 43	8·0	Step
	waveform 44	8·0	CCIR
D3	waveform 17	5·0	Free and Sync: Bump
	waveform 12	4·0	Mixed: Bump
D4	+6 volts (source)	—	—
D5	−12 volts	—	—
D6	0 volts (chassis)	—	—
D7	+12 volts	—	—
D8	waveform 33	2·0	Step and CCIR
D9	waveform 27	7·0	Step and CCIR
$TR2_c$	waveform 28	11·0	Step and CCIR
$TR3_e$	waveform 29	13·0	Step and CCIR
junction of R8 and C5	waveform 30	1·2	Step and CCIR
junction of R11 and C6	waveform 31	18·0	Step and CCIR
$TR4_c$	waveform 32	5·5	Step and CCIR
$TR7_g$	waveform 33	1·65	Step and CCIR

Circuit Description (Board A)

The circuit of printed wiring board A, which contains the modular timing-pulse generator, is shown in Fig. 25.12 and a block diagram is shown in Fig. 25.13. Negative-going pulses coincident with the start of line syncs are fed to two delay circuits. The first delay circuit provides outputs of positive-going and of negative-going pulses at the end of line blanking. The second circuit is the first of a chain of six delay circuits connected in cascade. The outputs of the first five of these circuits are combined to give trains of pulses which are used to time the steps of the staircase waveform. The output of the last circuit in the chain is used to time the trailing edge of the staircase and bar waveforms in the *Sync* and *Free* modes.

The delay circuits are emitter-coupled monostable multivibrators (see Television Engineering, Volume 3) inter-connected via transformers. A change in line standard is effected by changing the potential of the negative supply rail and hence the aiming potential of the timing capacitor in each multivibrator.

Circuit Description (Board B)

The circuit of printed wiring board B, shown in Fig. 25.14, contains the following:

Mixed Mode Trigger Pulse Generator

Mixed blanking pulses (waveform 9) are fed to a two-stage clipping amplifier, which produces five outputs (waveforms 10 to 14). Some of these are differentiated and clipped.

Inverter (2)

Negative-going input pulses at the start of blanking periods (waveforms 11 and 24) are inverted and clipped (waveform 39).

Line Frequency Pulse Extractor

Mixed-sync input pulses (waveform 1) are inverted and clipped by transistor TR5. The inverted sync pulses (waveform 2) are differentiated and used to trigger an emitter-coupled monostable multivibrator with a time constant long enough to avoid double-triggering during the field-sync signal. The output of the multivibrator (waveform 3) is differentiated and inverted to give a negative-going pulse at the start of each line-sync pulse (waveform 4).

A change of line standard is effected by changing the value of the timing capacitor. Variable resistor R21 is a timing control common to both line standards.

Line Frequency Pulse Generator

The line frequency pulse generator is an emitter-coupled astable multivibrator whose output is differentiated, clipped and inverted in a common-emitter output stage. A change of line standard is effected by changing the value of the timing capacitor. Variable resistor R30 is a timing control common to both line standards.

Staircase Gate

The inputs to the staircase gate are:

(a) staircase timing pulses on pin 7 (waveform 25)

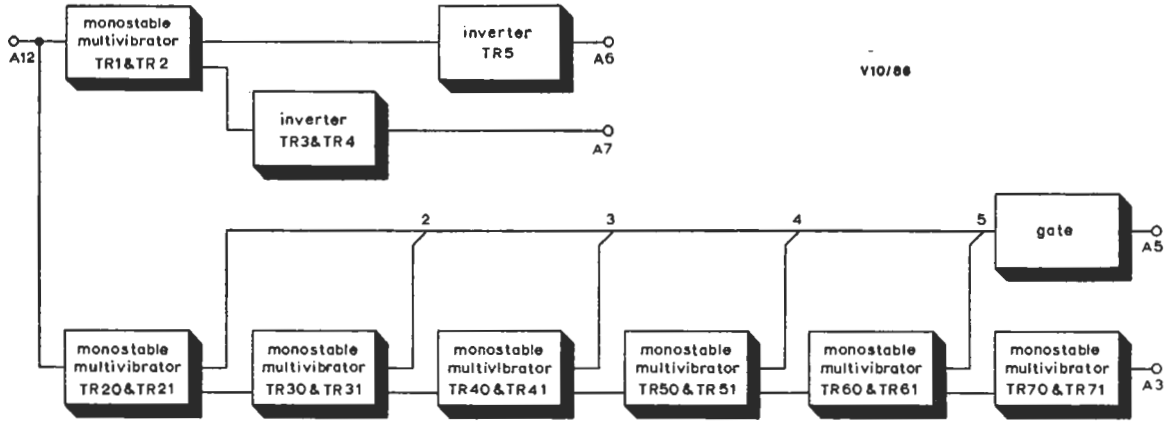

Fig. 25.13 Block Diagram of Printed-wiring Board A

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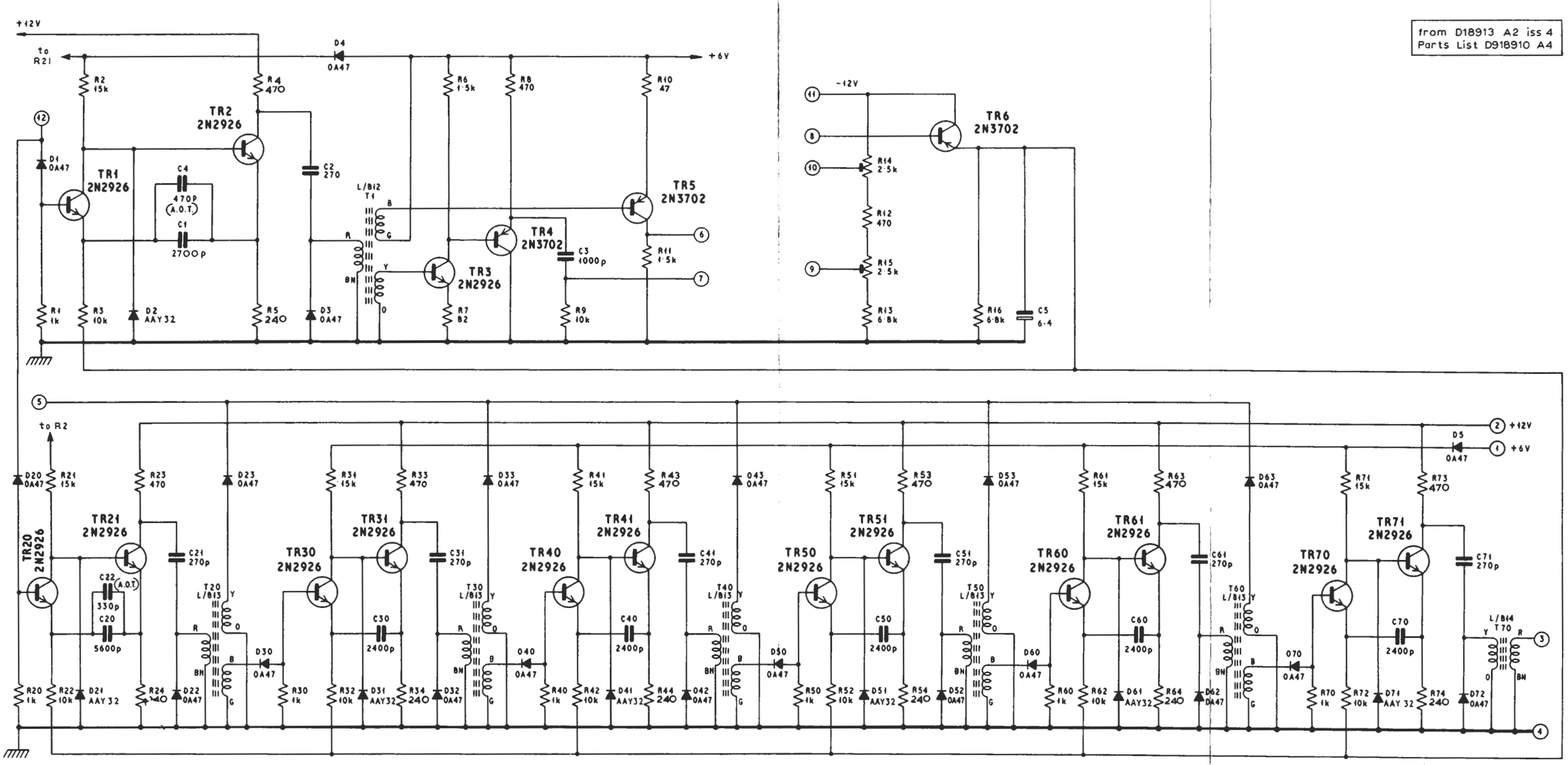
Parts List D918910 A4



NOTE:-
1. TR2, 21, 31, 41, 51, 61, 71 OTHERS ANY COLOUR EXCEPT BROWN.
2. NUMBERS IN BALLOONS REFER TO SOLDER TAGS ON PRINTED BOARD.

transistor terminations view on leads

THIS DRAWING TO BE READ IN CONJUNCTION WITH D1B909 A1

GE4/525/4T

Fig 12. Circuit of Printed-wiring Board A

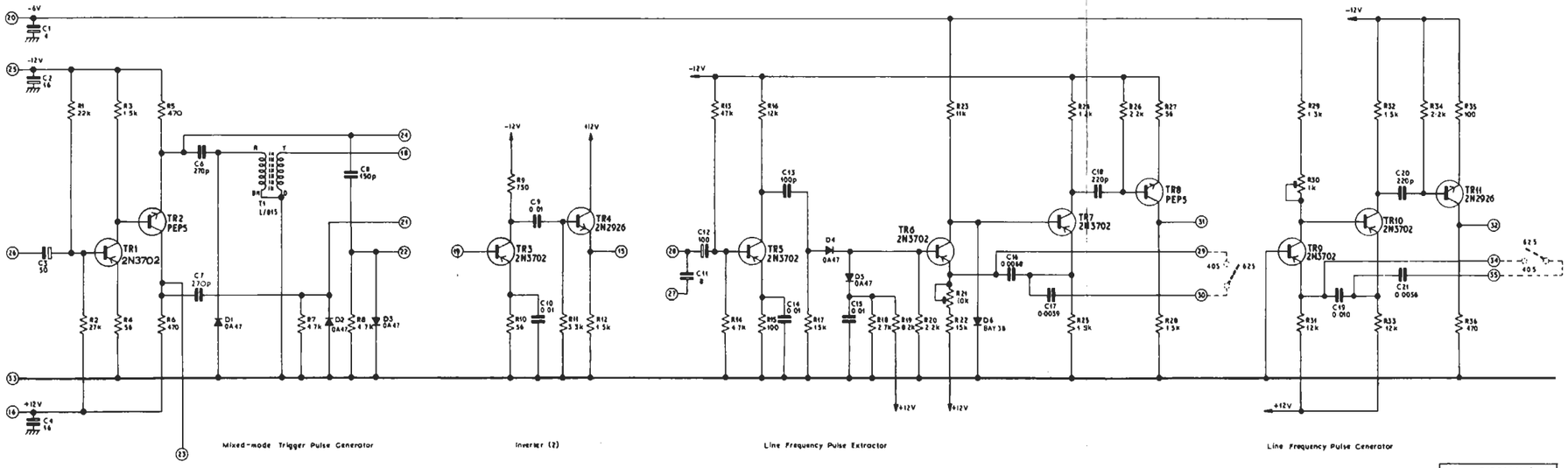


Fig. 14 Circuit of Printed-wiring Board B

(b) mixed blanking pulses on pin 9 (waveform 13)
(c) master gate pulse on pin 10 (waveform 40 inverted).

The positive-going staircase timing pulses appear inverted at the output of transistor TR12 except when the other inputs maintain this transistor in the cut-off condition.

Divider

Positive-going pulses (waveforms 14 or 25) trigger a monostable multivibrator with an unstable-state duration set to about three and a half line periods. A change of line standard is effected by a change in the value of the timing capacitor. Variable resistor R49 is a timing control common to both line standards.

Transistor TR17 forms part of an output amplifier. The output (waveforms 37 and 38) is differentiated by capacitor C27 and an external load.

Inverter (1)

This circuit inverts, amplifies and clips line-frequency pulses.

Line Sync Pulse Generator

Line-frequency pulses (waveforms 4 or 6) trigger a monostable multivibrator. A change of line standard is effected by a change in the value of a timing capacitor. Variable resistor R62 is a timing control common to both line standards.

Sync Pulse Clipper

Sync pulses (waveform 1 or 7) are clipped by diodes at the output of a two-stage amplifier.

Circuit Description (Board C)

The circuit of printed wiring board C, given in Fig. 25.15, contains the following:

Master Gate Pulse Generator

The master gate pulse generator is a bistable multivibrator with one directly-connected input on pin 16 and an input via the test-waveform switch from either a d.c. source (−12 volts) or a feed of line pulses via a differentiating network.

Part of Staircase Gate

Transistor TR3 inverts one output of the master gate-pulse generator. This output is applied to the emitter of transistor TR12 in the staircase gate on printed wiring board B.

Bar Gate

Capacitor C9 isolates diode D4 from the d.c. at the emitter of transistor TR5 (see Fig. 25.11, waveform 41).

Bar Generator

The bar generator is a bistable multivibrator with an inverting output stage.

Pedestal Gate

Negative-going blanking-finish pulses on pin 7 (waveforms 12 or 17) are amplified by a common-base stage, transistor TR9, and by a common-emitter stage, transistor TR10. Master gate pulses (waveform 40) are inverted by transistor TR11 and these bias off transistor TR10 for three lines in every four.

Emitter Follower

Transistor TR12 is an output buffer stage for pulses which are fed to an associated GE4/526 and are also used as c.r.o. trigger pulses.

Pedestal Generator

The pedestal generator is a bistable multivibrator.

Bump Gate Pulse Generator

In the *On* position of the *Auto* switch the gate pulse generator is an emitter-coupled astable multivibrator with a common emitter output stage. In the *Off* position of the *Auto* switch part of the multivibrator is replaced by a d.c. source.

The bar *On/Off* switch short-circuits the output of this generator to the −6 volts supply in the *On* position.

Mixer and Output Amplifier

Transistors TR18 to TR20 form part of a directly-coupled negative-feedback three-stage amplifier with an emitter follower output stage. Three of the four mixer inputs are directly coupled to the amplifier. Variable resistor R64 controls the output d.c. level of the GE4/525.

The amplifier feeds the output of the GE4/525 via a low pass filter and a delta-connected resistance mixing network for adding the chrominance component of the colour non-linearity test signal.

Circuit Description (Board D)

The circuit of printed wiring board D, given in Fig. 25.16, contains the following:

Staircase Generator

Negative-going pulses are fed via an input emitter follower to the base of a blocking oscillator transistor TR2. The positive-going output pulses of the oscillator are fed via an emitter follower to a low-pass filter. The purpose of the blocking oscillator and filter is to produce pulses whose amplitude and shape is independent of the input pulses to the generator. The shaped pulses from the filter are amplified, clipped and inverted in a long-tailed pair amplifier (transistors TR4 and TR17). Variable resistor R10 sets the clipping level.

The negative-going pulse waveform at the collector of transistor TR4 is integrated to produce the staircase waveform. Current pulses from transistors TR5 and TR6 discharge capacitor C7 which is recharged at the end of the active line by clamping at the gate of field effect transistor TR7. The common-base connected transistor TR6 increases the current-pulse source impedance and the use of a field effect transistor TR7 increases the load resistance across capacitor C7. Transistor TR7, connected as a common-drain amplifier, feeds an emitter follower output stage.

Reset Pulse Generator

The reset-pulse generator is a conventional clamping circuit driven either from a waveform (pin D2) which is differentiated and clipped to produce a clamping pulse or from a source (pin D3) of suitable pulses.

Power Supply Regulator Circuits

These conventional circuits produce supplies of $+6$ volts and -6 volts from the ± 12 volt supplies.

Test Procedure

If the GE4/525 requires extensive maintenance it should be returned to Equipment Department. In this Instruction the action of each of the preset controls is given together with the factors relating to their adjustment.

Preset Controls (Board A)

Variable resistors R14 and R15 are the staircase timing controls on the 405-line and 625-line standards respectively. The correct timings for the five leading edges and the trailing edge of the staircase are given in Fig. 25.10 (waveform 25 and 24). If the relative timings of these edges are not quite as shown, the controls must be set to give the correct trailing-edge timing.

Preset Controls (Board B)

Variable resistors R21, R30, R49 and R62 control the unstable-state duration of four monostable multivibrators. The controls are common to both line standards and so a compromise is necessary in their adjustment.

1. Observe the waveform on pin 29.
   Adjust R21 to give an unstable-state duration of 40 ± 3 μs on 625-lines and 63 ± 5 μs on 405-lines.
2. Observe the waveform on pin 32.
   Adjust R30 to give a period of 64 μs on 625-lines.
   The period on 405-lines should be 100 ± 7 μs.
3. Observe the waveform on pin 13.
   Adjust R49 to give an unstable state duration of 224 ± 8 μs on 625-lines and 350 ± 12 μs on 405-lines.
4. Observe the waveform on pin 3.
   Adjust R62 to give a period of $4{\cdot}7\pm0{\cdot}2$ μs on 625-lines.
   The period on 405-lines should be 9 ± 1 μs.

Preset Controls (Board C)

Variable resistor R51 controls the period of the bump waveform which should be set at about 20 seconds.

Variable resistor R64 controls the d.c. level at the output of the GE4/525 and should be adjusted to give a blanking level of $+0{\cdot}5$ volts at the output socket.

Preset Controls (Board D)

Variable resistor R10 controls the clipping level of transistor TR4. It should be set so that the potential of the base-line of the waveform is $+10$ volts.

Variable resistor R32 is the staircase generator clamping-level control. It should be set to give minimum change of d.c. level at the output of the GE4/525 with a change in staircase amplitude.

Variable resistors R35 and R44 are the $+6$ volts and -6 volts regulator controls.

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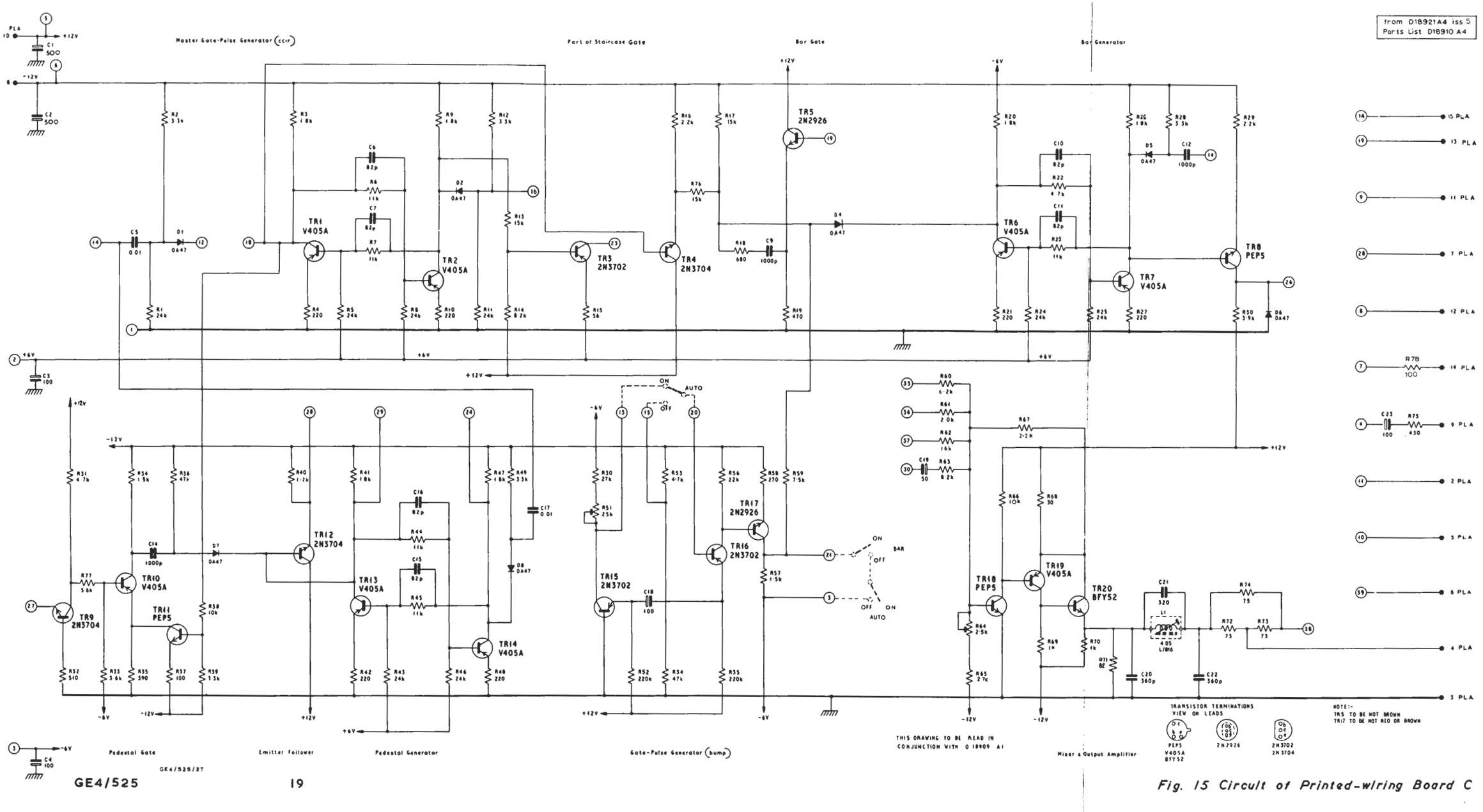

Fig. 15 Circuit of Printed-wiring Board C

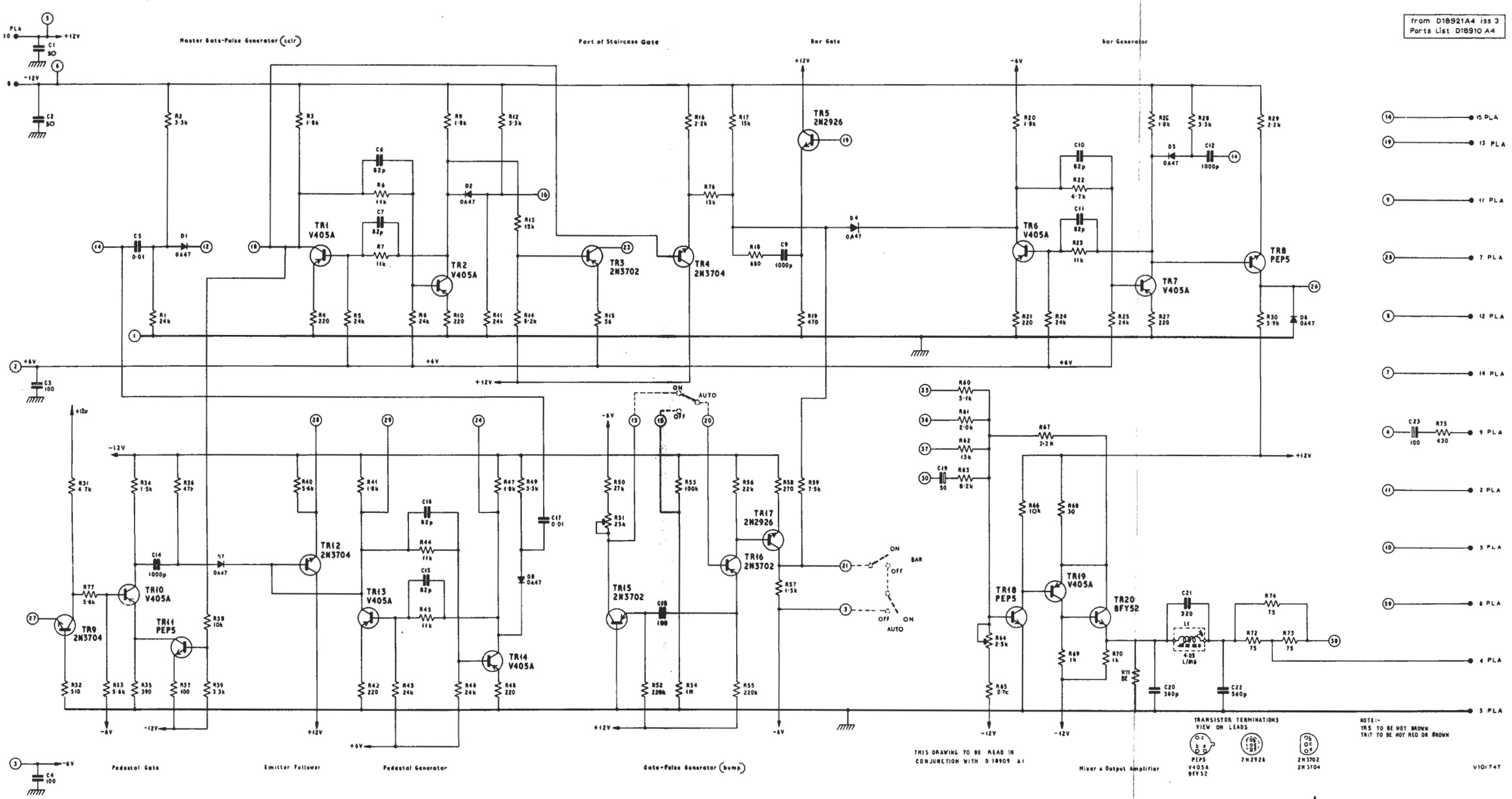

Fig. 25.15 Circuit of Printed-wiring Board C

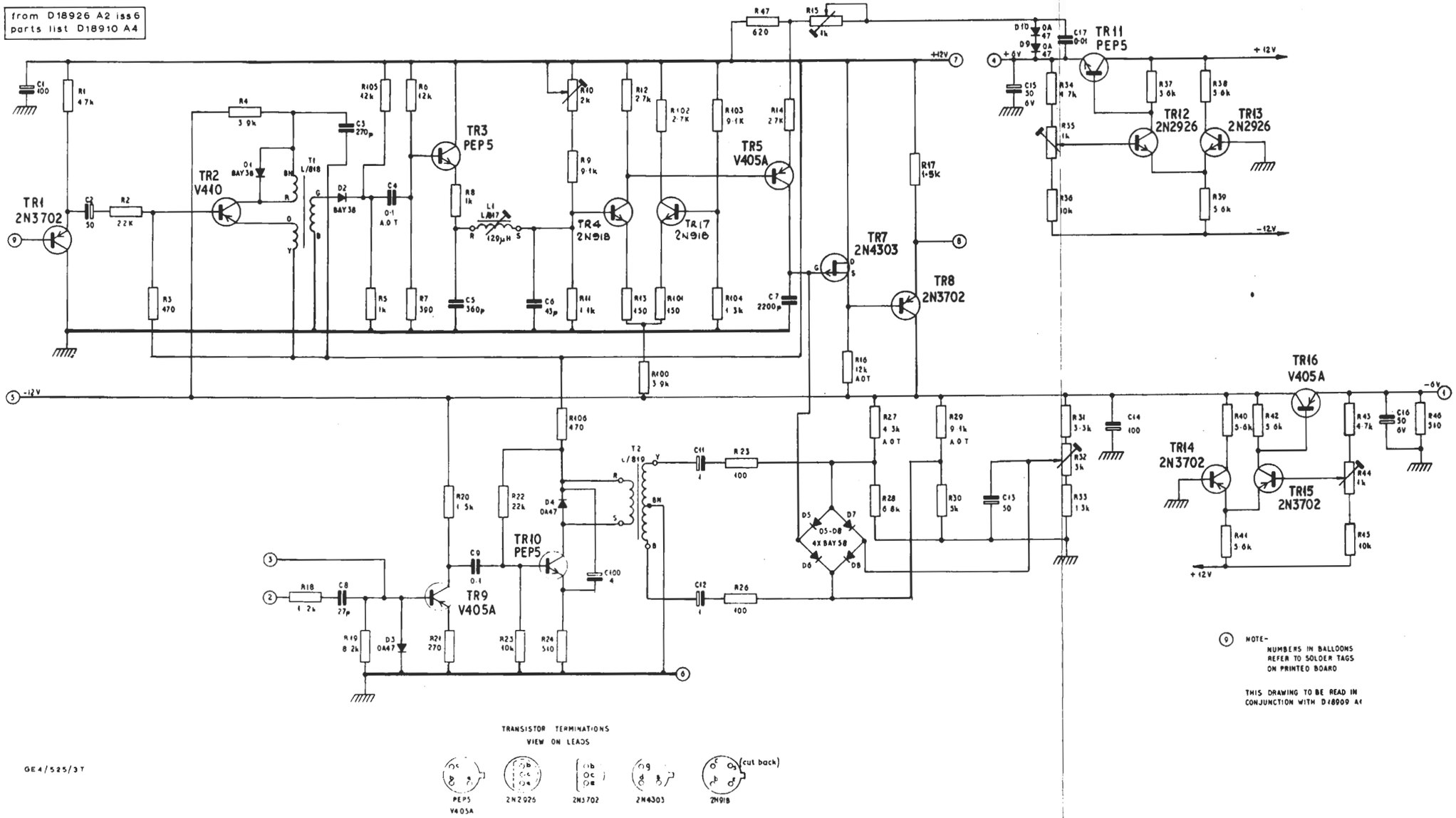

Fig. 16. Circuit of Printed-wiring Board D