FAULT INDICATOR UNIT IN5/503

Introduction

The IN5/503 accepts a d.c. input signal which, if present for greater than a predetermined integration period, causes a d.c. output signal to be produced and a lamp signal to be given. The integration circuit can be reset by other d.c. signals. Another circuit in the unit allows a single bit of information, at a separate input, to be stored until the integration circuit is reset. The unit is designed for use with a Television Automatic Monitor MN2M/518.

The unit is built on a printed wiring board which is mounted on a CH1/43A chassis with index pegs in positions 1, 4 and 9.

General Specification

Integration delay before a continuous output signal is given	10 seconds nominal
Delay after which the continuous output signal ceases	15 seconds nominal
Logic levels	
Logic 1	+2·6 volts minimum
Logic 2	+0·4 volt maximum
Power requirements	+12 volts at 20 mA +6 volts at 60 mA +5 volts at 35 mA
Pin connections	25-way ISEP plug

Circuit Description (Fig. 1)

The circuit (Fig. 1) is in two sections which are considered separately below.

(a) Integrate and Reset Circuit

This is shown in the upper half of Fig. 1 and comprises the quad NAND gate and all the transistors.

A logic 1 signal at PLA12 charges C3 in a time determined by R4. When the potential across C3 has risen sufficiently, field-effect transistor TR2 conducts and Schmitt trigger TR1c and TR1d changes state. Consequently TR4 and TR1e are cut off. Alarm lamp ILP1 is switched off and a logic 1 output signal is developed at pin PLA13.

(b) Store Circuit

This comprises the two quad NAND gates IC2 and IC3. The circuit is arranged so that when logic 1 signals are entered at the inputs to gate IC2a/3, the output at PLA11 is held at the logic level of the signal input to PLA10. A change in state of the signal at PLA10 does not affect the output at PLA11 if the inputs to gate IC2a/3 are not at logic 1.

Test Schedule

Apparatus Required

+12 volt Stabilised Power Supplier
+6 volt Stabilised Power Supplier
+5 volt Stabilised Power Supplier
Avometer Model 8

Test Procedure

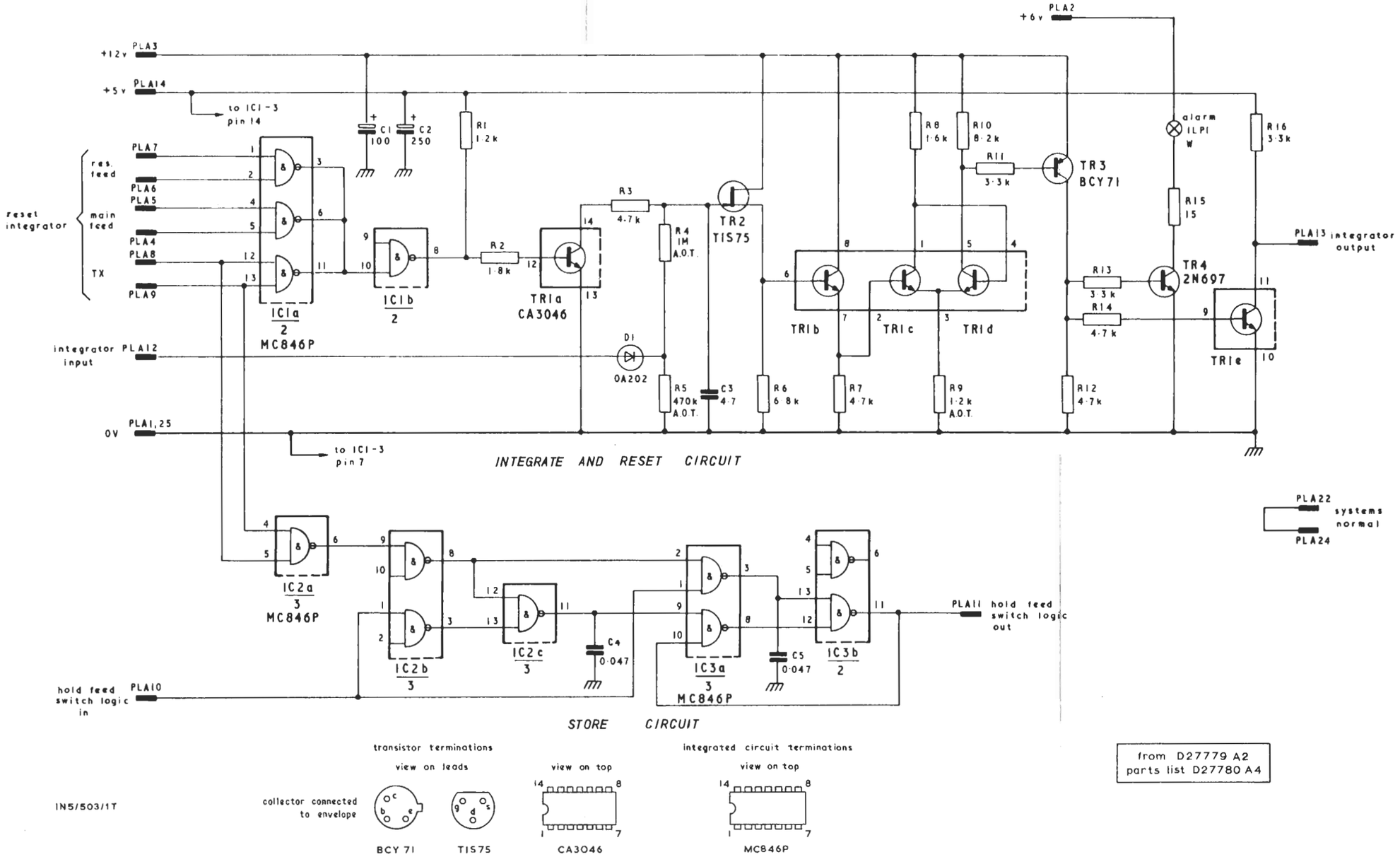
1. Connect pins PLA5, 6, 8 and 12 to chassis.
2. Measure the f.e.t. offset voltage developed across resistor R7.
3. Disconnect pin PLA12 from chassis and connect it to the +5 volt supply.
4. Check that after about 10 seconds the Alarm lamp goes out.
5. Measure the final voltage developed across resistor R7 after the lamp is extinguished.
6. Remove the 5-volt supply and reconnect pin PLA12 to chassis.
7. Check that, after about 15 seconds, the Alarm lamp lights.
8. Repeat steps 3 to 7 and measure the trigger voltages across resistor R7 each time the lamp is switched off and on. The voltage difference between these two measurements must be 1·25 ±0·5 volts. The two measured voltages must also lie symmetrically between the f.e.t. offset voltage and the final voltage. The higher trigger voltage must be at least one volt above the f.e.t. offset voltage. The value of resistor R9 is selected to make this so.
9. Measure the voltage at pin PLA13; this should be at least four volts when the lamp is off and less than 250 mV when the lamp is on.
10. Disconnect pin PLA12 from the chassis and connect it to the +5 volt supply.
11. Disconnect pin PLA5 from chassis and check that the lamp is switched on.
12. Connect pin PLA5 to chassis and check that the lamp is switched off after about 10 seconds.
13. Repeat steps 11 and 12 but using pins PLA6 and PLA8.
14. Connect pin PLA10 to chassis.
15. Connect the Avometer between pin PLA11 and chassis and check that the meter reads zero volts.
16. Momentarily disconnect pin PLA8 from chassis. Check that no change occurs in the meter reading.
17. Disconnect pin PLA10 from chassis and check that no change occurs in the meter reading.
18. Momentarily disconnect pin PLA8 from chassis. Check that the voltage at pin PLA11 is about 4·5 volts. This voltage should be maintained irrespective of further changes at pin PLA10.

Reference

Designs Department Specification 11.102 (70).

Reference to Typical Associated Equipment

Television Automatic Monitor MN2M/518.



IN5/503/1T

transistor terminations view on leads

collector connected to envelope

BCY 71 2N697

TIS75

view on top

CA3046

integrated circuit terminations view on top

MC846P

from D27779 A2
parts list D27780 A4

Fig.1. Circuit of IN5/503