# VIDEO SWITCHING MATRICES MA2M/501, MA2M/502 SERIES

## Introduction

The MA2M/501,502 series of solid-state matrices provide remotely-controlled facilities for switching a number of video inputs (sources) to a number of outputs (destinations). The MA2M/501 has a maximum capacity of 25 sources and 12 destinations and the MA2M/502 has a maximum of 25 sources and 8 destinations. The MA2M/501A and MA2M/502A are precisely similar except that they have high impedance inputs and are used for parallel working.

Each matrix is built from one or more of the sub-units listed:

AM23/501A–D Video Matrix Source Amplifier for MA2M/501 (suffix indicates 12, 11, 10 or 9 destination routes).

AM23/503A–H Video Matrix Source Amplifier for MA2M/502 (suffix indicates number of destination routes from 8 to 1).

AM23/502A–Z Video Matrix Destination Amplifier (suffix indicates number of sources from 25 to 1).

PS2L/80 Power Supplier
EQ1/516 Video Equaliser
NE4/515 Matrix Phasing Network
AT3/510 Video Frequency Attenuator

} depending on circumstances at each installation

Source and destination amplifier cards are mounted edgeways and at right angles to each other on opposite sides of a mother card which provides the interconnections. A screened housing accommodates the input circuit terminations and the attenuator, equalising or phasing units and a musa panel provides one output per destination. The assembly is arranged for rack mounting.

Matrices are equipped with the number of source and destination amplifiers relevant to the number of inputs and outputs being served. Up to three matrices may be connected in parallel at the inputs, providing 25 sources and 36 destinations, i.e. 25 times 36 switching points. In such arrangements 2 of the 3 paralleled matrices must be of the high impedance types but an external power supplier PS2L/80 is required for each MA2M/501 or MA2M/502 matrix.

## General Specification

The following applies to any route through the matrix:

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|---|---|
| *Input and Output Signal Level* | 1V p-p |
| *L.F. Insertion Gain* | 0 dB ±0·2 dB |
| *Chrominance/Luminance Gain Ratio* | 1 ±1% |
| *Monochrome Pulse and Bar Waveform k Ratings* | |
| Pulse/bar ratio | less than 0·25% |
| 26-μsec bar | less than 0·25% |
| 50-Hz square wave tilt | less than 0·5% |
| *Return Loss at 4·43 MHz* | |
| Input | 40 dB |
| Output | 46 dB |
| *Non-Linearity Distortion* | |
| Line-time non-linearity | not greater than 0·5% |
| Differential phase distortion | not greater than 0·2% |
| Differential gain distortion | not greater than 1% |
| *D.C. Characteristics* | |
| Mid point of picture component of staircase waveform | 0V ±50mV |
| Output d.c. (source selected, no signal) | −0·15V ±50mV |
| Output d.c. (no source selected) | +0·1V ±0·1V |
| *Crosstalk at Subcarrier Frequency* (With all other routes hostile, crosstalk to measured route) | not greater than −70 dB |
| *Route Propagation Time* (between input and output musas) | 67° at 4·43 MHz |
| *Power Input to PS2/80 Power Supplier* (nominal) | 0·75A at 240v, 50Hz |

| | |
|---|---|
| *Performance Stability* | |
| Up to 10,000 hours use, operationally and standby | negligible change |
| Gain Variations 20° C.–40° C. | less than 0·1 dB |
| Change in Output D.C. Level with temperature | —3mV/° C. |
| *Maximum Temperature of Ingoing Cooling Air* | 40° C. |

**Circuit Description**

The input video cables terminate in the musa jackfield. From each input point the signal normally passes through a 3-dB attenuator AT3/510 but this may be replaced by an equaliser EQ1/516 to offset loss caused by a maximum of 150 ft. of PSF1/3 input cable. The equaliser has an insertion loss of 3 dB and gives equalisation at 4·43MHz of between 0·26 dB and 0·4 dB. The high impedance matrices MA2M/501A and MA2M/502A are used in parallel with the MA2M/501 or MA2M/502 with the connections shunted across the source amplifier input, see Fig. 1. NE4/515 Phasing Networks can be fitted at the inputs if required and give an adjustment of $\pm 2°$ at 4·43 MHz. Any routes through high impedance matrices which are not paralleled are fitted with equalisers or attenuators during installation.

Each of the 25 inputs to the matrix has a source amplifier with 3-dB gain and with a maximum of 12 outputs. Each output is connected via a cross point to one of the 25 inputs of each of 12 destination amplifiers, the interconnections being provided by the mother card. The arrangement is indicated in Fig. 1. Each cross point consists of a shunt switch (associated with a source amplifier) and a series switch (associated with a destination amplifier), each pair of switches being interdependent. The shunt element has an 'on' impedance of 1 ohm and a very high 'off' impedance which has negligible effect on the circuit. The series switch has an 'on' impedance of 30 ohms and an 'off' impedance comprised of a capacitive reactance of 0·3 megohm at 4·43 MHz in parallel with a very high resistance. Interaction between routes through the matrix is minimised by building out the intrinsic low output impedance of each source amplifier (less than 1 ohm) to 1·3 kilohm at the feed point to the associated shunt switch.

Selection of a route is by means of a 50-volt control signal which closes the series switch in the destination amplifier of the required route and causes a current of 4mA to flow from the source amplifier into the destination amplifier. While the current flows, the shunt switch in the source amplifier is held off. When the 50-volt control signal is removed the series switch opens and the circuit for the 4mA is broken. The potential at the output of the source amplifier starts to rise, causing the shunt switch to close, effectively short-circuiting the signal path. A minimum time of about 20 picture lines is required for this switching action to be completed. There must, therefore, be a clear break between the release of a source by a destination and the selection by that destination of a further source.

The removal of the 50-volt control signal from a destination amplifier, besides closing the shunt switch and opening the series switch, also operates a circuit in the destination amplifier which maintains the d.c. output level at sensibly the same value as when a source is selected, thus stabilising the d.c. conditions on the matrix.

A source amplifier can feed all 12 destination amplifiers simultaneously, but a destination amplifier can only accept an input from one source amplifier at a time. If more than one source is inadvertently connected to a destination amplifier, severe limiting of the signal occurs and nothing reaches the output.

**Maintenance**

The setting of the amplifier gain and d.c. level must be carried out with the greatest accuracy possible within the resolution of the controls concerned. The setting-up process involves the use of a test jig TE2/502 which accurately simulates the matrix conditions. The test procedure for both source and destination amplifiers is given in the relevant Technical Instructions.

Note that the signal level at the cross points is low and that monitoring at these points is not practical.

**References**

1. Designs Department Specification No. 8.348(69).
2. Designs Department Technical Memorandum No. 8.277(69).
3. *B.B.C. Engineering* No. 83 (July 1970).

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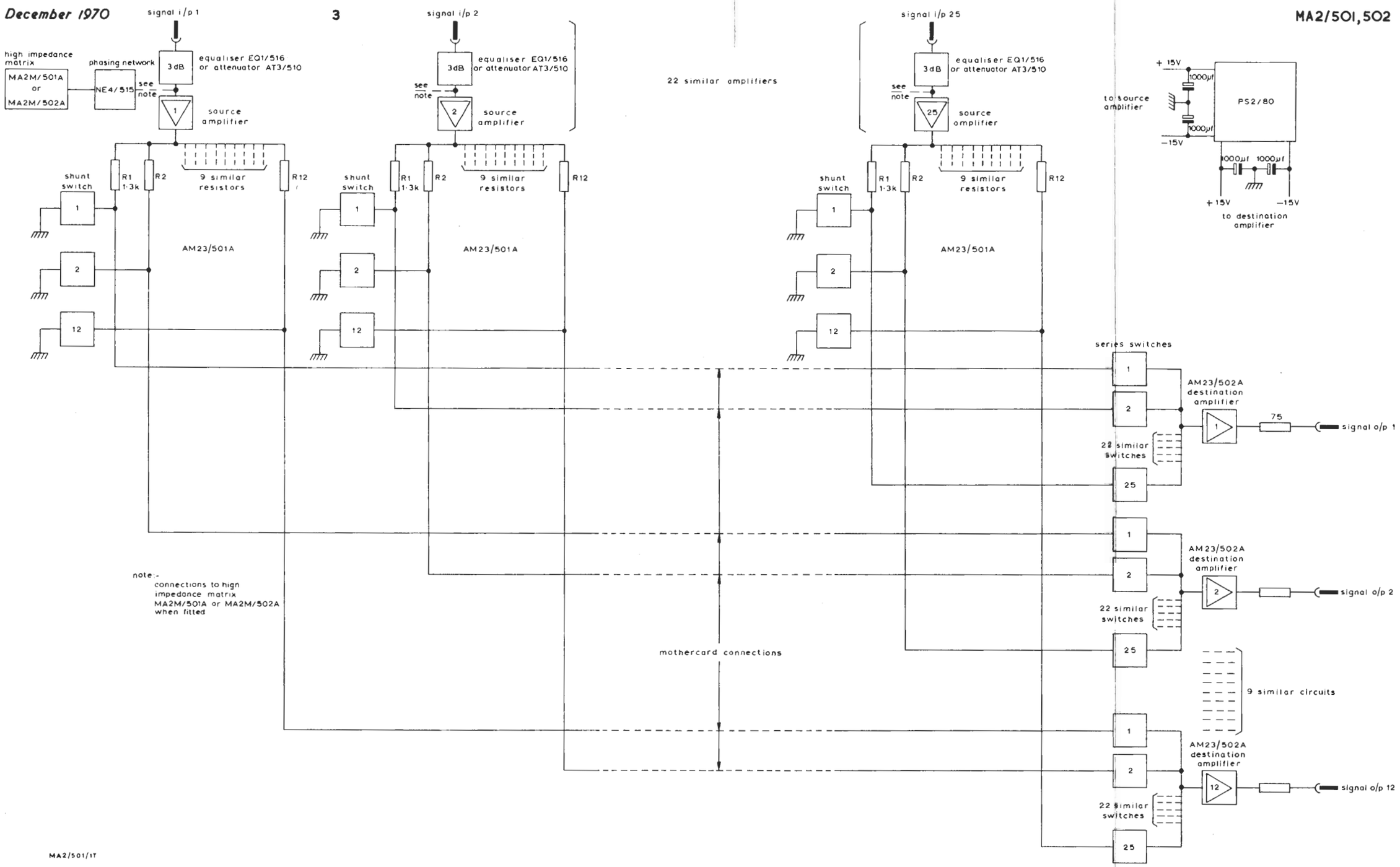


*Fig.1 Block Diagram of the Video Matrices MA2/501 and MA2/502*