VIDEO SWITCHING MATRIX MA2L/504

Introduction

The MA2L/504 provides two fully independent 6-input to 1-output source selection systems. Each source signal is d.c. restored prior to switching so that this can be performed with negligible disturbance to the output blanking level. Switching can be timed to occur during the field interval by the use of an external switching waveform generator[1] driven by a sync-pulse-triggered clock-pulse generator[2].

The MA2L/504 comprises:

- two MA2/503 Unit Matrix printed-wiring cards;
- a chassis PN3/53A which occupies $2\frac{1}{8}$ in of a PN3/23; this chassis accommodates the two MA2/503 cards;
- a special back panel, equipped with connectors for video inputs and outputs, control inputs and power-supply inputs.

General Specification

Signal Inputs

Amplitude	standard level colour video signal
Impedance	75 ohms (matched to ±0·1%)
Return loss at 4.43 MHz	⩾30 dB

Signal Outputs

Number	2 of transmission quality standard level ± 0·1 dB colour video signal
Impedance	75 ohms ± 1%
Return loss at 4·43 MHz	⩾36 dB
No-signal output voltage	−0·65 ± 0·05 V
Signal blanking level	−0·35 ± 0·05 V

Control Inputs see **Description**

Transmission Parameters

Input-to-output delay	36° ± 0·5° at 4·43 MHz
Chrominance/luminance	
gain inequality	<± 0·5%
delay inequality	<± 2 ns

Crosstalk (worst case) better than −76 dB

All except one input hostile with 1-V p-p 4·43 MHz signal; single terminated input selected

Power Input (per MA2/503) +12 V, 220 mA, −12 V, 180 mA

Temperature Range 0°C to 40°C ambient

Description

Circuit

A block diagram of the MA2L/504 is given in Fig. 1 and the circuit diagram is given in Fig. 2. The Matrix is available with one of several control-circuit configurations chosen from the range detailed in Table 1.

Table 1

Control Source	*Control Circuit Characteristics*		*Switching Mode*	
	To set video crosspoint on	*To set video crosspoint off*	*Untimed (Preselect)*	*Timed (On-air)*
D.C. supply voltage via make/break switch	+12 V from 620 Ω from MA2L/504 (PLJ.B)	Control input open circuit (0 V)	Fit C1 – 6; R7 – 12 = 560 Ω; Fit 510 Ω in link positions	
	+50 V from low impedance (in combination with MA2M/501)	Control input open circuit (0 V)	Fit C1 – 6; R7 – 12 = 560 Ω; Fit 6·2 kΩ in link positions	
I.C. logic e.g. GE6/527	+5 V from 2 kΩ, 6 kΩ (DTL)	0 V from low impedance	No C1 – 6; R7 – 12 = 18 kΩ; Fit links	No C1 –6; R7 – 12 = 18 kΩ; Fit links
	+3·8 V from low impedance (TTL)	0 V from low impedance	No C1 –6; R7 – 12 = 18 kΩ; Fit links	No C1 – 6; R7 – 12 = 18 kΩ; Fit links

Notes: 1. Low impedance is less than 150 ohms
2. Component numbers refer to MA2L/504 Circuit in Fig. 2.

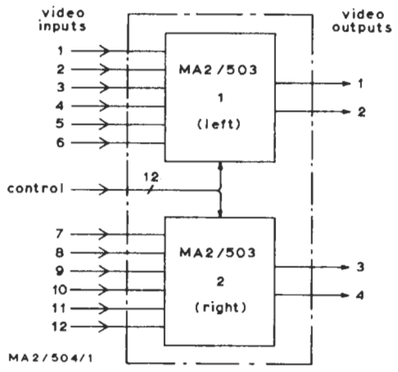
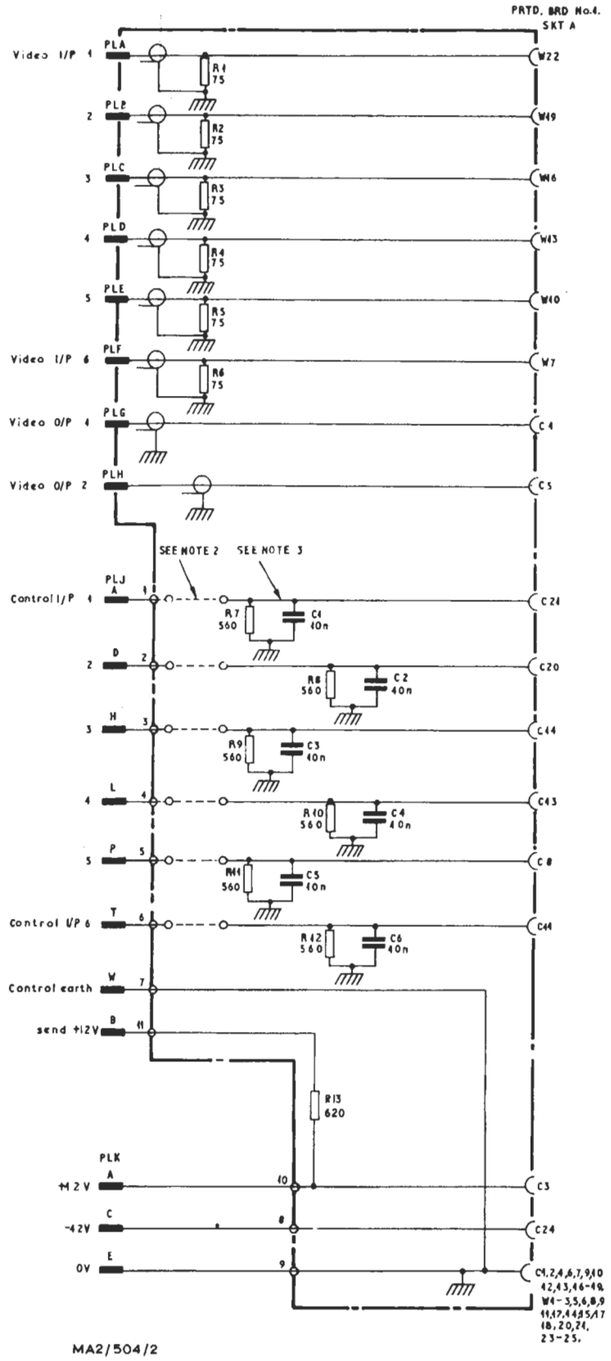


Fig. 1. MA2L/504: Block Diagram



NOTE 4. SKT A tag numbers pre-fixed by letter 'C' are on the component side of printed board, those pre-fixed by letter 'W' are on the wiring side of the board.
2. Link or component fitted as specified on order
3 R7-12, C1-6 fitted when specified on order.

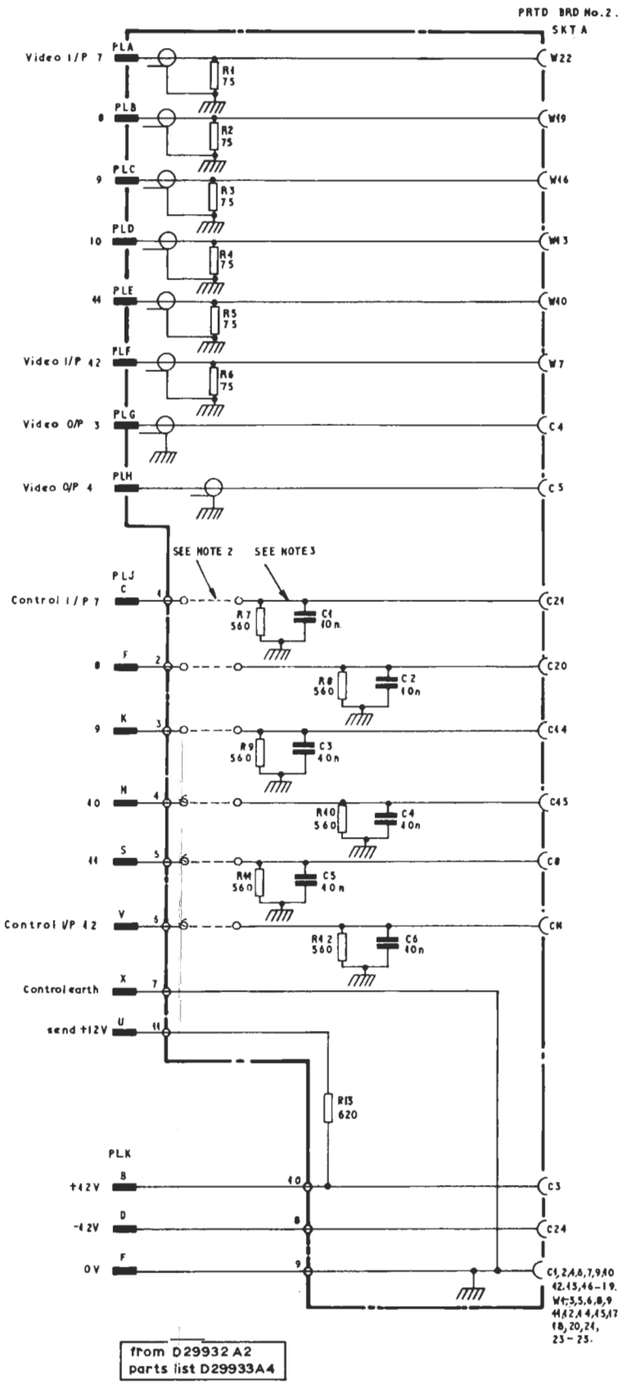


Fig. 2. MA2L/504: Circuit Diagram

Nevertheless, control inputs to the Unit Matrix card MA2/503 are the same, regardless of the option chosen. The limits of these control voltages are:

On condition V_{max}: + 5·2 V; V_{min}: +3·6 V;

Off condition V_{max}: + 0·2 V; V_{min}: 0 V.

Care should be taken with maintenance or test not to exceed these limits.

Field-interval Switching

The timing of control signals for field-interval switching should be coincident or non-overlapping.

Distortion on the output signal may occur during the resulting minimum 5-μs switching period; it can take two forms:

- blanking level may vary in a positive direction by up to 100 mV;
- fast transients may occur at start and finish of switching; their amplitude is less than 100 mV and typical duration is 100 ns.

Maintenance Notes

The following notes on adjust-on-test components cross-refere to the alignment procedure given below.

D.C. Conditions

R10 determines d.c. level at TR5 emitter and hence TR9 source voltage;
R43 determines d.c. level at output;
R44 determines TR41 emitter voltage.

Insertion Gain

R61 adjusts matrix gain;
R15 sets channel gain-matching

Chrominance/Luminance Gain Radio

C51 sets matrix chrominance/luminance gain ratio;
C8 sets channel chrominance/luminance gain ratio matching.

Transmission Delay

C7 determines channel transmission delay matching.

Alignment

This is not a routine procedure and should not be treated as such. It is given as a guide to correct alignment after a faulty component has been replaced. Extreme care is essential if any alteration is required.

D.C. Conditions

Set the supply voltages to ±12·00 ±0·05 V with all channels *off*.

TR9 gate potential should be −7 V for all channels.

Check that current consumption is 220 mA at +12 V and 180 mA at −12 V.

Disconnect one end of R41 before making any subsequent measurements.

Measure and record the voltage at TR9 source when each channel is selected *on*.

The average should be +220 mV and the spread less than 5 mV. If necessary, change R10 to align deviant channels.

Check that TR9 gate potential for each channel selected *on* is 0·03 ±0·05 V.

If necessary, change R44 to make TR41 emitter voltage 6 mV lower than the lowest voltage measured at TR9 source i.e. typically +214 mV.

If necessary, change R43 to set d.c. level at terminated output to −0·55 V.

Check that TR41 emitter voltage is still at the value set by R44.

Reconnect R41 and confirm that the picture component of an all-lines staircase signal is set mid-way about 0 V.

Insertion Gain

If the insertion gain for all channels is not correct, adjust R61 to obtain 0 ±0·1 dB on as many channels as possible.

Change R15 in out-of-tolerance channels; (sensitivity: 20 ohms per 0·1 dB).

Chrominance/Luminance Gain Ratio

If the gain ratio for all channels is not correct change C51 to obtain unity gain ±0·5% on as many channels as possible.

Change C8 in out-of-tolerance channels; (sensitivity: 30 pF per 0·2%).

Determine and allow for the effect of the screens.)

Transmission Delay

The uncorrected propagation delay of about 34° at 4·43 MHz is standardised to 36° ±0·5° by the capacitor C7; (sensitivity: 2 pF per 0·1°).

(Determine and allow for the effect of the screens).

References to Typical Associated Equipment

1. Switching-waveform Generators GE6/527
2. Clock Pulse Generators GE2/607

RDH 8/72