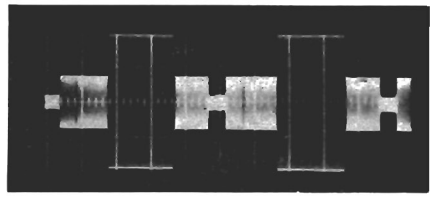
SECTION 18

CARRIER AMPLITUDE MODULATOR MD2/503

Introduction

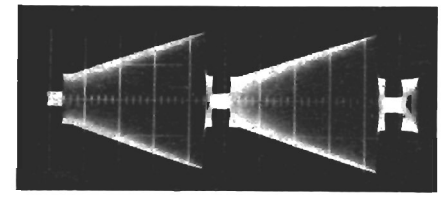
This sub-unit accepts a standard video signal and a feed of mixed synchronising pulses and produces a 30-MHz, positive-amplitude-modulated, double-sideband carrier signal as shown in Fig. 18.1 (a) and (b). Positive and negative power supplies are required.

The sub-unit is constructed on a Chassis Type CH1/12B (indexing pin positions Nos. 14 and 29). The components are assembled on two printed-wiring boards, one of which carries all the parts of the circuit operating at carrier frequency and is enclosed in a screening box.



Modulated Pulse and Bar
Output signal

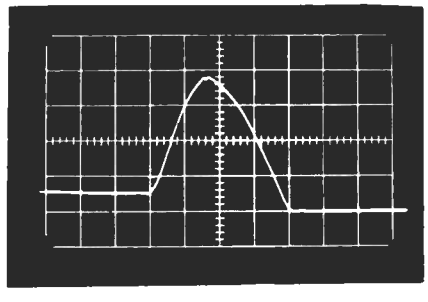
(a)



Modulated Sawtooth
Output signal

(b)

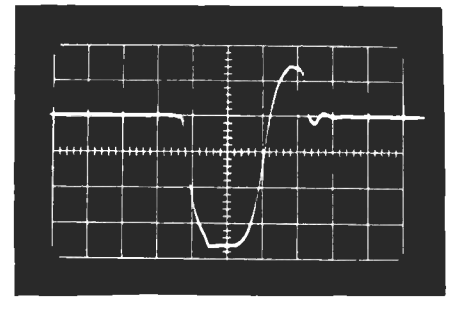
(Displayed on Tektronix type 585 Oscilloscope)



Waveform at junction of
R24 and L10
(0·5v/cm, 0·5μs/cm)

(c)

V9/27P



Waveform at junction of
C27 and R28
(2v/cm, 0·5μs/cm)

(d)

Fig. 18.1 Carrier-amplitude Modulator MD2/503: Waveforms

General Specification

Inputs	
Composite video signal	1 volt p-p into 75 ohms
Mixed synchronising pulses	2 volts p-p into 75 ohms, in synchronism with the video signal.
Output (30 MHz)	
peak white	90 mV ± 1 dB
sync level	8 mV ± 1 dB
Output-terminating Impedance	75 ohms
Delay	50 ns from video-signal input point to r.f.-signal output point.
Linearity	Picture-signal distortion factor is less than 1%
Bandwidth	Unrestricted over spectrum of video signal
Power Requirements	+18 volts, 95 mA −12 volts, 80 mA
Weight	2½ lbs.

Circuit Description

A circuit diagram of the sub-unit is given in Fig. 18.2. The carrier signal is generated by a crystal-controlled oscillator stage utilising TR1, and is amplified by the tuned-collector cascode stage TR2, TR3. The capacitor C8 is provided to neutralise the input inductance of TR3. After impedance-transformation (T1) and attenuation (R13-15) the signal is applied to transformer T2 of the ring modulator. (The principle of the ring modulator is explained in Section 2 of Instruction L.1.) From the secondary winding of the output transformer T3 of the modulator, the signal is fed to the output pin (11) of the sub-unit connector via a filter tuned to minimise any second-harmonic (60-MHz) component.

The modulating video signal is applied to the base of TR9, where clamping occurs during the line-synchronising pulses to a reference potential of approximately six volts determined by the zener diode D8. TR9 is the first of a chain of four emitter followers which serve to reduce the zero-frequency impedance of the signal path from the high value necessary at the clamped point to the low value required for connection to the ring modulator.

To maintain the dynamic balance of the ring modulator, a d.c.-balanced video input circuit is used so that the effects of changes of ambient temperature on the base-to-emitter potential differences in TR11 and TR12 are offset by the same changes in TR13 and TR14. (TR9 and TR10 are complementary transistors in which such changes tend to offset one another.)

To preserve the d.c. component of the video signal the modulator is adjusted so that there is about 9% carrier leak at the bottom of synchronising pulses.

The pulses which drive the clamp are derived from incoming negative-going mixed synchronising pulses. These, after current amplification by the emitter follower TR4, are differentiated by the short time-constant of C24 and the input impedance of TR5. The differentiated initial potential-transistion of each pulse causes a momentary flow of collector current in TR5 which shock-excites the tuned circuit L10, C25 (c), Fig. 18.1. The first half-cycle of oscillation, after voltage and current amplification by TR15 and TR6 respectively (see Fig. 18.1) is applied to T4 and produces a pulse of approximately 15 volts peak amplitude and 1·2 μs duration from the secondary winding of the transformer. The second half-cycle is heavily damped by the conduction of D5 and D6. The pulse from T4, applied to both TR7 and TR8, causes a low-resistance circuit path to appear between the collectors of the two transistors, which connects the base of TR9 to the clamping-reference potential at the cathode of D8. D7 and C28 produce a reverse bias on TR7 and TR8 between pulses, ensuring that the transistors are then non-conducting.

Clamping commences 1 μs after the initial transistions of the line-synchronising pulses.

Maintenance

The waveforms shown in Fig. 18.1, and the transistor-electrode potentials set out below, are given to assist in the maintenance of the sub-unit. The *Set Modulation* control is normally adjusted to cause about 90% positive modulation of the carrier signal, as shown in Fig. 18.1 (a); it should be possible, as a check on the balance of the modulator, to turn the control slightly anti-clockwise through a setting which causes the signal amplitude to fail to zero during synchronising pulses. If this cannot be done, the modulator must be re-balanced in the manner described in Designs Department Specification No. 7.67 (65).

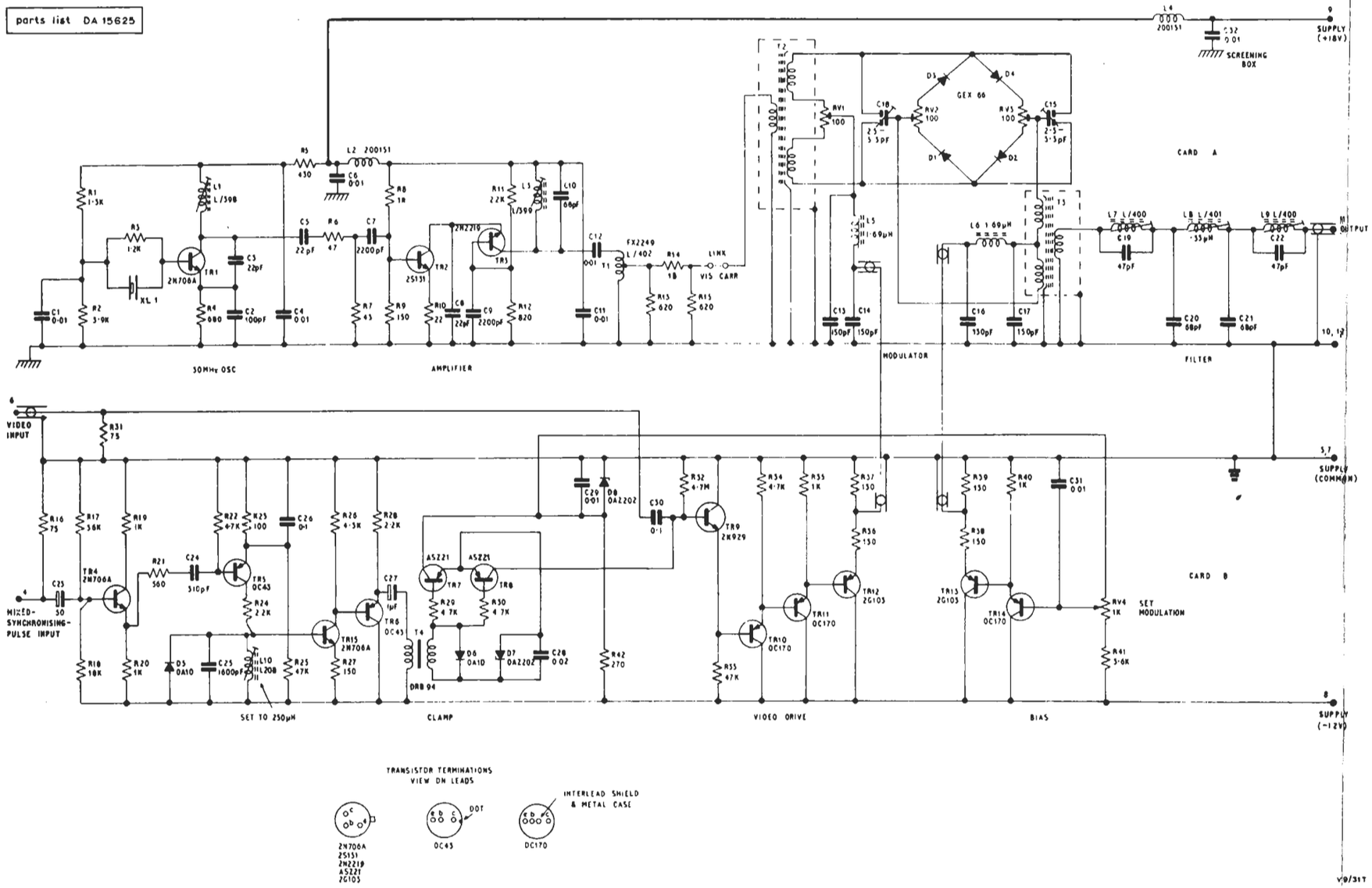


Fig. 18.2 Circuit of the MD2/503

Transistor-electrode Potentials

The following are as measured by an Avo Model-8 test meter, using the lowest usable range of the instrument:

Transistor	*Emitter*	*Collector*
TR1	+7·0 V	+12·0 V
TR2	+1·3 V	+4·0 V
TR3	—	+18 V
TR4	−9·5 V	—
TR5	—	−11·5 V
TR6	—	−0·25 V
TR7	—	−6·2 V
TR8	—	+6·0 V
TR9	−6·8 V	—
TR10	−6·5 V	—
TR11	−6·2 V	—
TR12	−6·0 V	—
TR13	−6·1 V	—
TR14	−6·4 V	Base: −6·6 V

Reference

In addition to the sources already mentioned, Designs Department Technical Memorandum No. 7.108(65) refers to this sub-unit.

DEH 5/67.