TRANSISTOR-OPERATED AUDIO-FREQUENCY TEST APPARATUS

SECTION 1

PROGRAMME METERS: ME12 SERIES

PEAK PROGRAMME METER ME12/4

General Description

Peak Programme Meter ME12/4 is of standard performance but utilises transistors instead of valves. It has printed wiring and is constructed on a CH1/18A chassis for plugging into a PN3/23 panel. The associated indicating instrument, which has the normal type of P.P.M. scale but a left-hand no-current zero, is mounted separately but a meter plug is provided on the front panel for test purposes.

The dimensions are approximately 2 in. wide by 5 in. high by 10 in. deep.

Circuit Description (Fig. 1)

Design Basis

The basic principles of operation are similar to those employed in existing valve peak programme meters and the equipment contains an input amplifier, a rectifier circuit, a logarithmic device and a d.c. output amplifier. In the ME12/4, however, the logarithmic device and the d.c. amplifier are not combined as the transistor equivalent of a variable-mu valve was not available; also a much greater stability of characteristic can be obtained from a balanced linear d.c. amplifier than from one arranged to have an approximately logarithmic response.

Input Amplifier

The input amplifier consists basically of a conventional single-stage push-pull circuit in which each half comprises two transistors connected as a ' Darlington ' or ' super-alpha ' pair.* A pair of transistors thus connected behaves as a single transistor having a current gain factor equal to the product of the gain factors of the separate transistors; in addition, the circuit gives a high input resistance (between the base of transistor 1 and the emitter of transistor 2) which in this instance is about 50 kilohms. The arrangement thus affords a convenient way of obtaining a high gain and high input resistance from two transistors without the complication and phase-shift of interstage coupling components.

Bias currents are supplied from the potential dividers R10/R11 and R12/R13 to the two halves of the stage via T1 secondary windings, and bias stabilisation is obtained in the usual manner by the emitter resistances R14 and R15 decoupled by C1 and C2. The potential dividers are connected between the respective collectors and earth, and therefore also provide balanced sources of signal-frequency voltage feedback which are connected to the respective transistor bases in series with T1 secondary windings. The magnitude of the feedback, about 16 dB, is determined by the resistance (R1 + RV1), the latter forming the *Sensitivity* control. The ganged switches SA1 and SA2 enable the gain to be varied by plus and minus 8 dB about the normal value for convenience in checking the scale shape of the apparatus.

The input impedance is nominally 50 kilohms and the output impedance 180 ohms, built out to 450 ohms by R16.

The open-circuit voltage gain at 1 kc/s is 10·5 dB for normal settings of RV1 and SA.

Logarithmic Rectifier Section

This part of the circuit extends from the secondary winding of transformer T2 to the time-constant capacitor C3. The signal from the input amplifier is full-wave rectified by the bridge MR1-MR4 and the resulting unidirectional pulses are applied to the resistance/rectifier load network shown in the diagram.

The rectifiers MR5, 6 and 7 are non linear diodes; the voltage developed across a diode of this type is approximately proportional to the logarithm of the current through it over a wide range. To use this property directly it would be necessary to provide a very high impedance (i.e., ' constant-current ') source to drive the diodes, but it was found to be impracticable to arrange this with transistors for the frequency range and other requirements of this apparatus with sufficient accuracy. A source of low impedance (approxi-

*See BBC Monograph No. 26, August 1959: 'Transistor Amplifiers for Sound Broadcasting,' by S. D. Berry.

mately 500 ohms) is, therefore, used and the diodes built out into three steps with resistors as shown. The voltage across the network is passed to the time-constant capacitor C3 via MR9 and R19.

To follow the operation of the circuit consider a pulse arriving from the input amplifier. At very low levels all diodes pass a very small current and the resistance of all of them is high. The relationship between the voltage across the network and the input voltage is, therefore, approximately linear. This state continues to around the point 2 on the programme meter, and the *Sensitivity* control RV1 is pre-set to give this reading at the correct input level.

As the input increases the current through MR5 and MR6 in series increases greatly, their resistance falls and the voltage across the network rises proportionally to the logarithm of the input. The first *Law* control RV2 is pre-set to give a meter reading of 4 at the corresponding input level. Below 4 the voltage existing across R17 and RV2 in series is insufficient to cause appreciable current to flow through MR7 and this arm of the network is, therefore, inoperative. As 4 is passed MR7 comes into operation and the logarithmic law is extended to around the meter point 6. The second *Law* control RV3 is pre-set for accurate calibration at 6. The third arm of the network contains MR8, a low impedance diode which in conjunction with R18 limits the meter reading at 7 and beyond.

The capacitor C3 is charged via R19 and MR9 (which prevents discharge of C3 by the charging circuit on the cessation of the pulse) from an impedance consisting of the parallel combination of the amplifier output impedance and the logarithmic network. Since the impedance of the latter varies with the signal the charge time-constant is not truly constant during the charge process; it varies from about 3 milliseconds in low signal conditions to about 2 milliseconds in high signal conditions and has an average value of the standard 2·5 milliseconds. The variation is imperceptible in practice.

The discharge time of C3 is controlled by R20, R21 and the input impedance of the following d.c. amplifier stage to give the required time constant of 1 second.

D.C. Amplifier

Two Darlington pairs of silicon transistors are used in a long-tailed pair bridge arrangement. Due to the low leakage current of silicon transistors and the accurate balance that can be obtained with this circuit the zero drift is very small and the gain very stable for both supply voltage and temperature changes.

The upper arm of one of the bias potential dividers is made variable over a small range to form a *Zero* control.

The signal is applied to both bases of the Darlington pairs in a balanced push-pull manner and the meter with 2 kilohms in series is connected between the two output collectors. The stage should work into a load of 2,600 ohms. With no signal input the bridge is balanced and the meter current is zero. Incoming signals drive the bridge off balance and the meter reads accordingly. The meter, therefore, has a left-hand no-current zero in contrast to the previous patterns of programme meter. Excessive meter deflection on overload is prevented by the sharply limiting action of MR8 in the logarithmic circuit and by the overload characteristics of the d.c. stage.

Several functions are performed by the network connected between the emitters of TR6/TR8 and earth. With R26 and RV4 short-circuited, R25 and R28 would be directly in parallel to give a single resistance forming the normal 'long-tail' of the pair, coupling them together and maintaining the balance of the system. Owing to the push-pull action of the circuit, no feedback would be given in such a condition (except the small amount given by gain differences between the two transistor pairs). With R26 and RV4 open-circuited, R25 and R28 appear each in its separate emitter circuit and give a large feedback to each transistor pair, thus considerably reducing the gain. The *Balance* control RV5 may then serve to adjust small differences between R25 and R28 and between the current gain factors of the two pairs and give an accurate balance to the arrangement. The circuit condition is intermediate between those described above, the *Gain* control RV4 adjusts feedback (magnitude about 4·5 dB) to give the required stage gain, RV5 gives a balance adjustment and the whole network a long-tail coupling between the two halves of the stage.

Meter

The meter differs from the standard instrument* in having a left-hand no-current zero, a full-scale deflection of 1·0 mA with a resistance of 600 ohms and a slightly different scale calibration.

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*Equipment Department Specification ED 1415.

It is intended for mounting on a non-ferrous panel, and the calibration may be upset if this is not adhered to. The scale calibration is given below.

Position	*Scale Division*	*Current mA*
Left-hand end	Zero mark	0
	1	0·10
	2	0·22
	3	0·35
	4	0·51
	5	0·67
	6	0·80
	7	0·93
Right-hand end	F.S.D. mark	1·00

The required load resistance for the d.c. stage is 2,600 ohms. Additional meters, up to a total of four, may be used in series and the series resistance altered accordingly, but it should be noted that only one zero control can be used for the group and this is mounted on the front panel of the ME12/4.

Performance

Complete lining-up adjustments are carried out on initial test before the apparatus is issued and the performance should then be as indicated below.

Calibration

The calibration error at any of the points 2 to 6 inclusive on the indicating meter should not exceed 0·25 dB, and at points 1 and 7 should not exceed 0·5 dB.

Frequency Response

With a constant input voltage varied over the range 40 c/s to 15 kc/s and adjusted to give a meter reading of 4 at 1 kc/s the meter reading should not alter by more than 0·3 dB.

Gain Switch

The switch SA when operated to the +8 dB and −8 dB positions should cause a corresponding change of meter reading to within ±0·3 dB.

Input Impedance

50 kΩ ±10 per cent at 1 kc/s.

Time Constants

The charge and discharge time-constants are 2·5 milliseconds and 1 second respectively as in previous programme meters, and the reading given by the normal flick test should fall within the limits of +0·5 −1 dB about the mark 4. R19 should be adjusted or shorted out if necessary to obtain this performance.

The interval between marks 7 and 1 is 24 dB, not 26 dB as with previous valve apparatus, so the time taken for a fall over this interval should be 2·77 seconds for a 1 second time constant. The time observed should be within 2·5 and 3·2 seconds.

Operation and Maintenance Adjustments

After the apparatus has been correctly lined up before issue only occasional zero adjustment and a routine check of sensitivity and law will be needed until a major overhaul is found to be necessary. These may be carried out quickly as follows:

1. Adjust zero.
2. Apply 1-kc/s accurate zero-level tone to the input, operate switch SA to −8 and adjust the *Sensitivity* control RV1 to give a meter reading of 2.
3. Switch SA to 0 and adjust *Law 1* to give a meter reading of 4.
4. Switch SA to +8 and adjust *Law 2* to give a meter reading of 6.
5. Repeat the last two steps which are to a small degree interdependent.

The Gain and Balance controls must not be disturbed unless a complete re-lining up is done.

Note that in contrast to previous practice with valve P.P.M.s the sensitivity adjustment is made at reading 2. The sensitivity control should not be used to line up at 4.

The characteristics of the ME12/4 should be stable and re-adjustment of controls rarely necessary. Needless re-adjustment may be caused by incorrect levels of test tone. The tone level should be zero dB *at the apparatus input terminals.*

Fault Finding

The following emitter/common positive voltages, measured with an Avometer 8 with no input signal, are given to assist fault-finding.

TR2	TR4	TR6	TR7
14·5 V	14·5 V	12 V	12 V

The voltages of the pairs TR2, TR4 and also TR6, TR7, should be equal within 10 per cent. They depend to a small extent on the setting of the controls.

The total current should be 85 ±5 mA from a 24-volt d.c. supply.

Complete Lining-up Procedure

General

Should it become necessary to carry out a complete re-lining up of the apparatus the procedure given below should be followed and final adjustments made after the apparatus has been switched on for at least ten minutes so that transistor junctions have reached a steady temperature. Switch SA should be at 0 unless otherwise specified.

Check operation to see that the circuit behaves properly and no obvious faults exist; it should be possible to zero the meter approximately with the *Zero* control, and zero-level tone applied should give a meter deflection somewhere around mid-scale.

Input Amplifier Gain

Turn the two *Law* controls fully clockwise. Apply 1-kc/s tone at a level of −8 ±0·2 dB to the input terminals. With a high impedance amplifier detector compare voltage at input and output (red and violet leads of T2). Adjust the *Sensitivity* control RV1 to make the voltage gain 10·5±0·2 dB. Remove tone from input.

D.C. Amplifier Balance and Gain

Connect the base terminal of TR5 to the base terminal of TR7 with a clip connector. Adjust the *Balance* control RV5 to give meter zero. Remove the clip connector. Restore meter zero with the external *Zero* control.

Re-apply the 1-kc/s tone at −8 ±0·2 dB at the input and adjust the *Gain* control RV4 to make the meter read 2.

The *Balance* and *Gain* controls are now set and should not be altered. Any further adjustments necessary to zero the meter should be made with the *Zero* control, and adjustment to gain with the *Sensitivity* control.

Law Adjustment

Increase level of 1-kc/s tone to make it zero level to the greatest accuracy available (within ±0·2 dB) and adjust *Law 1* control to give a meter reading of 4.

Increase input level another 8 dB and adjust *Law 2* to give a meter reading of 6.

The last two adjustments are inter-dependent to a small degree so they should be repeated, and small re-adjustments made.

Intermediate and extreme points should be checked in the obvious manner. Note that the interval between 2 and 1 is 4 dB.

Meter Slugging Circuit

Where a slowed-up external meter response is required to facilitate checking by telephone of the correspondence between meter readings at distantly separated locations, the arrangement shown in Fig. 1.1 is used.

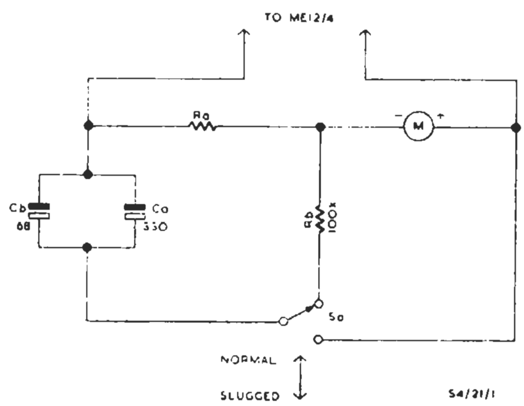

Fig. 1.1. Meter Slugging Circuit

Operation of the switch connects a 400-microfarad capacitor (Ca + Cb) across the meter and its series resistor Ra, to give a time constant of about 0·65 second on both charge and discharge; there will therefore be a large effect on the rise time of the meter, but little on the fall time, and the meter will indicate average peaks. The circuit has been arranged to give as nearly as possible the same effect as that used in the MNA/3 (Instruction

S.3 Section 21), and the two types of programme meter may be compared in the slugged condition with satisfactory accuracy.

When two or more meters in series are used with the ME12/4, the value of Ra (which is 2 kilohms for a single meter) is determined as described earlier to give a total load resistance of 2,600 ohms, and all the meters will be slugged; it is not possible to use some slugged and others working normally at the same time.

The 400-microfarad capacitor discharges through Rb when the switch is returned to its normal position.

The additional components required are:

Rb Erie Type N1 or 109, 2%.
Ca Tantalum electrolytic, 10%, 6 V.
Cb Tantalum electrolytic, 10%, 6 V.
Sa Single-pole change-over type.

The capacitors may be 'Tansitor' Type S of Thorne Electrical Industries, Enfield, Middlesex, Cat. Nos. S330-6C4KI and S68-6C3KI, or a similar type such as Plessey Type S.

W.G. 10/62

COMPONENT TABLE: FIG. 1

Comp.	Loc.	Type	Tolerance per cent	Comp.	Loc.	Type	Tolerance per cent
C1	E6	Plessey CE2087		R14	E4	Painton MVIA	5
C2	E3	U.C.C. SC517/8LS		R15	E6	Painton MVIA	5
C3	L5	Plessey S	10	R16	G5	Erie N1 0·1W	2
				R17	J4	Erie N1 0·1W	2
				R18	K4	Erie N1 0·1W	2
MR1	H4	Mullard OA10		R19	L3	Erie N1 0·1W	2
MR2	H5	Mullard OA10		R20	M3	Erie N1 0·1W	2
MR3	H4	Mullard OA10		R21	M6	Erie N1 0·1W	2
MR4	H5	Mullard OA10		R22	M2	Erie N1 0·1W	2
MR5	J5	G.E.C. SX640		R23	M6	Erie N1 0·1W	2
MR6	J5	G.E.C. SX640		R24	N2	Erie N1 0·1W	2
MR7	J5	G.E.C. SX640		R25	N8	Erie N1 0·1W	2
MR8	K4	Mullard OA10		R26	O7	Erie N1 0·1W	2
MR9	K3	G.E.C. SX641		R27	P2	Erie N1 0·1W	2
				R28	P8	Erie N1 0·1W	2
				R29	Q1	Erie N1 0·1W	2
R1	C4	Erie N1 0·1W	2	R30	Q6	Erie N1 0·1W	2
R2	C1	Erie N1 0·1W	2				
R3	C2	Erie N1 0·1W	2				
R4	C3	Erie N1 0·1W	2	RV1	C5	Painton 316525	
R5	C4	Erie N1 0·1W	2	RV2	J5	Painton 316525	
R6	C6	Erie N1 0·1W	2	RV3	J4	Painton 316525	
R7	C7	Erie N1 0·1W	2	RV4	O7	Painton 316525	
R8	C8	Erie N1 0·1W	2	RV5	O8	Painton 316525	
R9	C8	Erie N1 0·1W	2	RV6	Q3	Painton 316525	
R10	D3	Erie N1 0·1W	2				
R11	D4	Erie N1 0·1W	2				
R12	D6	Erie N1 0·1W	2	T1	B5		
R13	D7	Erie N1 0·1W	2	T2	F5		

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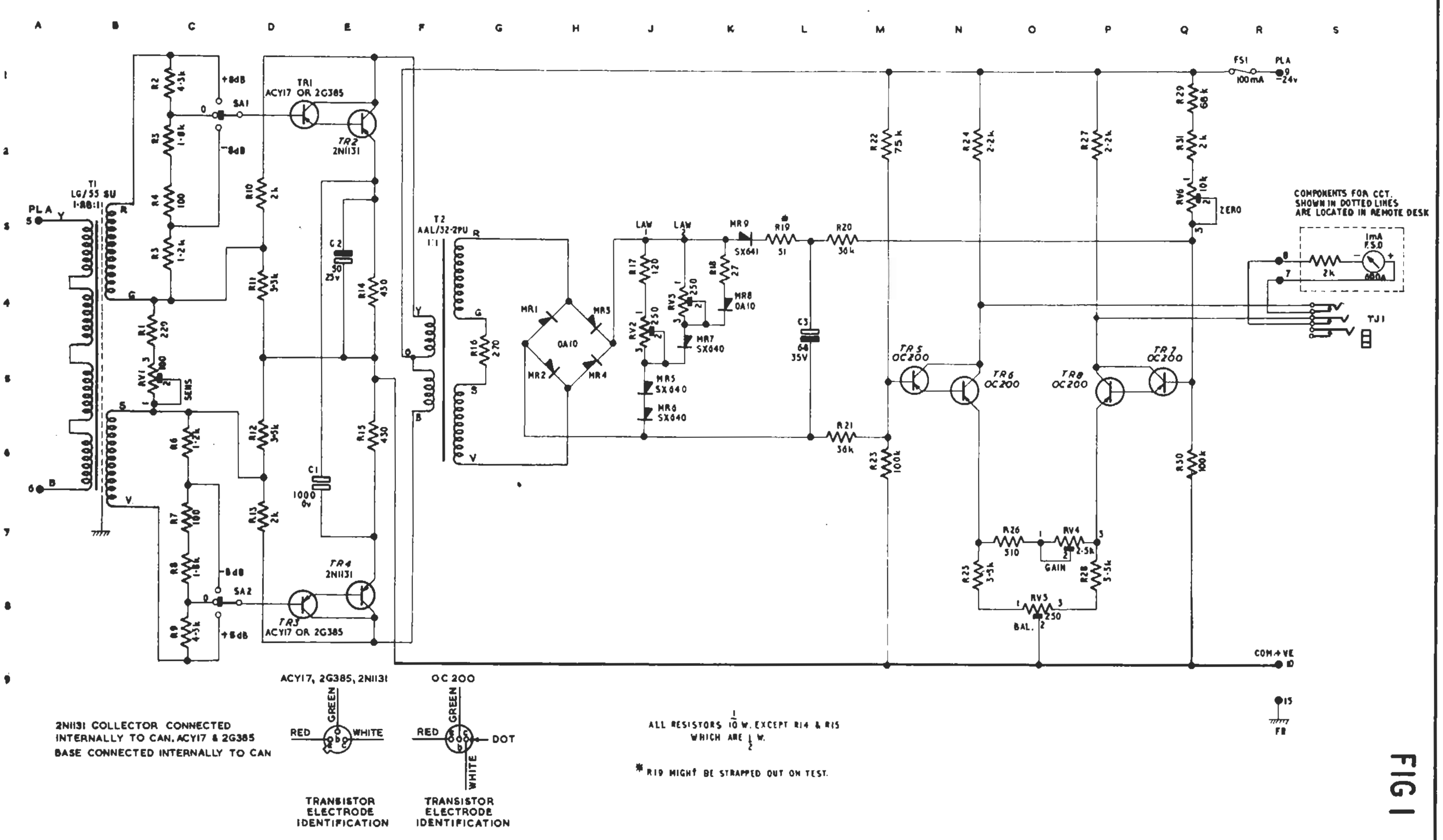

2N1131 COLLECTOR CONNECTED INTERNALLY TO CAN. ACY17 & 2G385 BASE CONNECTED INTERNALLY TO CAN

TRANSISTOR ELECTRODE IDENTIFICATION

TRANSISTOR ELECTRODE IDENTIFICATION

ALL RESISTORS $\frac{1}{10}$ W. EXCEPT R14 & R15 WHICH ARE $\frac{1}{2}$ W.

* R19 MIGHT BE STRAPPED OUT ON TEST.

PROGRAMME METER ME12/4 : CIRCUIT

FIG 1