FIELD SYNC DETECTOR UNITS MN1/505 AND MN1/505A

Introduction

The MN1/505 accepts a composite video signal and energises a relay if field-sync pulses are included in the input signal: two sets of relay changeover contacts are provided as output circuits. The relay energises 2 to 5 seconds after field sync pulses are applied and releases 12 to 15 seconds after they are removed.

The MN1/505 is a 625-line-standard version with index-peg positions 9 and 27. The MN1/505A is a 405-line-standard version with index-peg positions 9 and 29. Both units are constructed on a CH1/12A chassis.

Circuit Description

A simplified block diagram of the unit is given in Fig. 1, a circuit diagram in Fig. 2 and waveforms in Fig. 3.

The input signal is fed via an emitter-follower, a subcarrier rejection network and a further emitter-follower, to a 14-dB three-stage negative-feedback amplifier. During sync pulses the output of this amplifier is clamped at the base of TR6.

The sync-pulse mean-level detector provides a potential which is proportional to the mean level of the input syncs. This potential is fed to the TR14 side of the TR13-TR14 long-tailed pair to determine the cut-off point of the stage.

The field pulse output from the UN16/523 card is amplified and clipped by the TR13-TR14 long-tailed pair stage and is then applied to a charge-storage stage consisting of TR15 and TR16.

Transistors TR15 and TR16 are normally cut off

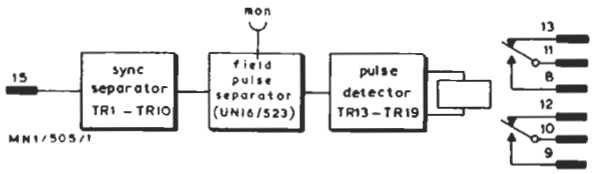

Fig.1 Block Diagram of the MNI/505

Positive-going signals at the emitter of transistor TR6 reverse-bias diode D2 and this removes most of any picture signal. The clipped signal is fed via emitter-followers TR7 and TR8 to a standard sync-separator circuit. The signal at the base of transistor TR9 is d.c.-restored via the base-emitter junction diode. The transistor is cut off, therefore, except during sync pulses when positive-going pulses are developed at the collector.

Diode D4 limits the positive excursion of the positive-going sync pulses fed to transistor TR10. This transistor produces positive-going clamping pulses which are fed to the base of TR6.

Positive-going sync pulses from TR9 are fed to a UN16/523 printed-wiring card[1] where they are applied to a field-pulse separator circuit and a sync-pulse mean-level detector circuit.

The field pulse separator consists of a differentiator-integrator combination; it produces a positive-going field-pulse with a steep front edge and a flat top, as shown in Fig. 3. The front edge is coincident in time with the trailing edge of the first broad pulse in the input signal. The field-pulse separator output is fed to the TR13 side of a long-tailed pair comprising TR13 and TR14.

ıncreasing the charge on capacitors C12 and C13 by a small amount in each field.

If the input field-sync pulses are removed, capacitors C12 and C13 discharge through resistor R38. The value of this resistor controls the relay release delay time and the value of resistor R39 controls the relay-energising delay time.

The voltage fed to the base of transistor TR17 is amplified and limited in transistor TR18. The emitter potential of transistor TR19 is biased by diode D6 to ensure that this transistor is cut off when there are no input field sync pulses.

by the voltage across zener diode D5. This voltage is shared between them by resistors R40 and R41. Positive-going pulses at the base of transistor TR15 cause both TR15 and TR16 to conduct, thereby

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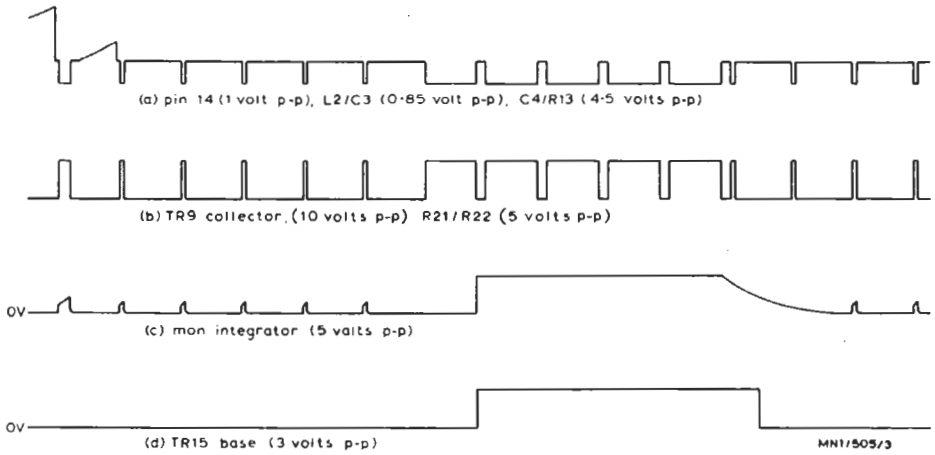
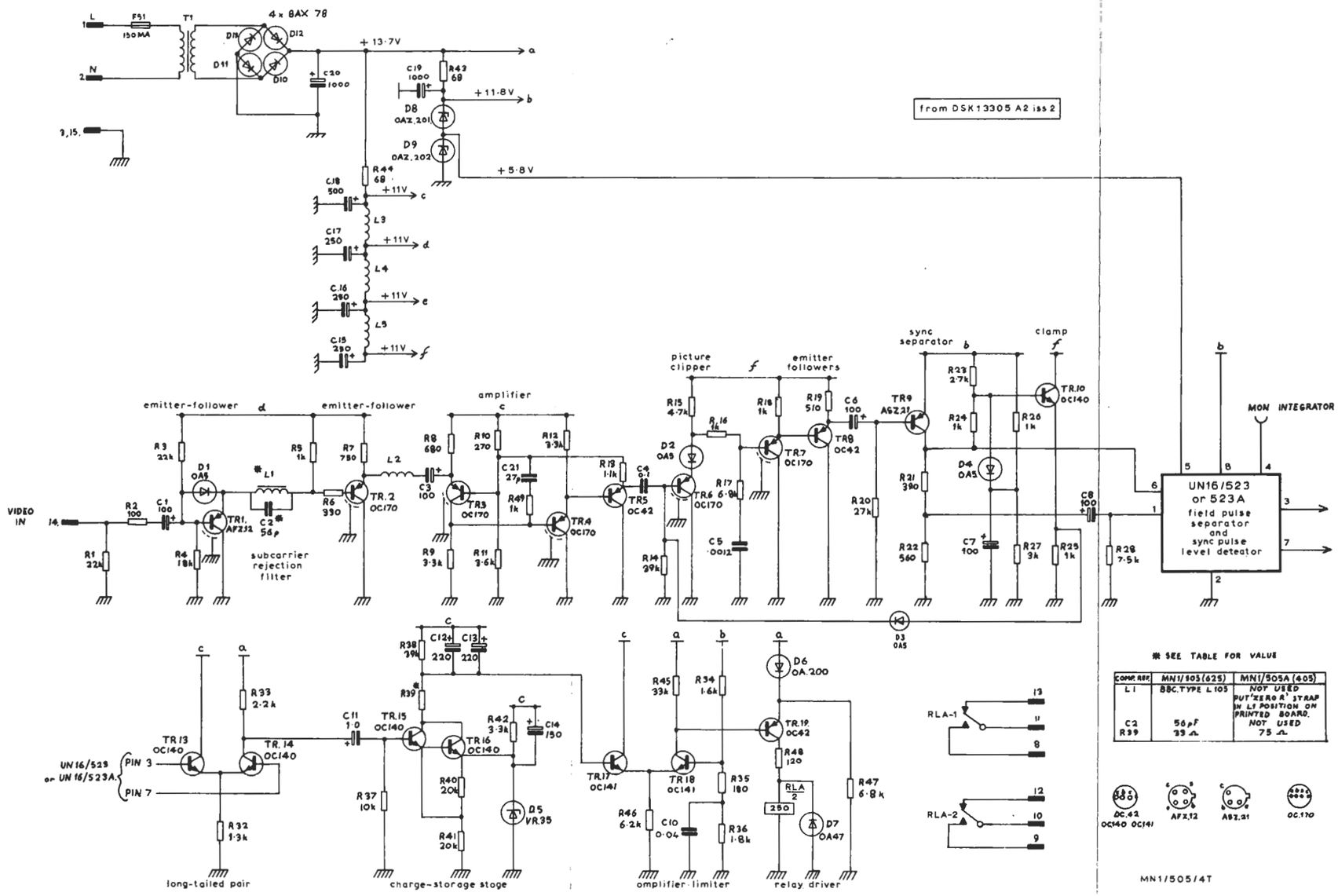


Fig.3 Waveforms in the MNI/505



COMP. REF.	MN1/505 (625)	MN1/505A (405)
L1	BBC. TYPE L.105	NOT USED PUT 'ZERO Ω' STRAP IN LF POSITION ON PRINTED BOARD.
C2	56 pF	NOT USED
R39	33 Ω	75 Ω

Fig.2 Circuit of the MN1/505

Maintenance

Apply a composite video signal to the input of the unit and check that the relay operates within 2 to 5 seconds. Remove the input signal and check that the relay releases within 12 to 15 seconds.

Table 1 gives typical voltages at various points in the circuit for no signal input. If faults within the clamp feedback loop are difficult to locate:

(a) Open the loop by disconnecting the base of transistor TR10 from the circuit and connecting it to the junction of resistors R26 and R27.

(b) Check that diode D3 acts as a d.c. restorer and holds the sync pulse tips at about +8·5V (if not the fault lies between D3 and the junction of R26 and R27).

(c) Check waveforms and voltages between transistors TR6 and TR9.

Note: The clamp circuit has appreciable gain; great care must be taken when checking potentials as a short-circuited transistor terminal could cause the destruction of the transistor.

Table 1
MN1/505 or 505A

	emitter	*base*	*collector*
TR1	5·3	4·9	0
TR2	5·6	5.3	0
TR3	9·8	9·6	5·9
TR4	6·2	5·9	0
TR5	6·3	6·2	0
TR6	9·8	9·5	0
TR7	10·2	9·9	0
TR8	10·3	10·2	0
TR9	11·3	10·8	11
TR10	9·7	9·9	11
TR13	8·2	0·2	11
TR14	8·2	8·5	8·2
TR15	1·5	0	10·3
TR16	3·0	1·5	10·3
TR17	10·2	10	11
TR18	10·2	7	12·8
TR19	13	12·8	0

UN16/523 or 523A

TR1	0·7	0	0
TR2	5·8	5·8	0·7
TR3	0·1	0·7	5·8
TR4	7·9	6·5	11·3
TR5	8·5	9·1	11.3

Alignment

Equipment Required

Oscilloscope	Tektronix Type 515A (or equivalent)
Avometer	Model 8
Attenuators	0 to 9 dB and 0 to 90 dB, 75 ohms impedance
Test Waveform	composite video at standard level (preferably mixed-syncs and white bars)
Termination	75 ohms

Procedure

1. Terminate the input of the unit in 75 ohms and apply the test signal to the input. Turn the adjusting screw of variable resistor R10 (on the UN16/523 board) fully clockwise.
2. Check that a field pulse with a p-p amplitude of about 5 V is present at the *Mon. Integrator* monitor point. Use this pulse to trigger the oscilloscope.
3. Monitor the junction of C11 and R37. Check that a field pulse with an amplitude of between 2 V p-p and 5 V p-p is present.
4. Remove the 75-ohm input termination. Turn the adjusting screw of variable resistor R10 slowly anticlockwise until the pulse at C11 is on the point of breaking up or vanishing. (Note that the relay may *hunt* in this condition.)
5. Replace the input termination. Allow a few seconds recovery time and check that a well-defined pulse is present at C11. If the displayed pulse shows signs of breaking up, adjust R10.
6. Progressively reduce the level of the input signal. The pulse should begin to break up at an attenuator setting of about −9 dB and should disappear at about −13 dB. Check that the relay releases when the pulse disappears.
   Note that the relay may *hunt* in this condition.
   If a test waveform other than that recommended is used, the levels at which the pulse breaks up and vanishes will differ from those given above. These levels depend on the picture content of the waveform.
7. Check that for further reductions of signal level (including the no signal input condition) the relay stays released. Any spurious pulses which tend to re-energise the relay must be suppressed by slight re-adjustment of R10.
8. Restore the level of the input signal to 1 V p-p (0-dB setting on attenuator). Allow several seconds for the circuit to stabilise. Remove the input signal and check that the relay releases in from 12 to 15 seconds. Restore the signal and check that the relay energises within 2 to 5 seconds.

References

1. Field Pulse Separators UN16/523 (625 lines) and UN16/523A (405 lines).

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