S.I.S. SYSTEM MONITOR MN1/7

Introduction

The MN1/7 forms part of a sound-in-syncs decoder[1] and is used in conjunction with a UN20/527 Error Detection Unit to provide visual indications of a number of possible fault conditions. The MN1/7 contains also an integrator circuit which sums all fault conditions and operates an external alarm in the event of continuous or recurrent faults.

The unit is constructed on a CH1/43 chassis with index-peg positions 1, 3 and 7. Power supplies at +5·2V and −5·2V are required.

General Specification

Fault Indication Inputs

Hold
Pilot Tone
Timing Generator Unlock
L.F. Overswing
Sync Fail

Input Signals are normally at logic level 0 (TTL), but change to logic level 1 when a fault is present.

Reset Input — normally at logic level 1 (TTL) but changes to 0 when a reset pulse is applied.

Outputs

Set — normally logic level 0 (TTL), but changed to 1 if one or more faults are present.

Relay Output — changeover contacts (any external relays driven from these contacts must be adequately suppressed with diodes).

Power Requirements — 60 mA at +5·2V
400 mA at −5·2V

TTL Logic Levels — logic level 1, about +3·5V (+5V max.)
logic level 0, about 0V (+0·4V max.)

Circuit Description

A block diagram of the MN1/7 is given in Fig. 1 and a circuit diagram in Fig. 2.

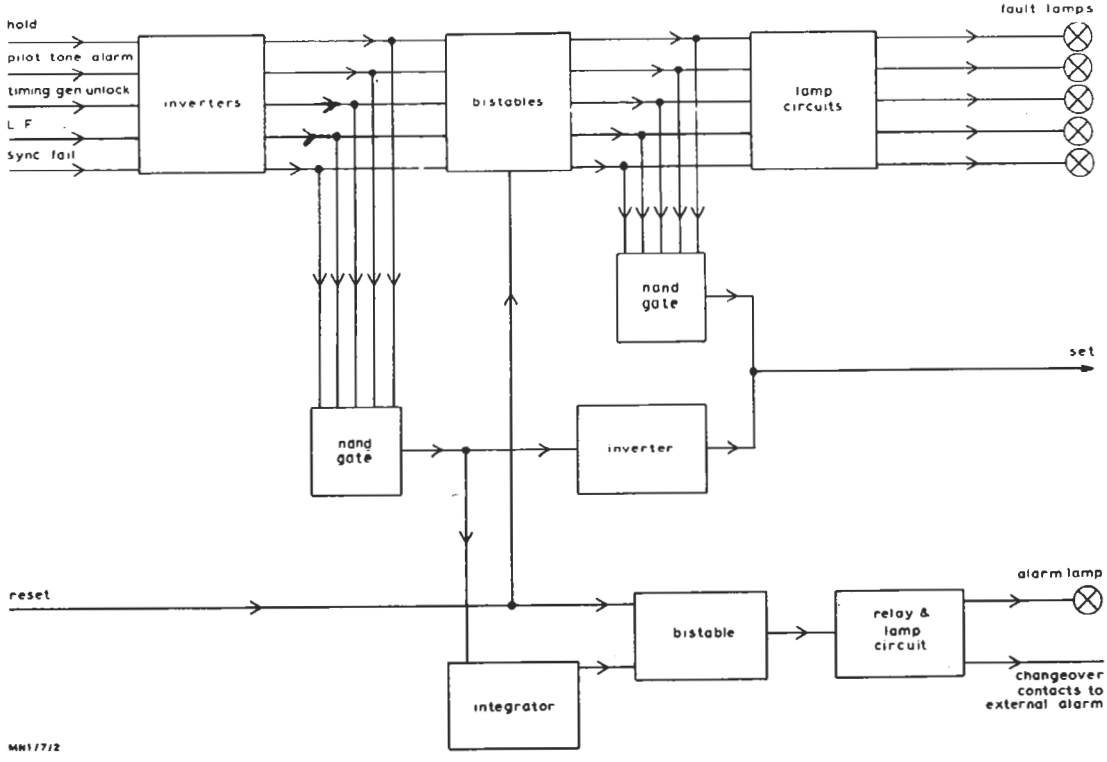

Fig. 1 Simplified Block Diagram of the S.i.S. Monitor MN1/7

Lamp Operation

The five fault-signal inputs to the unit are supplied, via inverters, to identical lamp-operating circuits. The operation of the *Hold* circuit is described below.

When a Reset pulse has been applied to the unit the logic states in the *Hold* lamp-operation circuit are as shown in Table 1.

TABLE 1

IC1a		*IC2a and IC2b*			
pin 5	pin 6	pin 1	pins 2 and 6	pins 3 and 4	pin 5 (reset)
0	1	1	1	0	1

When the output of IC2b is at 1, transistors TR1 and TR2 are both cut off and so the *Hold* lamp is not illuminated.

When the *Hold* input changes to logic 1 (fault condition) the bistable stage formed by IC2 changes state, whereupon transistors TR1 and TR2 conduct and the *Hold* lamp is illuminated.

Reset System

The timer which governs the generation of Reset pulses is located in the associated UN20/537 unit, but it is controlled by the *Set* output of the MN1/7. If the *Set* output remains at logic 1 for a continuous period of five seconds a Reset pulse is generated and, as a result, the signal present at the *Reset* input (PLA 6) changes from logic 1 to logic 0 for a period of approximately 200 ns. The *Set* logic circuit is arranged so that the *Set* output becomes logic 1 if a lamp is illuminated and a fault condition is not present. It follows, therefore, that the appropriate lamp, or lamps, will remain illuminated for five seconds after the cessation of a fault.

The *Set* logic function is achieved by monitoring the five fault-signal inputs to detect the presence of a fault signal and by monitoring the five bistable elements contained in integrated circuits IC2 to IC4 to determine when a lamp is illuminated. The monitoring is carried out by NAND gates IC5a (for the input signals) and IC5b (for the bistables). The outputs of the two gates are combined at the junction of IC5b (pin 6) and inverter stage IC1b (pin 1), the combination acts as an AND gate and a logic 1 is applied to the *Set* output only when both IC5b (pin 6) and IC1a (pin 1) are at logic 1. Table 2 shows the logic states that precede and follow a *Sync-fail* fault; logic tables for the other fault conditions can be derived in a similar manner.

Integrator

Any fault signal changes the output of IC5a to logic 1. Thus IC5a provides a summation of all fault signals. This fault information is applied via R24 to the fault-signal integrator circuit. The operation of the integrator both for continuous faults and for intermittent faults is detailed below.

(a) Continuous Faults If a steady fault occurs, transistors TR11 and TR12 are cut off, and capacitor C4 charges through R24, D2 and R27, the charge time being determined principally by R27. When C4 has charged to about +2V, unijunction transistor TR14 conducts and C4 discharges into resistors R30 and R31. The narrow pulse thus produced turns on TR16 and causes a logic 0 to be applied to pin 13 of the bistable device formed by IC4c. On receipt of this pulse the bistable changes state and logic 1 appears at pin 11. From pin 11 the logic 1 pulse is applied to TR17 which is cut off; TR18 is cut off also, relay RLA is de-energised, TR19 cuts off and the alarm lamp lights.

A Reset pulse is applied to pin 9 of IC4a when the fault clears. On receipt of this pulse, IC4a changes state and a logic 0 appears at pin 11. Transistors TR17 and TR18 now conduct, relay RLA is energised, TR19 is cut off and the alarm light goes out. The contacts of RLA are wired to a connector at the rear of the decoder chassis. Note that any

TABLE 2

State of Circuit	*IC5a*			*IC5b*			*IC1b*	*Set*
	pins 2–5	*pin 1*	*pin 6*	*pins 10–13*	*pin 9*	*pin 8 AND pin 2*		*PLA 7*
Normal	1	1	0	1	1	0	(1)	0
Fault Present	1	0	1	1	0	(1)	0	0
Fault Cleared	1	1	0	1	0	1	1	1
5s later (normal)	1	1	0	1	1	0	(1)	0

external relays operated by these contacts must be adequately suppressed by diodes.

The unit has been designed in such a way that if any of the +24V, +12V, −12V or +5V decoder power supplies fail, RLA de-energises and the alarm lamp lights. If the −5V supply fails, RLA releases but the alarm lamp does not light.

(b) Intermittent Faults The integrator responds to intermittent faults which last for a quarter of a second or more and the alarm is energised if approximately 20 faults occur within 30 seconds.

After each intermittent fault signal TR11 conducts again and the positive-going edge of the signal developed at its collector is coupled via C3 to the emitter of TR13. As a result TR13 conducts momentarily and transfers charge from C3 to C4; therefore a rapid succession of faults causes the potential on C4 to increase in a series of steps until, if sufficient faults occur within the specified period, TR14 is triggered and the alarm is energised. The discharge time-constant of C4 is determined by the sum of R26 and R27 and is about five times as long as the normal charge time; thus the integrator can store, for a limited period, information relating to previous faults.

Unijunction transistor TR15 is a relaxation oscillator and its function is to improve the sensitivity of TR14. The negative-going pulses developed at the emitter of TR15 are fed to the upper base of TR14 where they momentarily reduce the voltage; if this reduction forces the base voltage below the emitter voltage, TR14 conducts.

Maintenance

To locate faults in lamp circuits, insert the MN1/7 unit in an operative decoder and then remove from the decoder the associated UN20/527 Error Detection Unit. If the MN1/7 is functioning correctly all the individual fault lamps on it will light up at once and the alarm will operate after about 3 seconds. Replace the UN20/527 in the decoder and check that all lights on the MN1/7 are extinguished after about 5 seconds.

To check individual circuits in the MN1/7, remove the UN20/527 unit from the decoder and replace it with a 25-way ISEP connector which is wired so that the fault signal outputs can be connected to 0V by means of switches. A fault signal on any line can be simulated by opening the appropriate switch.

References to Typical Associated Equipment

1. Sound-in-syncs Decoder CD3M/504.

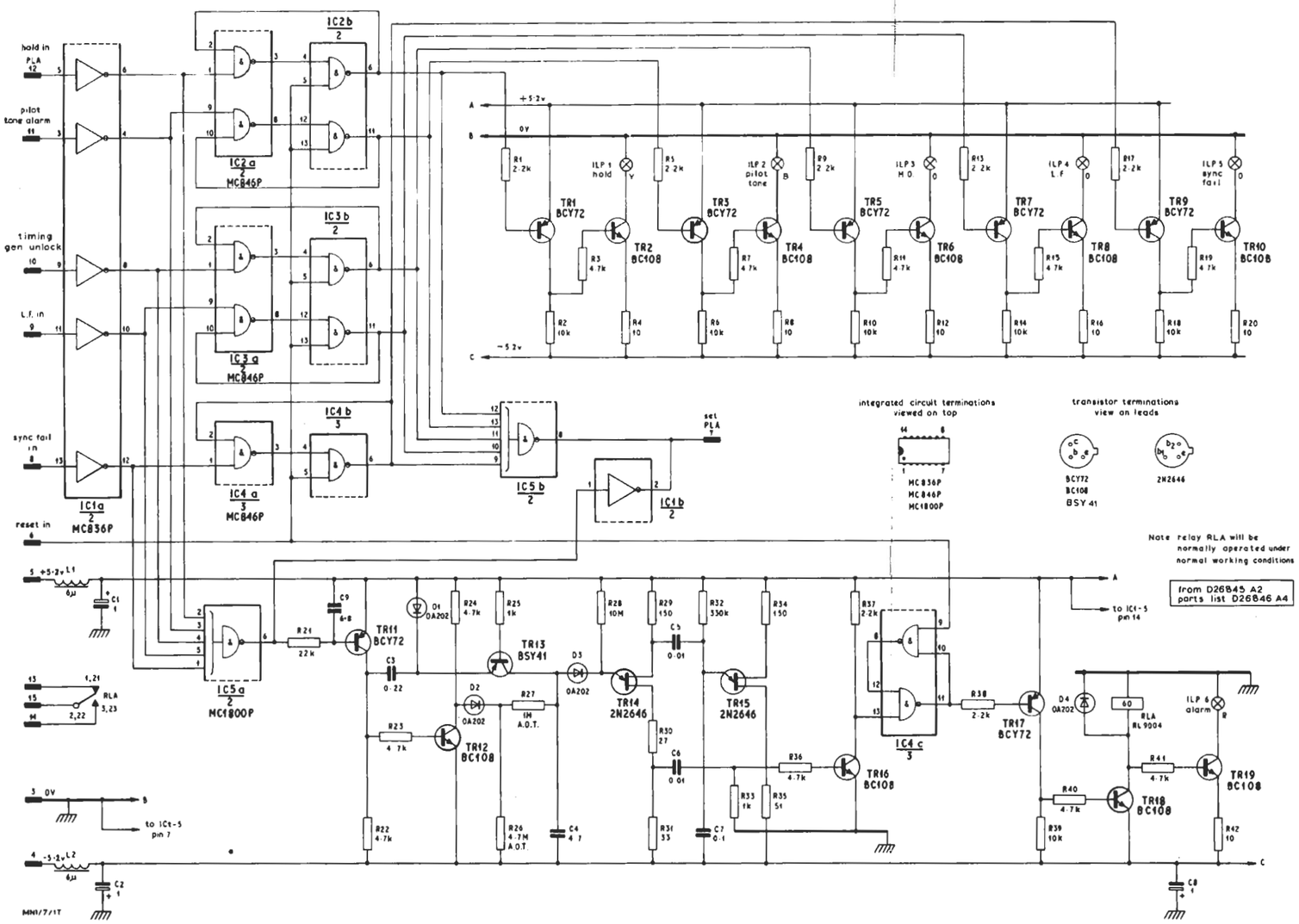

Fig. 2 Circuit of the S.i.S. Monitor MN1/7