SYNC MONITOR MN2/511

Introduction

The MN2/511 compares separated synchronising pulses and colour bursts with reference signals. One +12V output and one independent relay-switched output is provided for each of the input conditions listed (see also Fig. 1):

Separated sync pulses present	*Pulses*
Synchronous with reference syncs	*Timed*
Separated colour bursts present	*Colour*
Phased relative to reference subcarrier	*Phased*

An output at 0V is also available to mute the burst output from an associated Sync Separator[1] when it is below the acceptable level.

The MN2/511 will operate on 405-line monochrome, 525-line NTSC and 625-line PAL standards without any switching.

The monitor is constructed on two printed wiring boards accommodated in a modified CH1/26A chassis (having two 15-way connectors) using index-peg position 12. The front panel carries four lamps indicating each of the conditions listed above.

General Specification

Input Signal Amplitudes from UN1/589

Mixed Syncs	2V p-p
Colour Bursts	0·3V p-p

Reference Signal Amplitudes

Mixed Syncs	2V p-p ±3 dB timed 225ns later than input to UN1/589
Subcarrier	1V p-p in lagging phase quadrature with mean burst-phase at input to sync separator
PAL Squarewave	1V p-p

Input Impedances

Separated Mixed Syncs	About 6·5 kilohms
Separated Colour Burst	High impedance bridging
Reference Mixed Syncs	About 10 kilohms
Reference Sub-carrier	High impedance bridging
Reference PAL Squarewave	High impedance bridging

Outputs	(a) Four independent relay changeover contacts (b) Four +12V 'crash d.c.' outputs at a maximum total load of 20mA when the circuit is not satisfied, i.e. no pulses; not timed; etc. (c) 0V d.c. burst-muting output
Operating Levels	
Pulses	No indication if line-rate information is more than 10 dB below standard level
Timed	Lock in for a timing error of ±400ns Hold in for a timing error of ±600ns
Colour	Lock in at −6 dB burst amplitude w.r.t. 0·3V p-p Hold in to −7 dB burst amplitude w.r.t. 0·3V p-p
Phased	Lock in at ±10° phase error Hold in for ±12° phase error
Operating Standards	405-line Monochrome 525-line NTSC 625-line PAL
Power Supplies	+12V and −5·5V d.c. approx. (supplied from UN1/589) 3V a.c. at 400mA max. for lamps
Operating Temperature	15°–45° C.
Weight	1·25 kg. (2¾ lb.)

Circuit Description

A block diagram of the MN2/511 is given in Fig. 1. The circuit diagram is given in Fig. 2 on page 5. This circuit description is based on 625-line PAL signals; operation on other standards is discussed later. The presence and relative timing of the syncs and bursts are analysed by the MN2/511 in four stages:

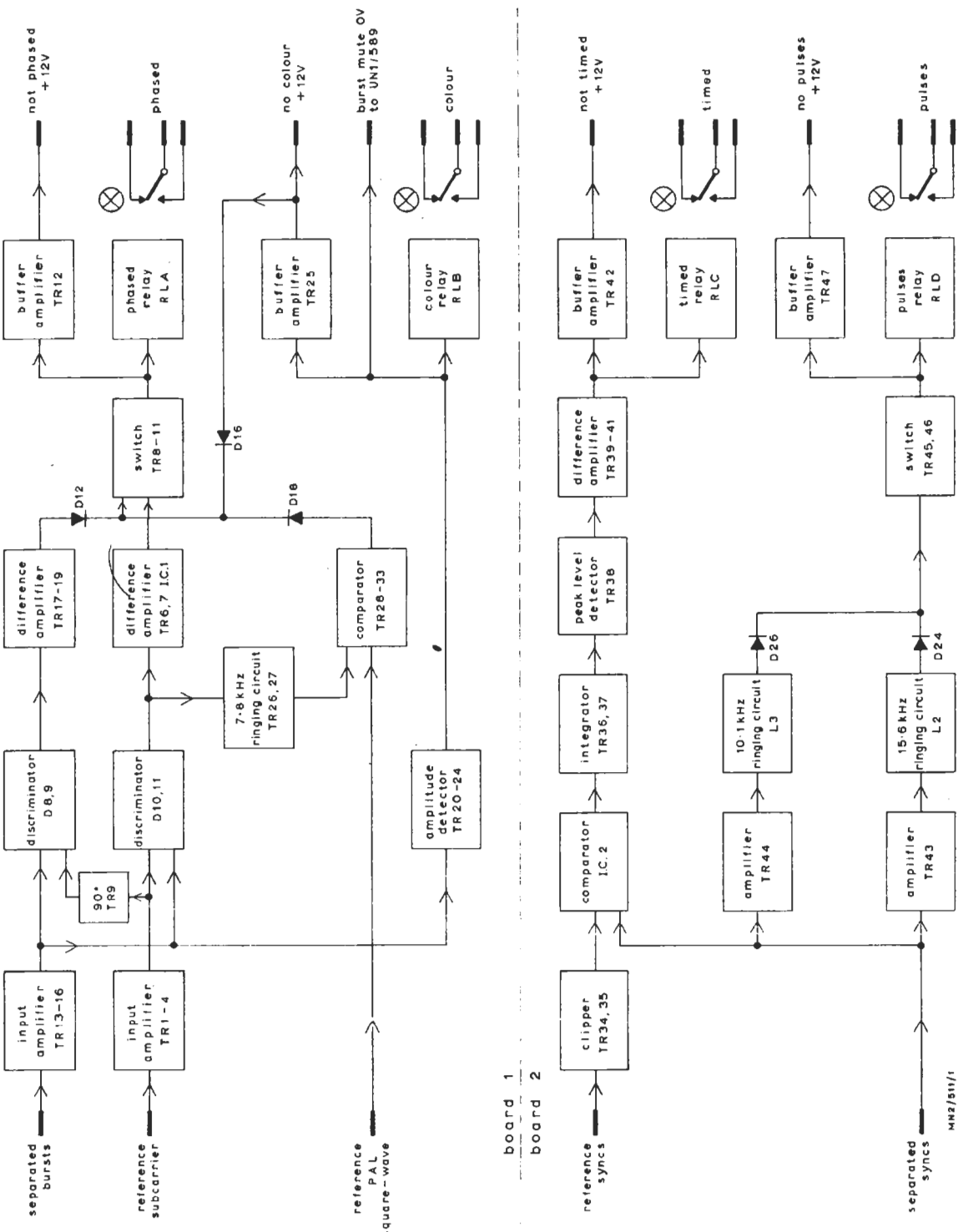

Fig.1 Block Diagram of the Sync Monitor MN2/511

(a) *Pulses.* The pulses indicator must be able to detect signals having a line-frequency of either 10·125kHz (405-lines) or approximately 15·7kHz (525-lines and 625-lines). The separated syncs from the UN1/589 are therefore examined in parallel by two tuned circuits (L3, C43 for 405-line signals; L2, C41 for 525- and 625-line signals) each of which is preceded by a single stage common-emitter amplifier. The line-frequency sinewave output is detected by one of the diodes D24 or D26 at the input to the *Pulses* indicator switch TR45–46 which drives relay RLD. The signal level at which the switch gives an output is determined by the time-constant R136, C44 and by the d.c. voltage required to forward bias TR45.

(b) *Timed.* Reference syncs are applied to a long-tailed-pair clipper TR34–35 the output from which is fed to one input of IC2, the timing comparator. The second input is IC2 is fed with separated syncs.

If the separated syncs are not coincident with reference syncs then positive error pulses are generated at the junction D19–D20. The error signal is a double pulse; the duration of the first is proportional to the timing error between leading edges of separated and reference syncs. Similarly, the second pulse has a duration proportional to the timing error between trailing edges. These error pulses are integrated by C37, R112 and the negative peak level of the resulting sawtooth waveform detected in TR38. When the detected output passes the threshold trigger-level of the emitter-coupled backlash pair TR39–40, the first stage is turned off and the second on. The timed indicator switch TR41 is turned off by TR39, causing relay RLC to be de-energised and declare a not-timed output.

If the separated and reference syncs are timed to within ±400ns, TR39 in the backlash pair remains turned on. Switch TR41 is therefore also turned on to energise RLC which indicates a *Timed* signal.

The stability of this indication is dependent on the biasing of the integrator TR37 and backlash pair TR39–40. Transistor TR36 is biased to provide the required reference potential, its emitter being used as a low impedance voltage source.

(c) *Colour.* Separated bursts are processed by a three-stage input amplifier TR13–16 in which a.c. bootstrap feedback is applied over the first stage to increase input impedance and d.c. negative feedback is applied over the last two stages to decrease the output impedance. The amplified bursts are detected by TR20 and the output waveform is integrated by R61, C26–C49. The level-sensitive detector TR21–22 couples directly to the colour indicator switch TR23–24 which operates the *Colour* relay RLB and provides a burst muting output for use with an associated Sync Separator.

(d) *Phased.* This circuit will declare a *Phased* output if each one of these criteria is satisfied:

Colour indication is present
Burst phase swing satisfies the PAL sequence
Burst is not 180° out of phase
Error between mean burst phase and reference subcarrier is within the Operating Tolerance

The circuit operates in a logical mode. If any of the first three criteria is not satisfied corresponding inhibit signals are generated and applied to an inhibit gate TR9 which prevents a *Phased* indication being given. If the first three criteria are satisfied then the resultant indication depends on the error signal from the phase comparator circuit. The inhibit signal generation will be described first, followed by the phase comparator operation.

Information showing absence of the *Colour* indication is carried to TR9 by D16 from the collector of TR25 which is turned on when the *Colour* indicator switch TR23, 24 is not operated.

The PAL sequence of the separated burst is compared with the reference PAL squarewave in the long-tailed-pair timing comparator TR28,29. One input of the comparator is fed with separated PAL squarewave which is regenerated at the junction R50–R51 by discriminator D10,11 and amplified by the 7·8-kHz ringing circuit L1,C30. The other input of the comparator is fed with reference PAL squarewave. When a sequence error is present, positive-going pulses are generated at the collector of TR28. These are amplified in TR31, integrated by R85,C32 and the resulting d.c. signal is used to drive the threshold switch TR32, 33. The logic output from TR33 is taken to the inhibit gate TR9 by the diode D18.

The 180° burst-phase-error inhibit signal is generated by discriminator D8, 9 and amplified by TR17–19. The output from TR18 is applied to the inhibit gate TR9 by the diode D12. (This error detector is necessary only to compensate for inadequacies in the type of discriminator used in the phase comparator circuit which would otherwise allow the 180° phase error to pass undetected.)

In the phase comparator circuit, reference subcarrier is fed to discriminator D10,11 by the input amplifier TR1–4 which, apart from R6, duplicates the burst input amplifier to give good thermal tracking. The output from the discriminator is a

d.c. signal at the junction R52, R53 proportional to the error in quadrature between mean burst phase and reference subcarrier. This signal is integrated by C24, C48 and the input impedance of TR6. This stage feeds the difference amplifier IC1 which in turn drives the long-tailed-pair TR8, 9 a dual-function d.c. level comparator and inhibit gate.

Operation on 405-line Monochrome Signals

The *Pulses* and *Timed* circuits operate in identical manner. Colour is not detected; the outputs therefore do not declare *Colour* or *Phased*. The burst muting is present.

Operation on 525-line NTSC Signals

Both the phase of NTSC colour bursts and the mean phase of PAL colour bursts are in quadrature with the reference subcarrier, hence the discriminators function identically. The NTSC burst, however, has no 180° phase alternation and therefore no input of reference PAL squarewave is required. Under this condition the PAL sequence error detector gives a non-inhibit output, allowing the *Phased* indication to appear.

Alignment

The MN2/511 requires feeds of syncs and colour bursts at standard level for its alignment. These can be obtained conveniently from a Sync Separator UN1/589, both units being mounted for testing in a panel PA1M/537, PA1M/538 or PA1M/544. Care should be taken when using these panels to ensure that the feeds are correctly terminated.

Apparatus Required

Voltmeter (Avo 8)
Oscilloscope (5mV/cm)
4·43-MHz Vectorscope fitted with probe
Switched attenuator 0 to 20 dB
Extender board CH1A/3
Tested Sync Separator UN1/589
Back panel as above
Feed of coded PAL colour bars
Feed of mixed syncs (225ns later than colour bars) from
Gen-locking S.P.G. (625-lines)
Feed of PAL squarewave
Feed of subcarrier via
UN1/537 phase shifter
Feed of 405-line composite video.

Procedure

1. Plug the MN2/511 into the back panel. With mains connected the *Pulses* and *Phased* lamps should light.
   Plug in the UN1/589. The two lamps should go out, PLA4 should go to +12·5V d.c. and PLA6 to −5·5V d.c. w.r.t. chassis.
2. Connect the colour-bar feed to the UN1/589 input. Confirm that 2V p-p of separated syncs appears on PLA14 and 0·3V p-p of separated bursts on PLA7 of the MN2/511. Both *Pulses* and *Colour* lamps should light.
3. Monitor the waveform at the junction L2–R131. Tune the core of L2 for maximum sinewave. Replace the colour-bar feed with the 405-line feed. Monitor the waveform at the junction L3–R135 and tune the core of L3 for maximum sinewave.
4. Short-circuit PLA14 to chassis and confirm that the *Pulses* lamp goes out and that 12·5V d.c. appears on PLA8. Remove the short-circuit and confirm that the lamp lights and that the 12·5V disappears.
5. Replace the 405-line feed with the colour-bar feed. Connect the sync-pulse feed to PLA5 via the *Ref. Syncs* socket. Adjust R148 *Set comparator balance* to equalise the d.c. potentials at pins 6 and 8 of IC2.
6. Monitor the waveform at the base of TR38. Adjust the line phase of the SPG until the sawtooth waveform disappears, then offset it by 600ns and check that the *Timed* lamp goes out. Reset the line phase offset to 400ns and select R123 so that the lamp just lights. Check that the lamp just goes out at 600ns offset. Confirm that +12·5V d.c. is present on PLA2 when the lamp is out and absent when on.
7. Connect the PAL squarewave and subcarrier feeds. Using the Vectorscope, note the mean burst phase at the input on PLA7. Transfer the probe to the reference subcarrier input on PLA11 and adjust the subcarrier phase to be that of the mean burst phase. Shift the phase of the subcarrier by 90° clockwise on the Vectorscope, to be in lagging phase quadrature to the mean burst phase.
8. Measure the d.c. potentials at TR18 and TR33 collectors—both should be in the non-inhibit condition, slightly above earth.
9. Remove the colour-bar feed. With the oscilloscope direct-coupled, monitor TP1 and adjust *Set balance* control R21 to give a clear maximum. Replace the colour-bar feed.

NOTES 1. TR2, TR14 & TR20 TO BE MULLARD NO ALTERNATIVE SUITABLE

relay and transistor terminations view on leads

CA3028A (DN935 A4)

2N918

DC109 BCY71 BC108 BCY31 BFY51 BCY72 or BCY70 ASZ21

CLARE-ELLIOT RP-7601-60 615ohm

from D21696 A1 iss.4
Parts List D21697 A4

PLB 1 PLB 2 PLB 3 PLB 4 PLB 5 PLB 6 PLB 7 PLB 8 PLB 9 PLB 10 PLB 11 PLB 12 PLB 13 PLB 14 PLB 15

Fig.2 Circuit of the Sync Monitor MN2/511

10. Adjust *Set zero phase* control C47 to mid-range and select C14 to achieve a similar maximum at at TP1 to that obtained in stage 9.
11. Select R30 to give a *Phased* indication which will lock in at ±10° subcarrier phase adjustment and hold in for ±12°. Confirm that ±12V d.c. is present on PLA15 when the *Phased* lamp is out and absent when the lamp is on.
12. Switch the subcarrier phase through exactly 180° and confirm that *Phased* indication cannot be obtained. Check that the d.c. potentials at the collectors of TR18 and TR33 have changed to a few volts below ±12·5V (the inhibit condition).
13. Monitor the burst amplitude on PLA7; it should be 300±9mV. Using R82 in the UN1/589 attenuate the burst by 7 dB and select R68 such that the *Colour* lamp just does not light. Confirm that it will light at −6 dB. (The switching delay may be up to 5s.) Confirm that +12V d.c. is present on PLA1 with the *Colour* lamp out and absent with it on.
14. Monitor the Black-level output of the sync-separator and confirm that as the *Colour* lamp goes out the residual burst is blanked off.

References to Typical Associated Equipment

1. Sync Separator UN1/589.
2. Sync Separation and Monitoring Panels PA1M/537; PA1M/538; PA1M/544.

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