PRECISION SUBCARRIER FREQUENCY MONITOR MN7/504

Introduction

The MN7M/504 measures accurately several of the parameters of the subcarrier signal used in the 625-line PAL system; this Monitor is colloquially known as *A.M.O.S.* (*A*ccurate *M*easurement *O*f *S*ubcarrier).

According to the measurement required, the Monitor accepts up to four input signals:

local PAL subcarrier
local mixed syncs or composite video
remote composite video with PAL colour burst
reference frequency signal.

The reference signal is typically provided by a separate Droitwich monitoring receiver[1].

The measurement functions provided by the MN7M/504 are:

Subcarrier Frequency Selected (local or remote) subcarrier frequency is measured, using the Droitwich reference, and displayed to ±0·1 Hz.

Frequency Difference The frequency difference between local subcarrier and that derived from the remote signal is measured and displayed to ±0·1 Hz.

Cycles/8 Fields The number of cycles of selected subcarrier occurring in eight field-periods is measured and displayed to ±0·1 cycles. If the count is outside the correct value of 709 379·0 ±0·1 cycles on four consecutive counts, then audible and visible alarms are given. A *Check* facility is available in this mode whereby the count and display accuracies are increased to ±0·01 cycles, but the alarms are muted.

The MN7/504 requires a mains input and comprises the four units listed below as mounted from left to right in a modified PN3A/10A rear-interconnection panel:

UN1/603	Frequency Counter (a modified RACAL 835 Counter)
UN3/521	Control Unit
OS1/502 or OS1/513	Burst Locked Oscillator
UN1/540	Sync Separator and Power Unit

The Frequency Counter can be isolated from the other units by selecting *Counter Normal* or *Off*. In this mode the Control Unit does not affect the Frequency Counter which can then perform all its normal functions.

General Specification

Signal Inputs

Local PAL Subcarrier	1 V p-p
Local Composite Video	1 V p-p
or Mixed Syncs	2 V p-p
Remote Video	Standard colour video signal
with Burst	0·3 V p-p ±6 dB
Droitwich 200 kHz	sinewave, greater than −3 dB w.r.t. 1 V p-p
or 1 MHz	sinewave, greater than −18 dB w.r.t. 1 V p-p

Input Impedances

Local PAL Subcarrier	75 ohms
Local Composite Video	75 ohms) or high-
or Mixed Syncs	75 ohms) impedance,
Remote Video	75 ohms) depending on UN3/521 switch positions
Droitwich	about 1·5 kilohms

Counter Inputs	Normally fed from UN3/521. Two high-impedance inputs available when *Counter Normal* is selected on UN3/521.
Power Input	240 V, 50 Hz, 40 W
Operating Temperature	0° to 40°C ambient
Weight	12·25 kg (27 lb)

Operation

Figures 1 to 4 show the signal inputs required, the control positions and give details of the display and accuracy obtained in the normal modes of operation.

MEASUREMENT OF SUBCARRIER FREQUENCY

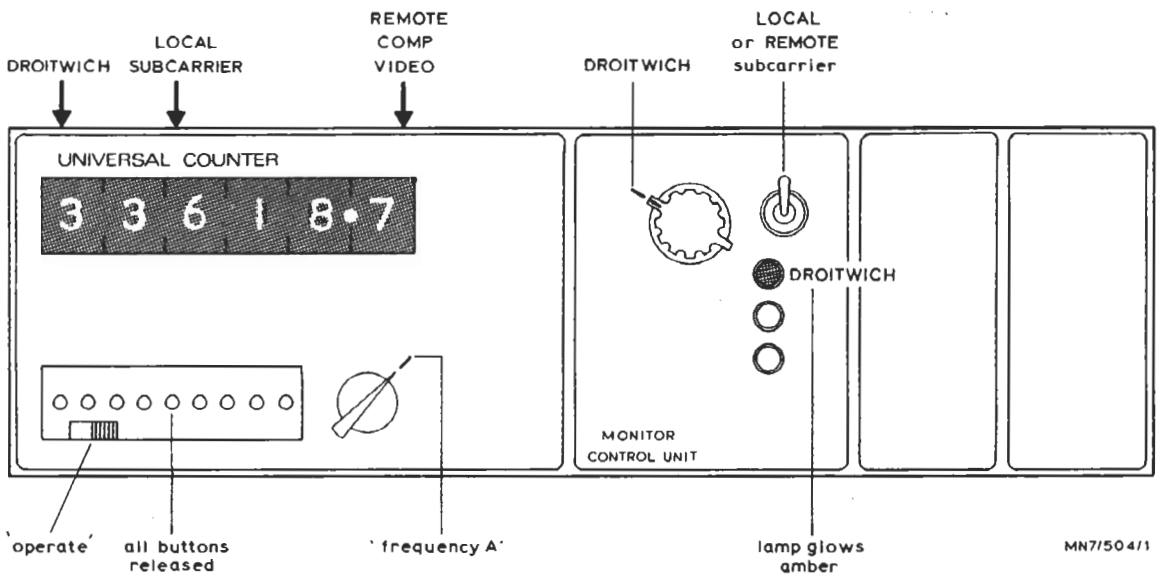


Fig. 1. Measurement of Subcarrier Frequency (Local or Remote)

Control positions	as indicated in Fig. 1
Signal inputs	Local subcarrier Remote comp. video (and burst) Droitwich
Display	selected subcarrier frequency; the last six digits of an eight-digit count are displayed, e.g. 44(33618·7) Hz
Accuracy	±0·1 Hz
Count time	10 seconds
Display time	1 to 5 seconds (manually variable or *Hold*)

MEASUREMENT OF FREQUENCY DIFFERENCE

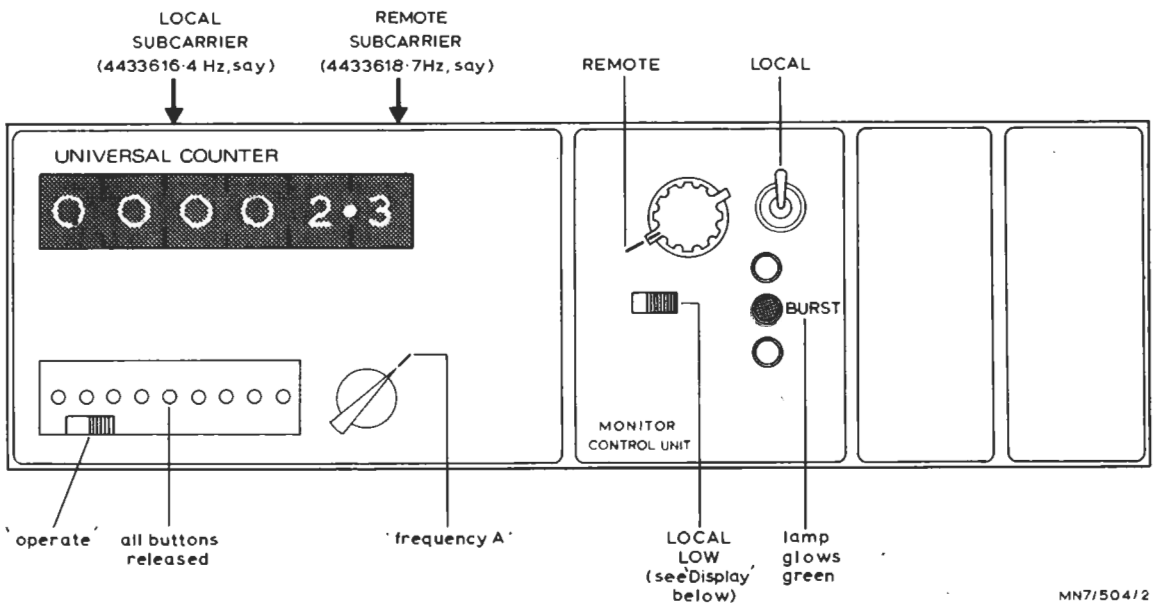


Fig. 2. Measurement of Frequency Difference

Control positions	as indicated in Fig. 2
Signal inputs	Local subcarrier Remote comp. video (and burst)
Display	frequency difference in Hertz between local subcarrier and that derived from the remote subcarrier-burst; sense of difference as determined by the position of the local high/local low switch to obtain non-complemented display
Accuracy	displayed difference is less than the true difference by 0·75% of the displayed difference
Resolution	±0·1 Hz
Count time	10 seconds
Display time	1 to 5 seconds (manually variable or *Hold*)

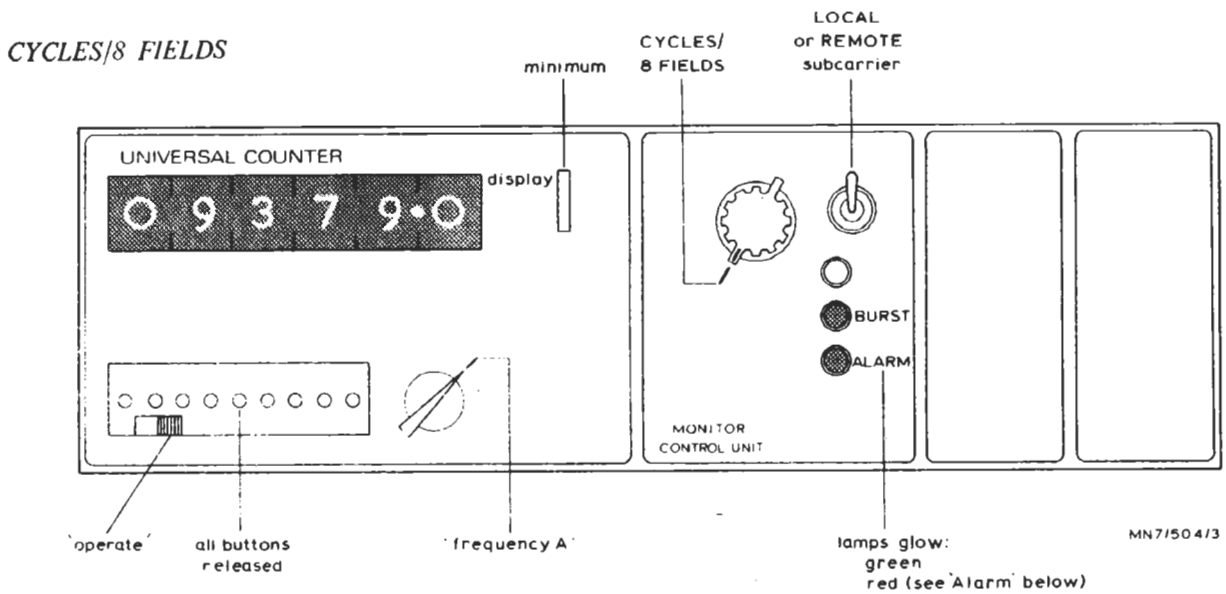


Fig. 3. Measurement of the number of cycles of subcarrier in the duration of eight field periods (Cycles/8 Fields)

ALARM FACILITY

Control positions — as indicated in Fig. 3

Signal inputs — Local subcarrier
Local comp. video
Remote comp. video (and burst)

Display — number of cycles of selected subcarrier occurring in eight field periods of associated mixed syncs; the last six digits of a seven-digit count are displayed; e.g. 7(09379·0) cycles

Accuracy — ±0·1 cycles

Alarm — one error registered for each count outside 709 379·0 ±0·1 cycles; number of errors before alarm: 4 (can be reduced to 2; see under **General Description**);
fault duration: 10 seconds (Counter *display* time set to minimum)
5 seconds for 2-count option
audible alarm: 1 kHz tone interrupted for ½ second at 1-second intervals;
visible alarm: flashing red light with 1-second period

Count time — 1·6 seconds

CHECK FACILITY

Control positions — *Function* switch on the Frequency Counter to *Ratio* $n\frac{A}{B}$
0·1 ms button on the Frequency Counter depressed;
Reset Alarm button on the Control Unit depressed for the count duration

Signal inputs — as for *Alarm Facility*

Display — number of cycles of selected subcarrier occurring in eight field periods of associated mixed syncs; the last six digits of an eight-digit count are displayed; e.g. 70(9379·00) cycles

Accuracy — ±0·01 cycles

Alarm — inhibited

Count time — 16 seconds

COUNTER NORMAL OPERATION

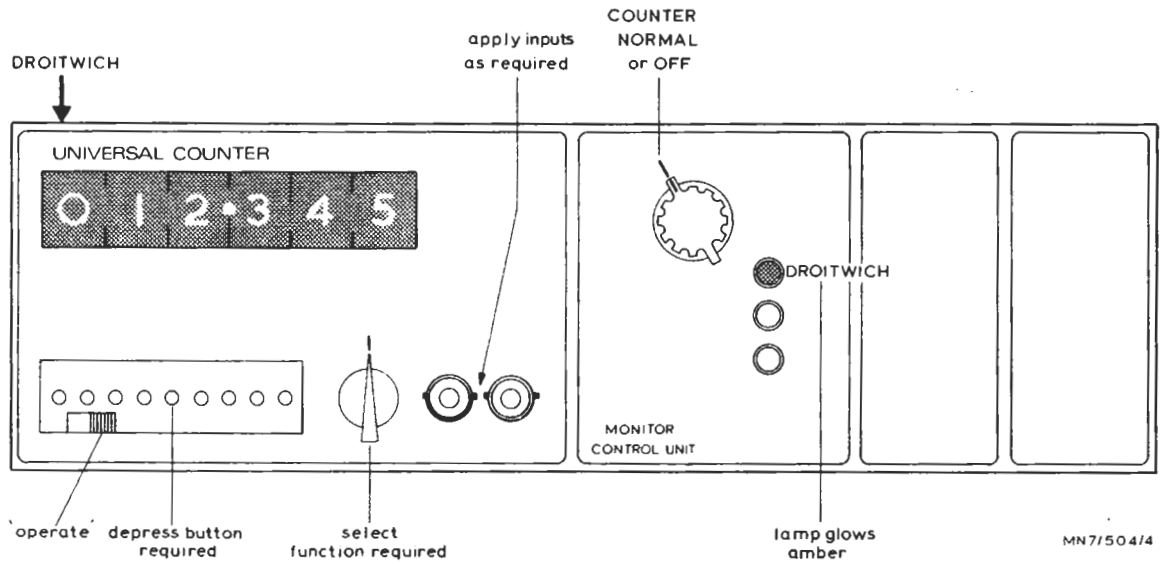


Fig. 4. Counter-normal Operation

Display	as selected
Signal inputs	Droitwich Front-panel A and B inputs as required
Accuracy (internal oscillator)	1 part in 10^{10} if Droitwich input is present

General Description

A block diagram of the Monitor (showing detail within the UN3/521 Control Unit) is given in Fig. 5.

(a) Subcarrier Frequency Measurement

In the *Droitwich* mode for the measurement of subcarrier frequency, the incoming 1 MHz or 200 kHz sinewave (derived from the Droitwich transmission) is amplified by a 1-MHz tuned amplifier and the output fed both to a 1-MHz detector and lamp, and also to Printed Board 2 to lock the reference oscillator in the UN1/603 Frequency Counter Unit.

Local and remote subcarriers are both supplied to the *Source* switch; remote subcarrier is derived from the burst in the OS1/502 which accepts back-porch pulses from the UN1/540 Sync Separator.

Decimal-point switching in the UN1/603 is controlled by SA5 and control relays on Printed Board 1 in the UN1/603 are operated by SA4 to select *Frequency A* and *10 sec* time gate.

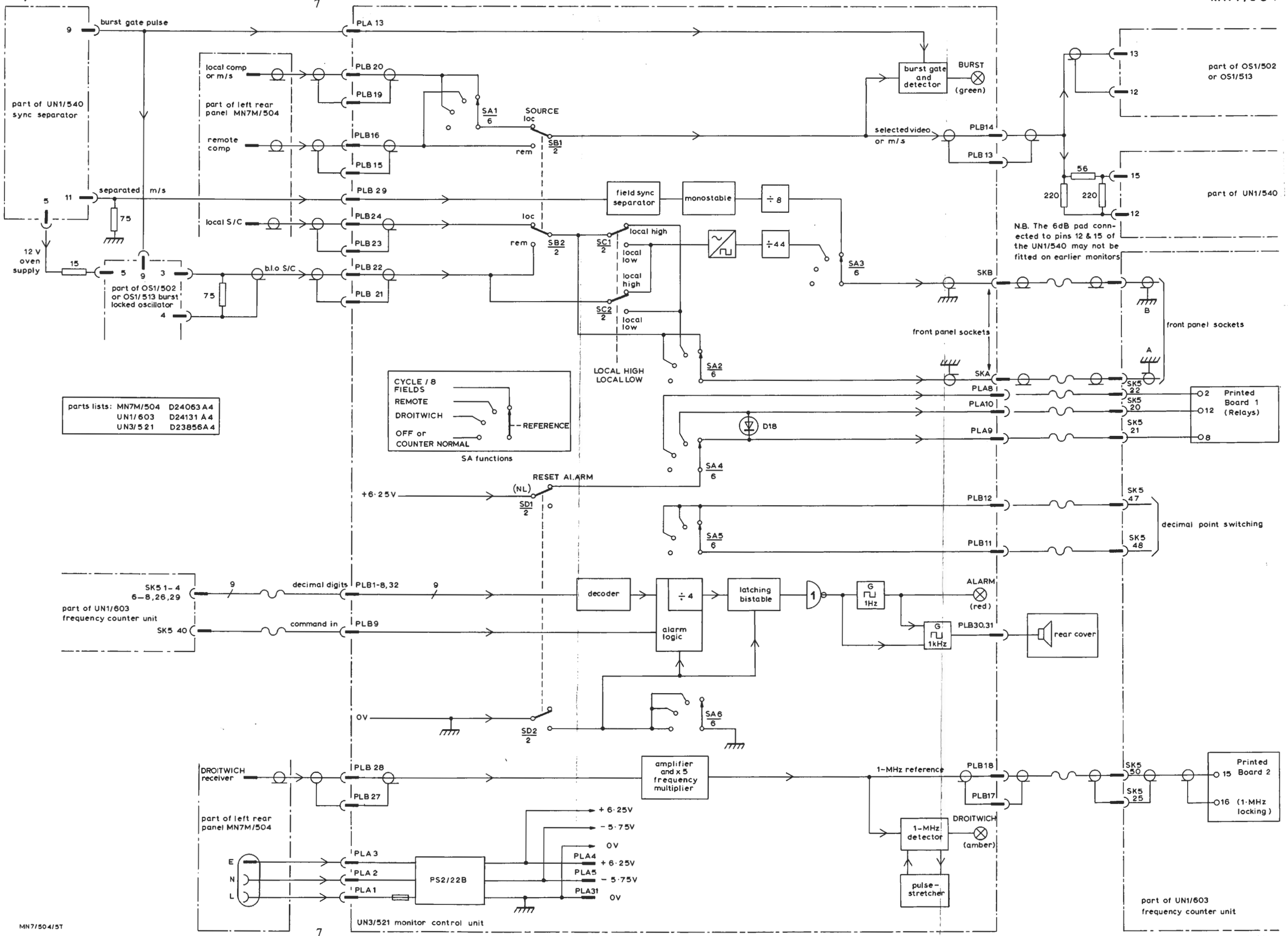
(b) Frequency Difference Measurement

Incoming remote video is applied to the UN1/540 Sync Separator, to the OS1/502 Burst Locked Oscillator and to the Burst detector in the UN3/521. The OS1/502 provides a derived remote subcarrier and the burst detector lights the *Burst* lamp when a burst is detected.

Local and remote subcarriers are switched by SB1, SB2 and SC so that the lower-frequency signal is routed by a divide-by-44 counter.

Decimal-point switching in the UN1/603 is controlled by SA5 and control relays on Printed Board 2 in the UN1/603 are operated by SA4 to select *Ratio* $\frac{A}{B}$ and *10 sec* time gate.

The display is derived as follows. Let the lower-frequency subcarrier be f_{SC} and the higher-frequency subcarrier be $f_{SC} + \Delta f$, and assume that both are approximately 4·4336 MHz. Thus the required display



parts lists: MN7M/504 D24063A4
UN1/603 D24131A4
UN3/521 D23856A4

Fig. 5: MN7/504: Block Diagram (With Details of UN3/521)

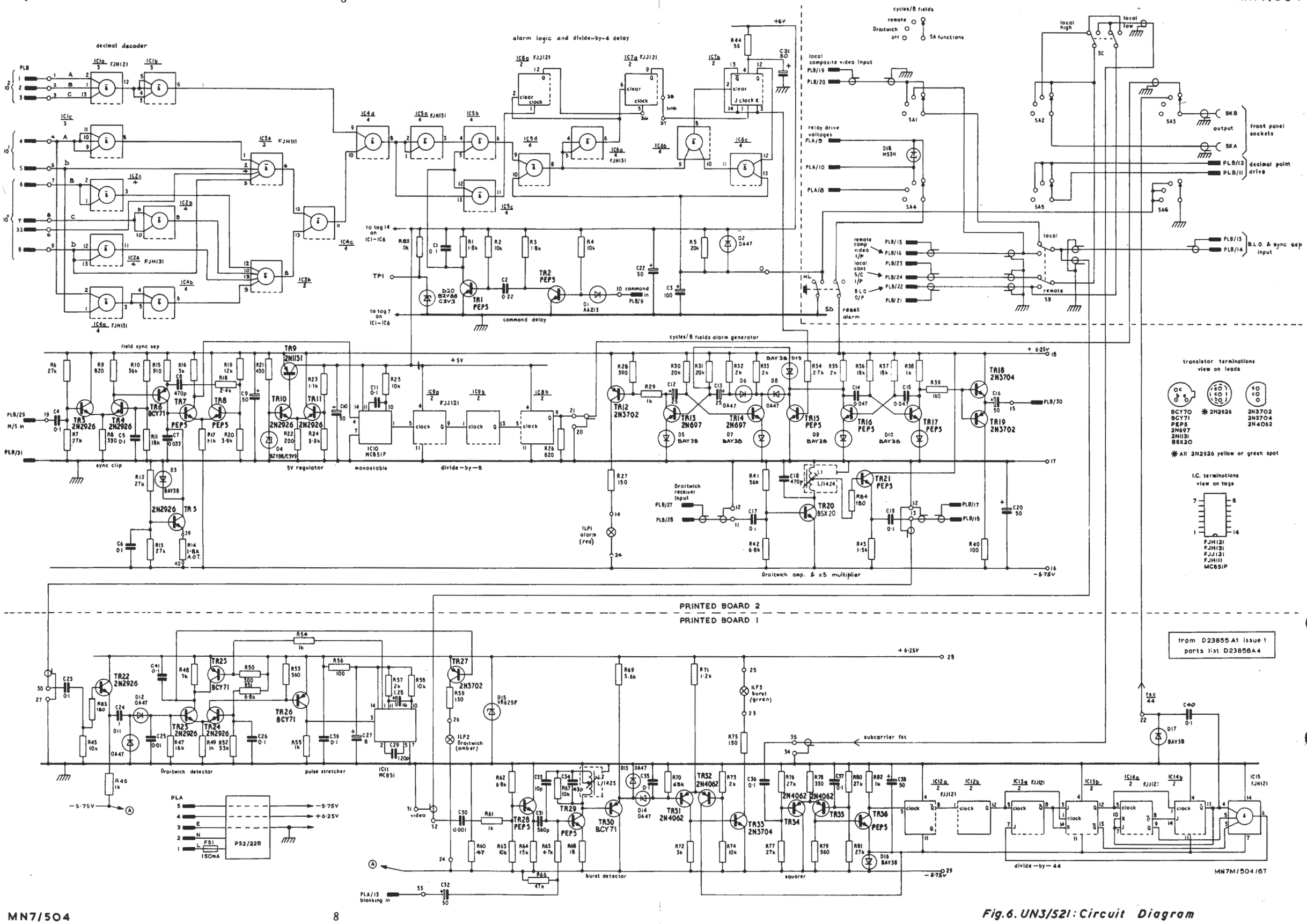


Fig.6. UN3/521: Circuit Diagram

is Δf. The UN1/603 accepts the input (f_{SC} + Δf) and $f_{SC}/44$ (from the UN3/521) and performs the division:

$$\frac{f_{SC} + \Delta f}{f_{SC}/44} = 44 + \frac{44\Delta f}{4{\cdot}4336 \times 10^{6}}$$

$$= 44 + \Delta f \times 10^{-5} - (0{\cdot}75 \times 10^{-2})\Delta f \times 10^{-5}$$

which is approximately equal to $44 + \Delta f \times 10^{-5}$

The Frequency Counter readout is designed to over-range such that the 44 is lost and the display gives the frequency difference in Hertz, with an error of 0·75% of the indicated difference. This error is negligible for displays of a few Hertz.

(c) Cycles/8 Fields Measurement

Two facilities are available in this mode of operation as detailed under Fig. 3 on page 5.

With both facilities, local or remote video signals and local or remote subcarrier are selected by the *Source* switch SB1 and SB2. Selected video is routed to the UN1/540 Sync Separator, to the OS1/502 Burst Locked Oscillator and to the burst detector in the UN3/521. Selected subcarrier is routed by SA2 to the *A* input of the UN1/603. Separated mixed syncs from the UN1/540 are taken to a field sync separator in the UN3/521 where the output is divided by 8 in a counter to feed the *B* input of the UN1/603.

With the *Alarm* facility, decimal-point switching in the UN1/603 is controlled by SA5 and control relays on Printed Board 2 in the UN1/603 are operated by SA4 to select *Ratio* $n\frac{A}{B}$ and *10 μs* gate time. The normal counter output is 709 379·0 ±0·1 cycles, but the Frequency Counter is designed to over-range such that the initial 7 is not displayed. A binary-coded-decimal (BCD) readout of the last three digits is fed to an error detector in the UN3/521. Alarm circuits in the UN3/521 are triggered by logic and a divide-by-4 counter when four successive counts outside 709 379·0 ±0·1 cycles are registered. (The UN3/521 can be modified to trigger the *Alarm* after only two successive counts.)

With the *Check* facility, both decimal-point switching and gate time are controlled by the Frequency Counter switches. (Holding depressed the *Reset Alarm* switch on the Control Unit gives internal control of the Frequency Counter relays.) The normal display is 9 379·00 ±0·01 cycles. Error-detector and alarm circuits in the UN3/521 are inhibited by the *Reset Alarm* switch.

(d) Counter Normal

The UN3/521 Control Unit serves in this mode only to indicate by the *Droitwich* lamp that a reference input is present and to feed that 1-MHz reference signal to the UN1/603 Frequency Counter oscillator locking-circuit on Printed Board 2.

All other switches and circuits of the UN3/521 are inoperative.

Circuit Notes

The circuit diagram of the UN3/521 is given in Fig. 6.

(a) Field Sync Separator

Mixed syncs are clipped by the long-tail pair TR3, TR4 and passed uninverted to the field sync separator TR5 to TR8. Transistor TR5 acts as a high-impedance load for TR6, thus the inverted broad pulses at TR6 collector are integrated by C7 during the field interval to give the waveform shown in Fig. 7(d). Non-inverted broad pulses are differentiated from the emitter of TR6 to drive TR8 with the waveform shown in Fig. 7(e). Thus TR7, which begins to conduct with the integrated first broad pulse is brought hard on by the differentiated pulse applied to TR8.

Correct operation of the field sync separator is largely determined by the value of R14. Typical waveforms of the signal at TR7 collector when this resistor is correct, low and high in value are given in Figs. 7(a), 7(b) and 7(c) respectively.

The signal from TR7 collector is applied to a 200-μs integrated-circuit monostable IC10 which feeds the divide-by-8 counter ICs 9a, 9b, 8b. The output from IC8b has an eight-field repetition period.

(b) Burst Gate and Detector

Emitter follower TR28 passes the selected video signal to a 1-MHz tuned amplifier TR29 which is neutralised by C33. Blanking pulses bias TR29 into the active region only during the back porch period to give the waveform shown in Fig. 8 when a burst is present on the video signal. Emitter follower TR30 passes this signal to a clamping diode D13 and peak-

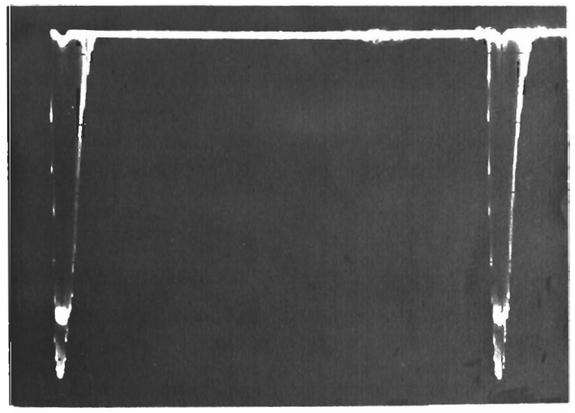
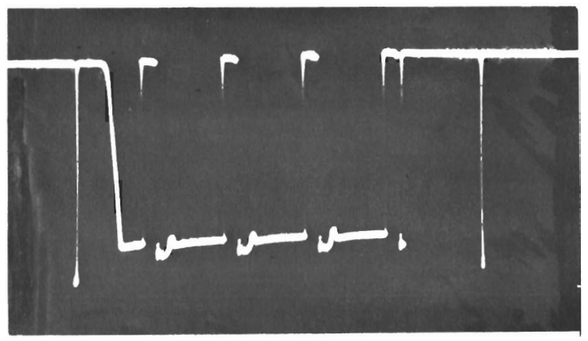
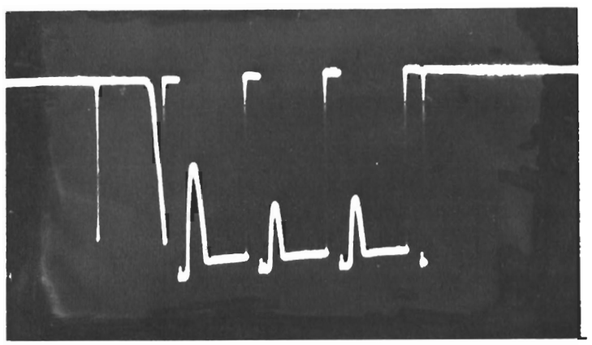


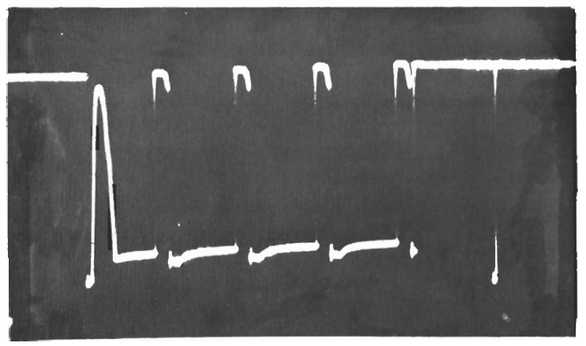
Fig. 8 Waveform in the UN3/521 Burst Detector at TR30 emitter



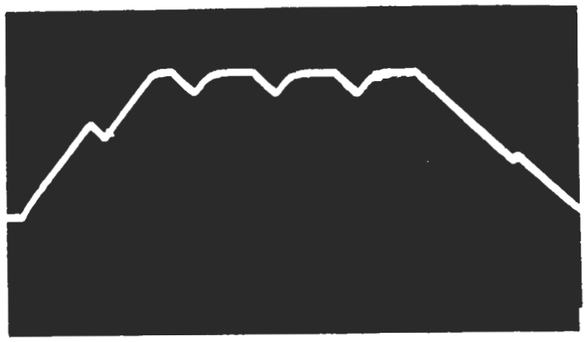
(a) TR7 collector : R14 correct



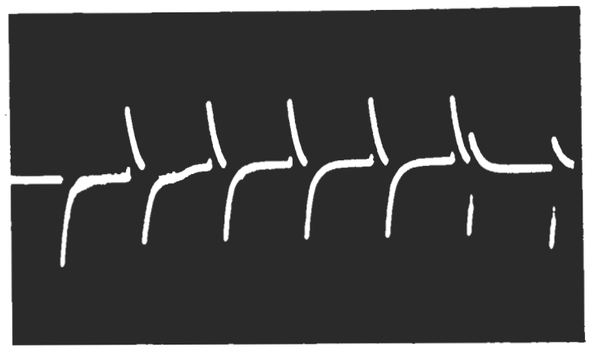
(b) TR7 collector : R14 low



(c) TR7 collector : R14 high



(d) TR7 base : correct waveform



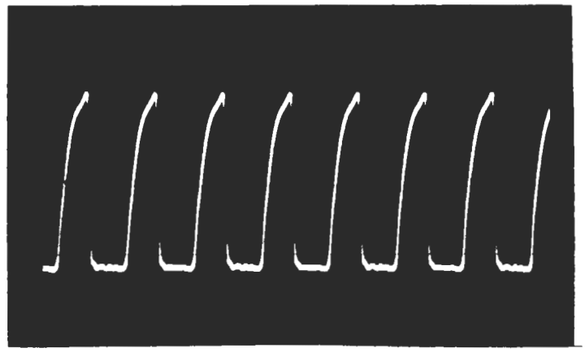
(e) TR8 base : correct waveform

Fig. 7 Waveforms in the UN3/521 Field Sync Separator (during field interval)

level detector diode D14 with RC filtering in R70,C35 (6·8 ms time constant). TR31, in the long-tail pair with TR32, conducts to turn on TR33 when burst is detected, illuminating the green *Burst* lamp ILP3.

(c) Divide-by-44 Counter

The bistables IC12a and IC12b form a divide-by-4 counter and bistables IC13a, IC13b, IC14a, IC14b form a divide-by-11 counter. Figure 9 gives photographs of input and output waveforms and Fig. 10 shows a simplified diagram of the divide-by-11 section; idealised waveforms for that counter are given in Fig. 11. All bistables are J-K master-slave types[2].



(a) TR36 collector (subcarrier frequency)

(b) pin 22, board 1 (divider output)

Fig.9 Waveforms in the UN3/521 Divide-by-44 circuit

MN7M/504/7P

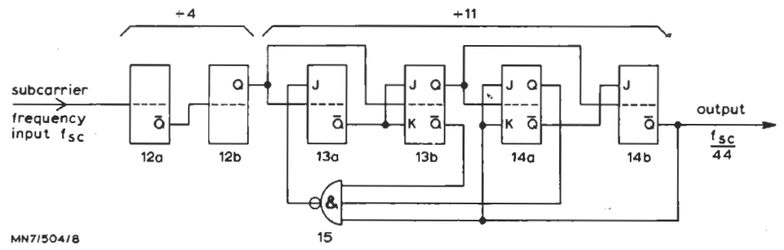


Fig. 10. Logic Diagram of the Subcarrier Divide-by-44 Circuit

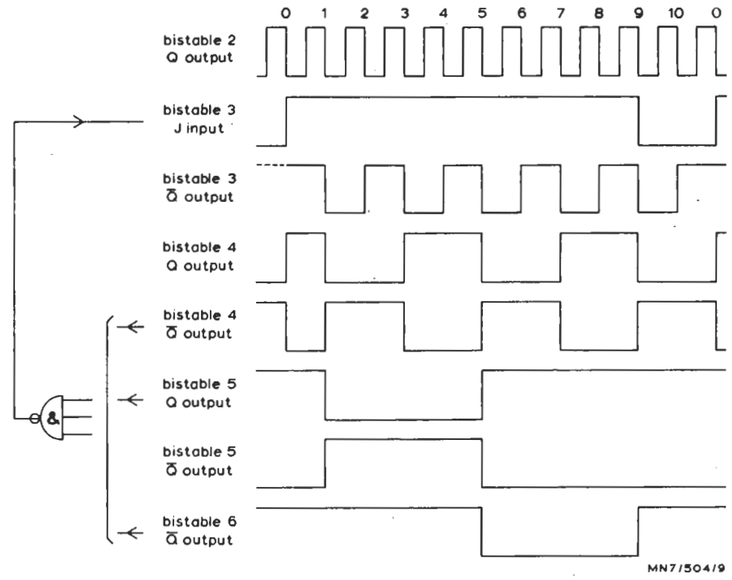


Fig. 11. Idealised waveforms in the divide-by-11 section of the subcarrier counter

(d) Error Detector and Alarm Logic

A simplified logic diagram of the error detector is given in Fig. 12. Binary-coded decimal inputs from the UN1/603 are fed to logic gates in the error detector. Six input combinations give a level-0 output from IC4d; these are listed in Table 1. Three of these combinations, corresponding to *Cycles/8 Fields* output counts of 709 379·0 ±0·1 are used; the other three cannot occur in the Counter output and are not used. All other input combinations give level-1 outputs from IC4d to register an error count in the alarm logic.

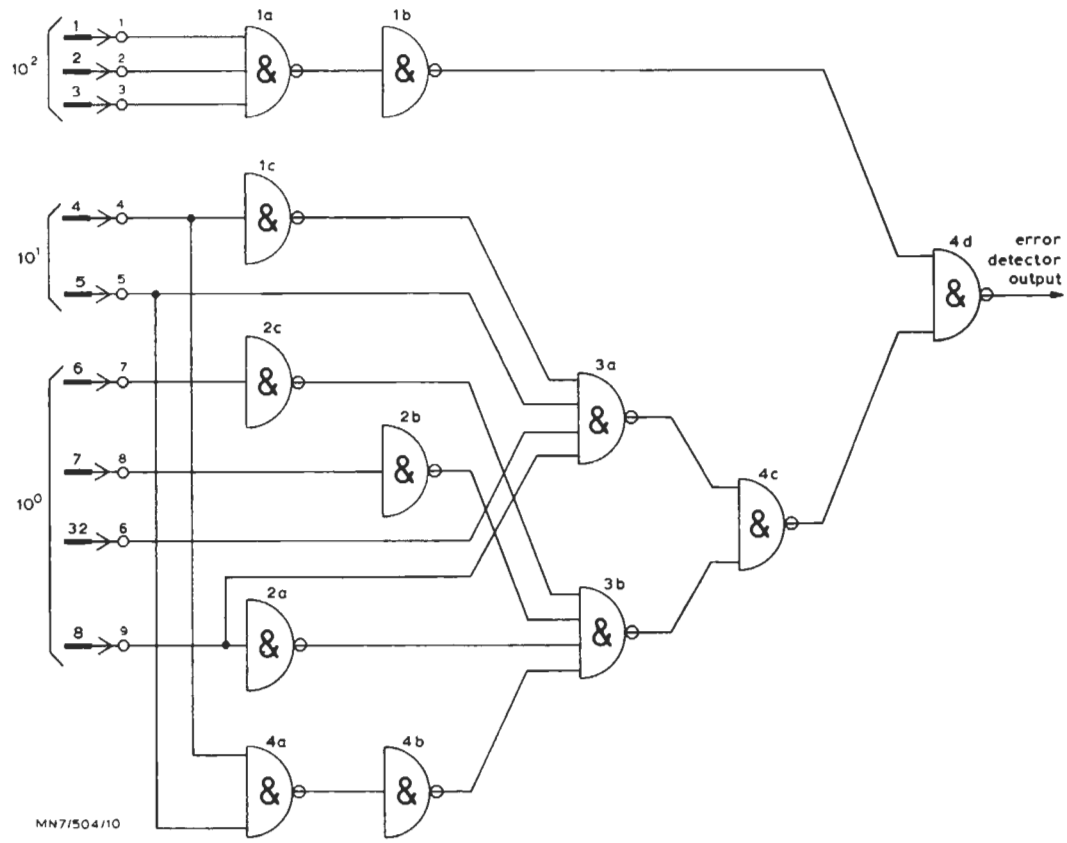


Fig. 12. Logic Diagram of the Error Detector

TABLE 1

Inputs for Level-0 Error-detector Outputs

Decimal weighting	10^2			10^1		10^0				
Binary weighting	4	2	1	8	1	8	4	2	1	*Display*
Input combinations	1	1	1	1	0	1	0	0	1	78·9
giving level-0	1	1	1	1	1	0	0	0	0	79·0
error-detector	1	1	1	1	1	0	0	0	1	79·1
output;	1	1	1	1	0	1	0	1	1	*
i.e. no error	1	1	1	1	0	1	1	0	1	*
	1	1	1	1	0	1	1	1	1	*
UN3/521 pin no.	3	2	1	5	4	8	7	6	32	

* These inputs would give level-0 outputs, but do not occur in the Frequency Counter BCD output

Fig. 13 shows a simplified diagram of the alarm logic. The error-detector output is inverted by IC5a and both normal and inverted outputs sampled in IC5c and IC5b by the delayed command (sampling) signal. For a level 0 detector output (no error) IC5b gives a reset level 0 which is gated with a manual reset signal and applied to bistables ICs 8a, 7a, 7b to set the Q outputs to 0. This *Clear* signal overrides the clocking effect on bistable IC8a of the negative-going signal from IC5c.

transistors against reverse emitter-base breakdown. Diode D6 ensures that on turn-on TR14 always conducts in preference to TR13. Thus the alarm does not operate when switching on but it may give a slight squeak when switching off.

When TR15 is turned on (in the *Alarm* inhibit condition) TR16 collector is held at about 0 V and TR13 base is also clamped to about 0 V by D19 to ensure that TR12 is cut off and ILP1 not illuminated. This inhibits the operation of both generators.

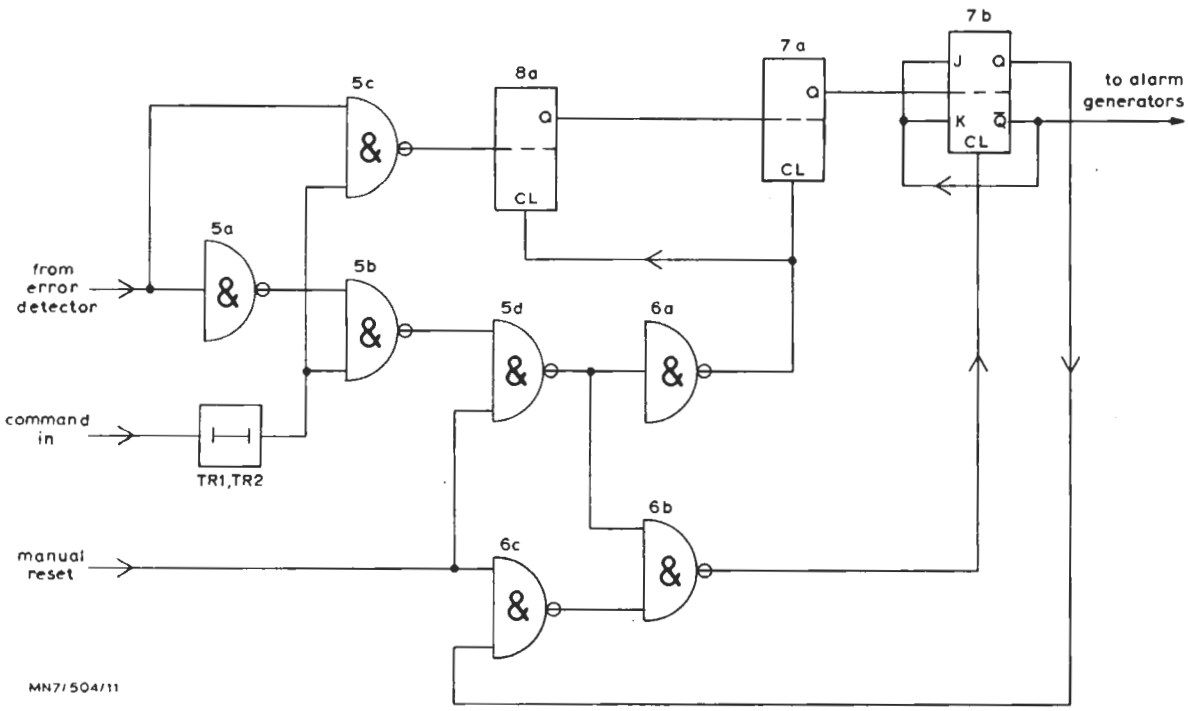


Fig. 13. Logic Diagram of the Alarm Logic and Divide-by-4 Counter

For a level-1 detector output (error present) IC5b output remains at level 1 so that a *Clear* signal is not generated. IC5c generates a dynamic-0 output which sets the Q output of bistable IC8a to 1. The outputs of the three bistables for successive error inputs are shown in Fig. 14. After the fourth consecutive error bistable IC7b is set and remains so, until reset by a level 0 on the manual reset input.

The bistable clearing circuits are such that counts of one, two or three consecutive errors are automatically cleared.

The divide-by-4 counter can be modified to trigger the *Alarm* circuits after a count of 2 by removing the link on Board 2 between pins 37 and 38, and replacing it between pins 36 and 37. Operation of the bistable clearing-circuits is unchanged.

(e) Alarm Generators

TR13,TR14 form a 1-Hz squarewave generator and TR16,TR17 form a 1-kHz squarewave generator. Diodes D5, D7, D9 and D10 protect the associated

When TR15 is cut off (in the *Alarm* condition) TR13 and TR14 are free to oscillate but D8 and D19 ensure that TR16,TR17 only oscillate when TR13 is conducting.

(f) Droitwich Amplifier and Detector

The Droitwich input signal (either 200 kHz or 1 MHz) is passed by the 1-MHz tuned amplifier TR20. Emitter follower TR21 provides the reference signal for the Frequency Counter and emitter follower TR22 feeds the detector circuit. Negative peaks are d.c.-restored by D11 and that signal peak-level detected by D12. The long-tail pair TR23,TR24 drives TR27 to power the *Droitwich* lamp and also operates the pulse-stretching circuit, TR26, IC11.

When a signal is first detected, TR23 begins to conduct and TR24 begins to turn off; the positive transistion at TR24 collector is inverted by TR26 and triggers an 80-ms monostable IC11. The negative-pulse output from pin 1 turns on TR25 thereby ensuring that the lamp does not illuminate until a Droitwich

signal has been received continuously for 80 ms.

Any disruption in the Droitwich signal immediately turns off the lamp and when the signal returns the monostable ensures that the lamp is held off until the signal once again has been received continuously for 80 ms. Thus by this pessimistic display the lamp indicates a satisfactory reference input for consistent operation of the Frequency Counter.

Test Schedule

This schedule is in two parts referring to the UN3/521 and the complete MN7M/504 respectively. Part 1 requires a UN1/540 Sync Separator and an OS1/502 (or OS1/513) Burst Locked Oscillator, each aligned according to the relevant Instruction. Part 2 requires in addition a UN3/521 Monitor Control Unit aligned according to Part 1 of this schedule. Complete Production Schedules are included in the relevant Technical Specifications[3].

EQUIPMENT

Part 1 Avo 8
Wayne-Kerr Video Oscillator or equivalent
Oscilloscope (Tektronix 515 or equivalent)
X10 Attenuator probe
Trimming tool, Neosid TT1 with handle cut to ½ inch

Part 2 Droitwich Receiver RC3/7 or RC3/8
Whip Aerial

SIGNALS

Part 1 1 V p-p composite video with PAL burst
2 V p-p mixed syncs
2 V p-p field trigger (synchronous with mixed syncs)

Part 2 1 V p-p PAL subcarrier
2 V p-p mixed syncs having the correct frequency relationship with the subcarrier

ALIGNMENT PART 1 (UN3/521)

1. Withdraw the UN1/540 and the OS1/502 from the Monitor chassis.
2. *Power Supply* Check the output voltage of the PS2/22 using the Avo 8. Set the voltage to 12·00 V ±0·05 V (about +6·25 V and −5·75 V w.r.t. chassis) by adjusting RV1. If a d.c. fault is suspected then refer to **Maintenance** section 1.
3. *Field Sync Separator* Plug the UN1/540 into the Monitor chassis. Connect the mixed sync feed to the *Local Comp* input of the Monitor. Switch on the mains to the Monitor. The *Burst* lamp may glow momentarily; if it fails to extinguish refer to **Maintenance** section 1 after completing this section of the alignment.
Set the *Reference* switch to *Cycles/8 Fields.* Check the oscilloscope probe alignment. Trigger the oscilloscope externally from the negative

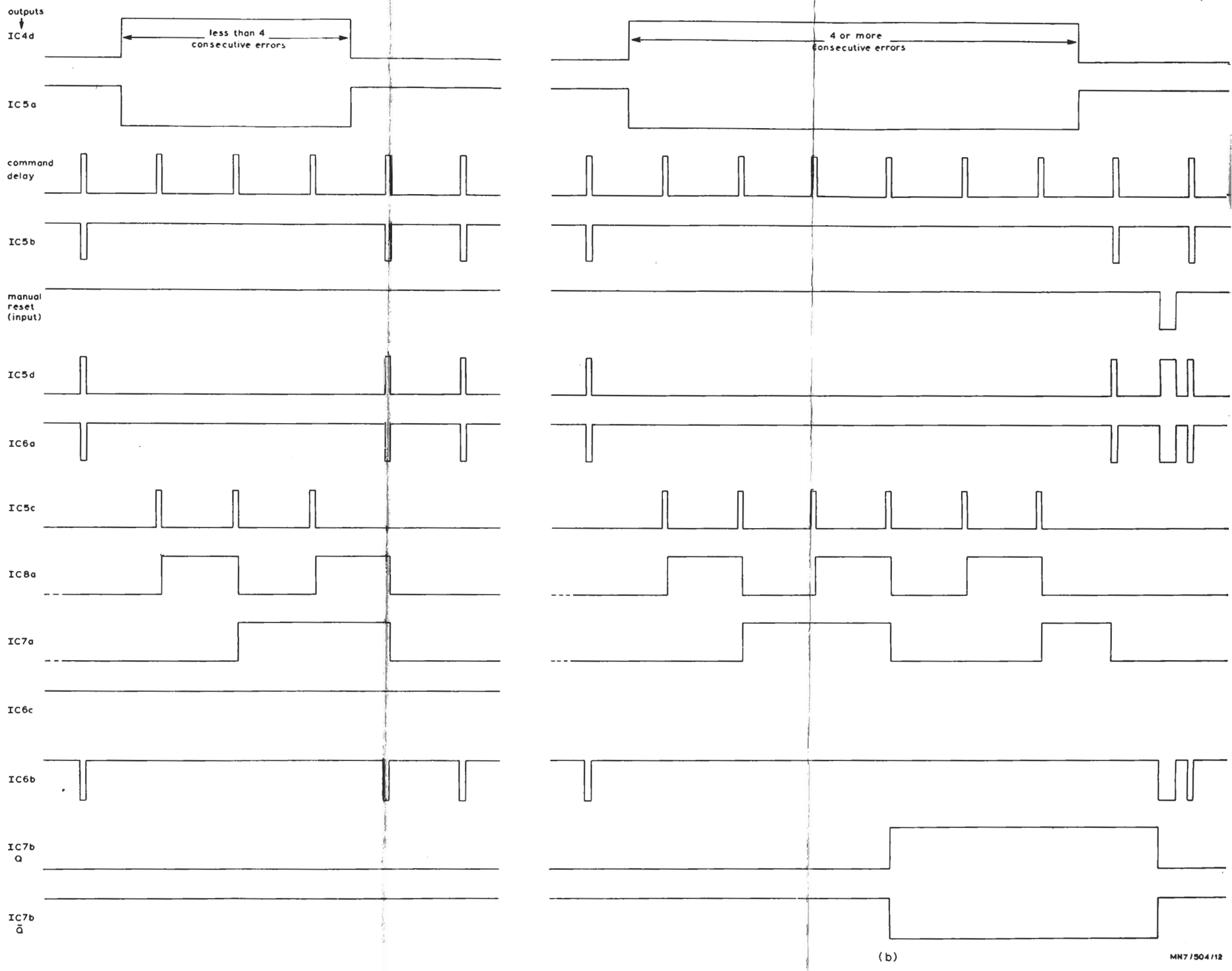


Fig. 14. Idealised waveforms in the alarm logic

edge of field trigger and monitor the waveform at TR7 collector. This should be as shown in Fig. 7(a) on page 7. If not, change the value of resistor R14 as indicated by Figs. 7(b) and 7(c). Figures 7(d) and 7(e) show the correct waveforms at the bases of TR7 and TR8 respectively.

4. *Burst Detector* Connect the composite video feed to the *Remote* input. Check that a 6 V p-p positive-going pulse is present on pin 33. Monitor the signal at the emitter of TR30, Adjust L2 for maximum burst amplitude; the waveform should be similar to that shown in Fig. 8 and the amplitude not less than 3·5 V p-p. If L2 tunes through a maximum but the amplitude does not exceed 3·5 V p-p then increase the value of C33.
Replace the video feed to the *Remote* input with mixed syncs. Check that the signal at TR30 emitter is less than 1 V p-p. (Ignore any spikes present only during the field interval.) If not, reduce the value of C33 until the amplitude is less than 1 V p-p. If C33 is changed repeat the step in the previous paragraph.

5. *Droitwich Amplifier and Detector* Disconnect the mains, remove all signal feeds and remove the UN1/540 Sync Separator. Connect a 75 ohm resistor across the *Droitwich Receiver* connector. Switch on the Monitor & Video Oscillator and allow them to reach operating temperature. Set the Oscillator to 0 dB and use the Frequency Counter UN1/603 to set the output frequency to 1 MHz ±1 kHz. Connect the oscillator to the *Droitwich Receiver* input of the Monitor. Reduce the output level until the signal at pin 13 (on Board 2) is less than 3 V p-p. Adjust L1 for maximum signal (reducing the Oscillator output level to keep the signal less than 3 V p-p). Check that limiting occurs at more than 4 V p-p. Reduce the Oscillator output until the *Droitwich* lamp just extinguishes; the signal at pin 13 should be 2·5 V ±0·5 V p-p.

ALIGNMENT PART 2 (MN7M/504 complete)

1. Connect mains to the Monitor and switch on. Allow at least 30 minutes before performing either of these operations:

2. *UN1/603 Oscillator Frequency* Substitute the 1-foot leads for the A and B input/output leads supplied with the Monitor. Connect the PAL subcarrier feed to the *Local S/C* input. Set the *Source* switch to *Local* and the *Reference* switch to *Droitwich*. Release the Frequency Counter from its case and withdraw as far as the bulkhead. **Live mains connectors are exposed on the Function switch when the unit is withdrawn.**

Adjust the trimming capacitor in the Frequency Counter for a display between 36616·0 and 33622·0. Push the Frequency Counter back into its case and secure it. Remove the 1-foot leads and replace with those supplied with the Monitor.

3. *OS1/502 (or OS1/513) Oscillator Frequency* Connect the mixed sync feed to the *Remote Comp* input. Set the *Source* switch to *Remote* and the *Reference* switch to *Cycles/8 Fields*. The *Burst* lamp should not glow. Adjust the potentiometer on the small board in the Burst Locked Oscillator for a display between 09380·0 and 09381·0. Do not mount the Oscillator on an extender board: the potentiometer can be easily reached from the top of the unit.

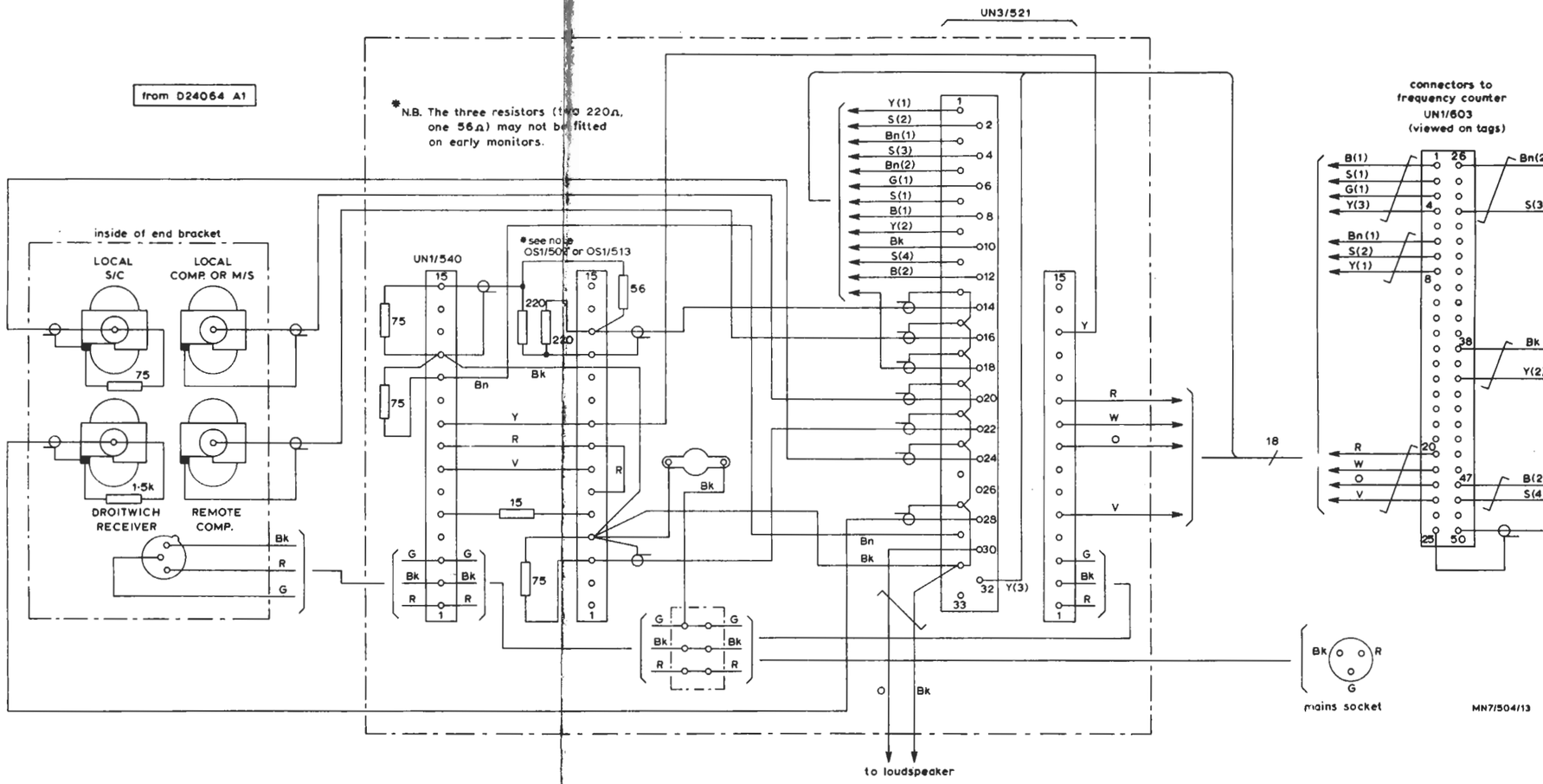


Fig. 15. Back-panel Wiring Diagram of the MN7M/504

Maintenance

Refer to the relevant Instruction for details of the OS1/502, UN1/540 and PS2/22B (within the UN3/521). The UN1/603 is described in the RACAL handbook; modifications to that unit are detailed in the relevant Instruction. Back-panel wiring of the MN7M/504 is shown in Fig. 15. Information given below only concerns faults within the UN3/521 Monitor Control Unit.

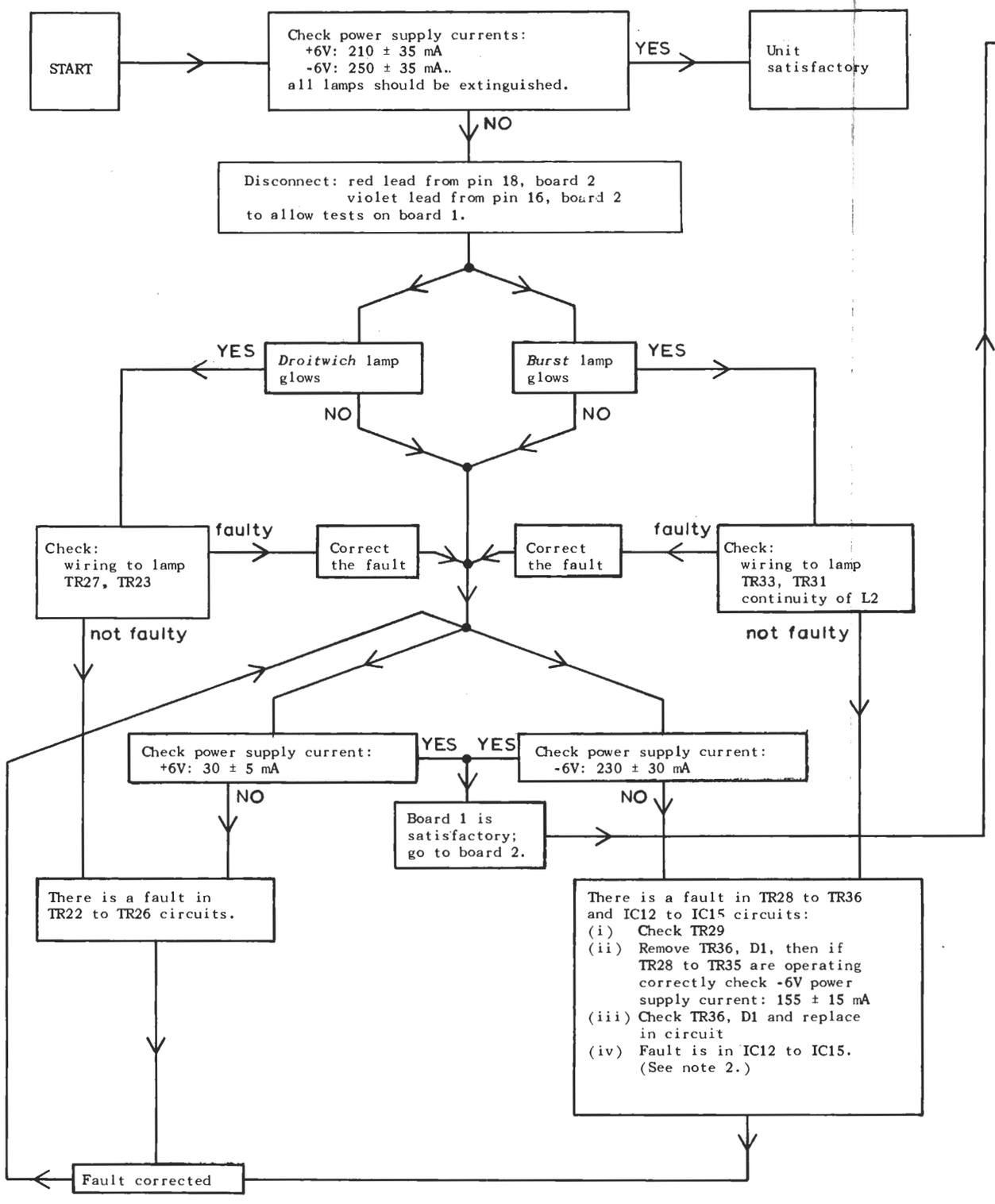
1. *D.C. Faults in the UN3/521*
Refer to the fault-finding guide in Fig. 16 for an indication of likely fault-areas.

2. *Alarm Logic in the UN3/521*
If a fault is suspected in the alarm logic it is necessary to add temporarily two extra components. Withdraw the UN3/521 and use short lengths of PUF1/3 to connect the pole of a microswitch to the printed wiring at the base of TR1 and the normally-open contact to the printed wiring at the emitter. Connect an 8-μF, 12-V capacitor across C1 with the positive end to the +5 V supply.

Set the *Reference* switch to *Cycles/8 Fields*, then make the checks (a) to (d) in the order indicated. If a check fails, refer to Fig. 17 and rectify the fault before proceeding with the next check.

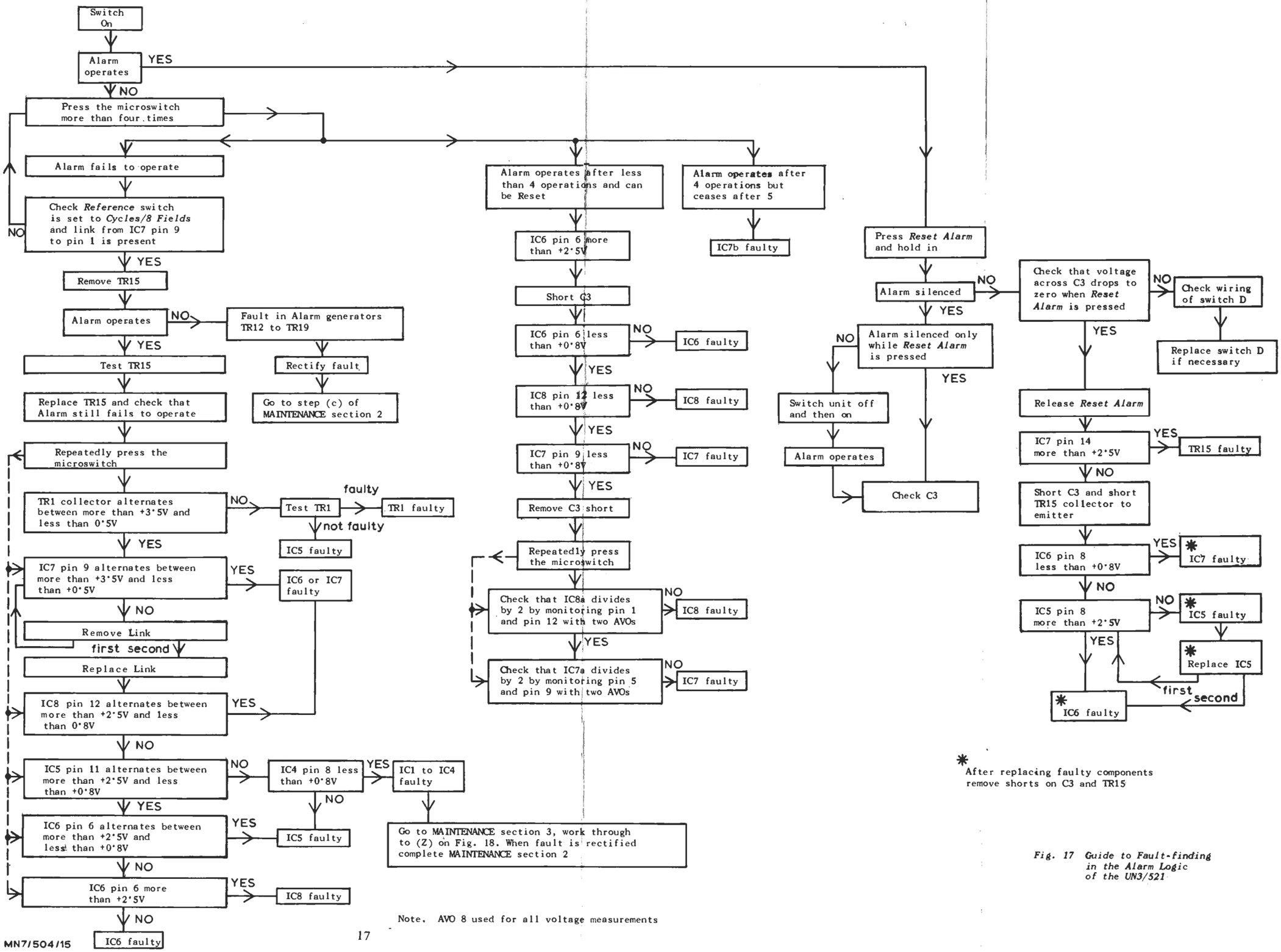
(a) Switch the mains on. The alarm must not operate but it may emit a slight squeak when switching off.

(b) Press the miscroswitch four times; on the fourth operation the alarm must operate. Press the *Alarm Reset* switch on the UN3/521 front panel; the alarm must be silenced. If not check the wiring to the *Alarm*



Notes 1. When component lists are given, perform the checks in the order indicated.
2. To isolate an integrated circuit, nick the printed wiring to V_{cc} pin with a razor blade.. Rejoin the circuit by soldering tinned copper wire across the gap.

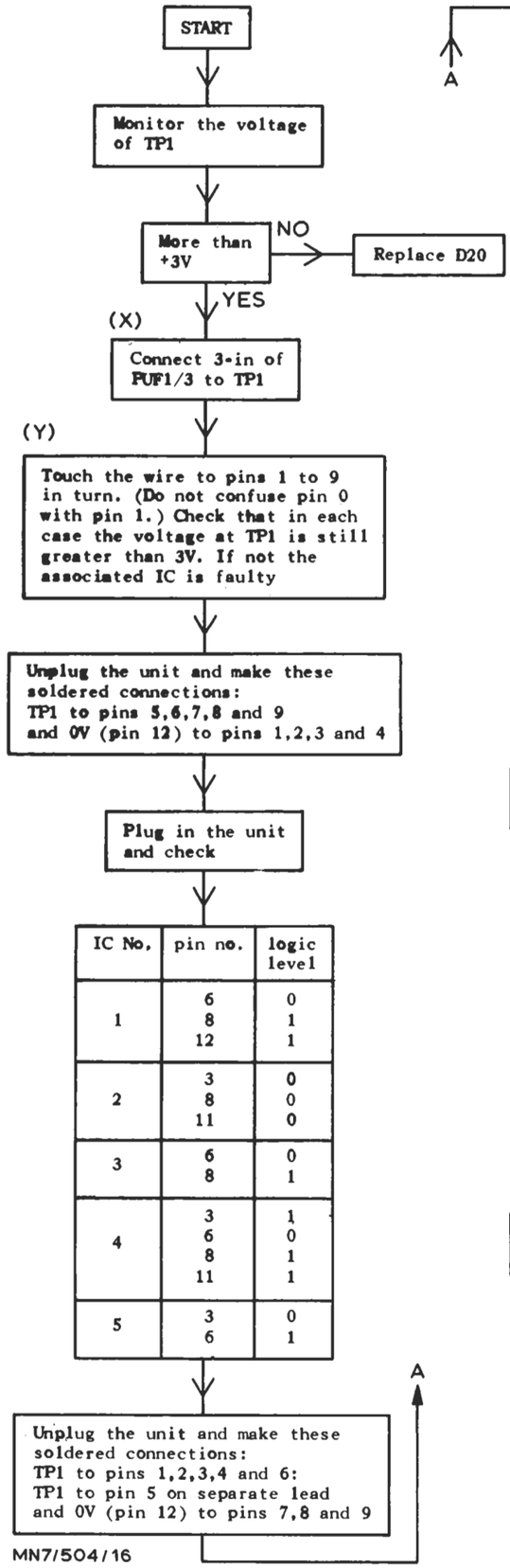
Fig. 16 Guide to D.C. Fault-finding in the UN3/521

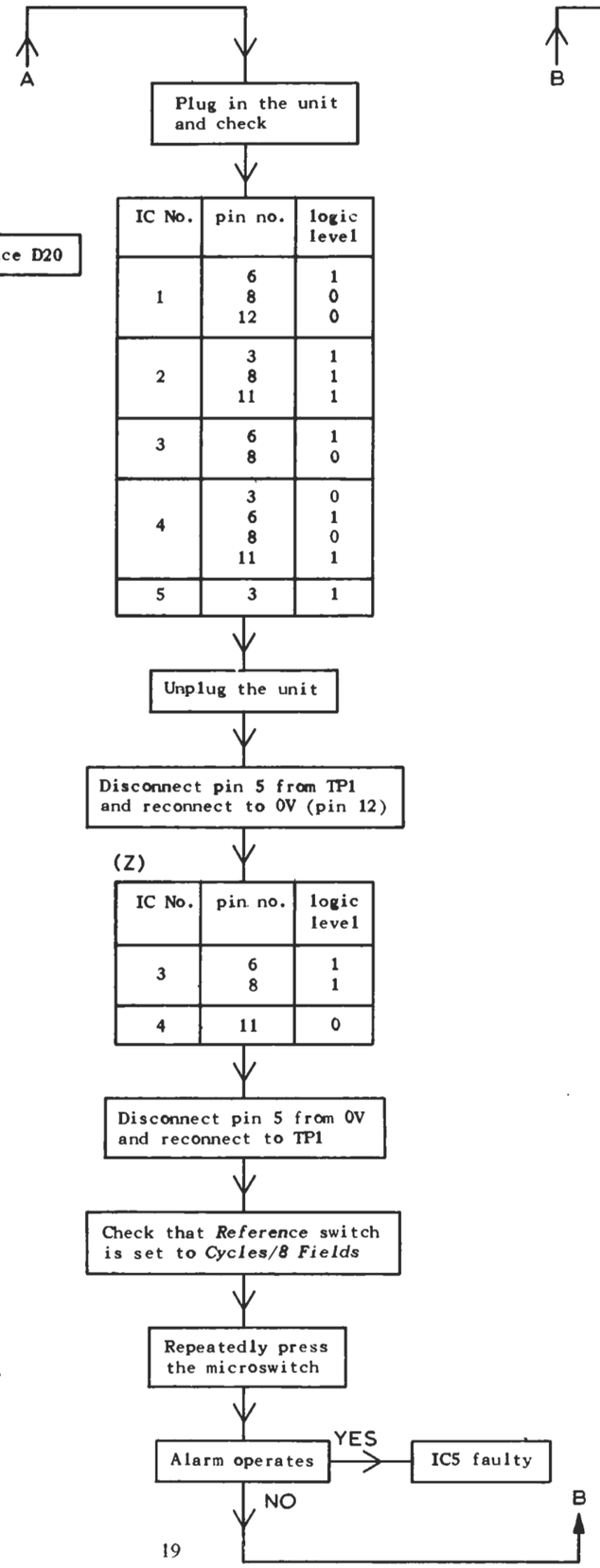


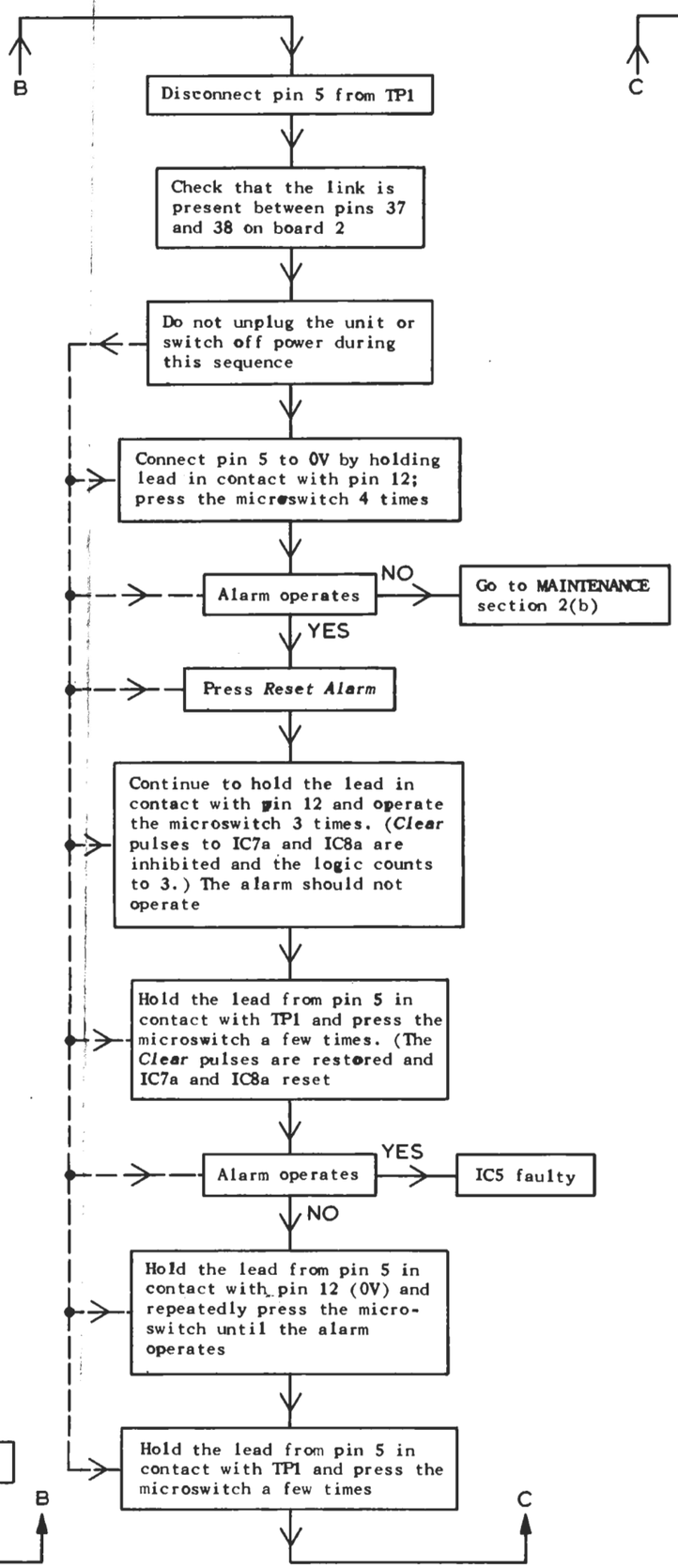
Note. AVO 8 used for all voltage measurements

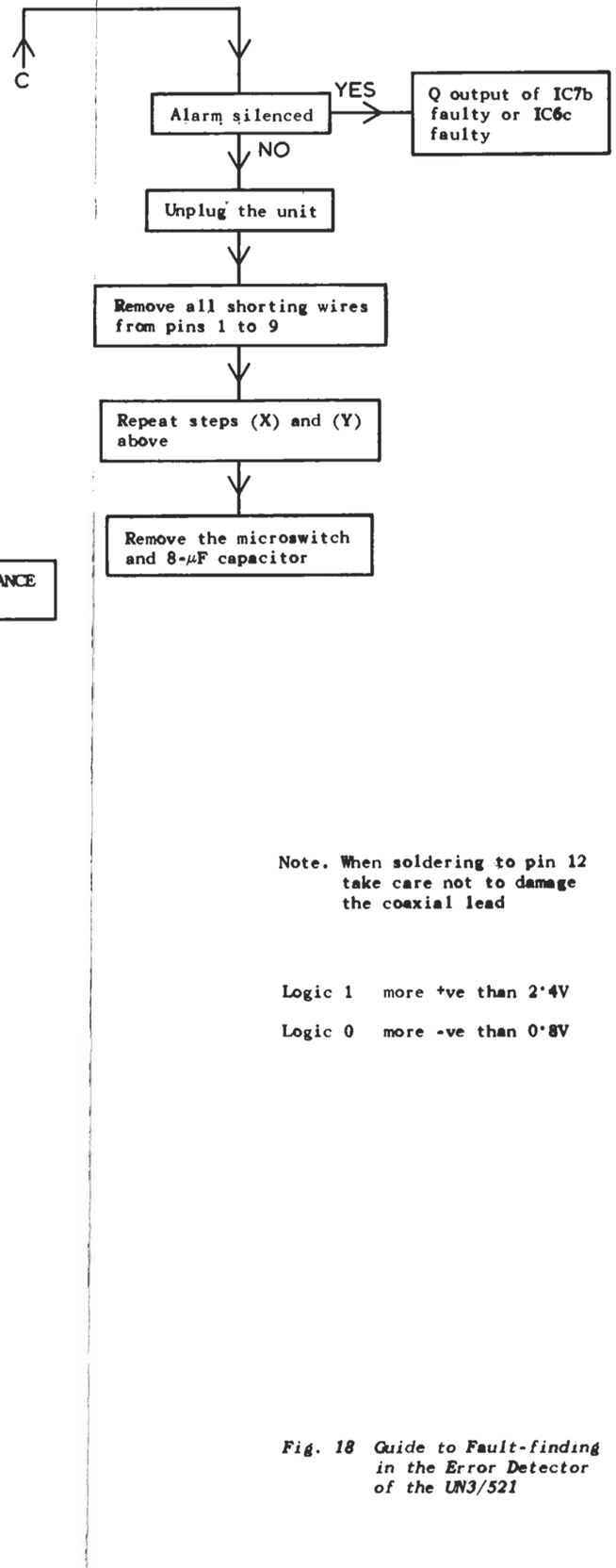
* After replacing faulty components remove shorts on C3 and TR15

Fig. 17 Guide to Fault-finding in the Alarm Logic of the UN3/521









Note. When soldering to pin 12 take care not to damage the coaxial lead

Logic 1 more +ve than 2·4V

Logic 0 more -ve than 0·8V

Fig. 18 Guide to Fault-finding in the Error Detector of the UN3/521

Reset switch and then if necessary refer to Fig. 17. Repeat the check several times to ensure that the circuit counts to four before triggering the alarm.

(c) Check that once the alarm is triggered by the fourth operation it does not reset on subsequent operations.

(d) Turn the *Reference* switch to each of the other positions. At each position ensure that the alarm does not operate. If it does, check the wiring of SA6.

Remove the microswitch and the 8-μF capacitor unless they are required for the next section.

3. *Error Detector*

If a fault is suspected in the error-detector circuitry, fit the microswitch and 8-μF capacitor as detailed in section 2 then follow the check-sequence given in Fig. 18. The pin numbers given are located at the hinge end of Board 2 and TP1 is just below IC1. When changing connections the power must be switched off except where stated otherwise. When connecting and re-connecting the pins to the various voltage points, solder the leads except where stated otherwise; take precautions against short circuits. Check the logic levels with an Avo 8 on the 10-V and 2·5-V ranges for level 1 (greater than 2·4 V) and level 0 (less than 0·8 V) respectively. Take care when soldering to pin 12 not to damage the coaxial lead. Do not confuse pin 0 with pin 1.

References

1. Droitwich Monitoring Receivers RC3/7, RC3/8.
2. Switching Circuits and Logic; Instruction GP.1.
3. Designs Department Technical Specifications:
   MN7M/504 9.113(69)
   UN1/603 9.115(69)
   UN3/521 9.114(69)

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