SECTION 21

BINARY DELAY NETWORK NE4/502

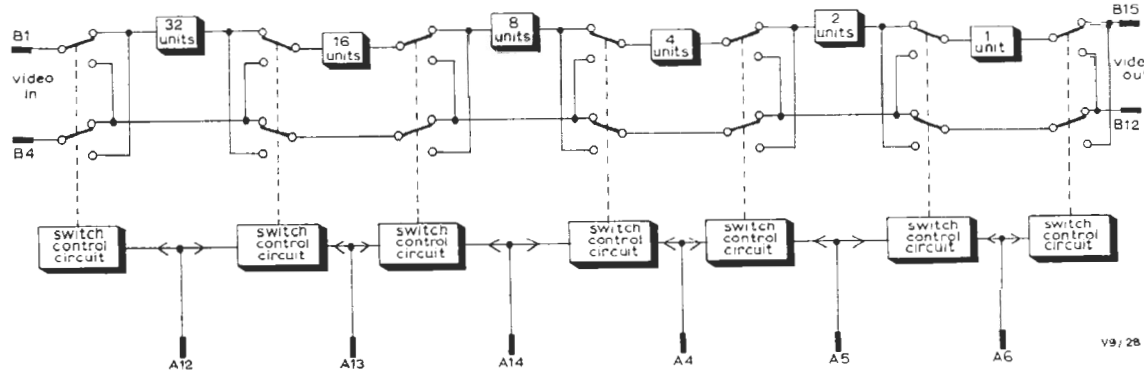


Fig. 21.1 Simplified Block Diagram of the NE4/502

Introduction

The NE4/502 contains two video signal paths sharing a total delay of about 2·2 μs. Control circuits switch the delay between the paths in increments of 35 ns.

The NE4/502 is constructed on a CH1/12D chassis with index peg positions 26 and 27.

General Description

A simplified block diagram of the NE4/502 is shown in Fig. 21.1. In this diagram the delay is shown as multiples of the incremental delay (35 ns). To avoid interchanging the outputs of the two video signal paths with respect to their inputs an even number of switches is operated at all times. This is achieved by making each switching input control two adjacent switches in the chain.

Circuit Description

The basic circuit of the NE4/502 is shown in Fig. 21.2. The behaviour of this circuit is summarised in Table 1.

The full circuit of the NE4/502 is given in Fig. 21.3.

TABLE 1

Inputs PLA 13	PLA 14	$TR23_b$	$TR28_b$	$TR23_c$	$TR23_e$	R76/79	R78/88	$TR27_b$	$TR27_c$	$TR26_c$	$TR21_c$	TR19 TR20	TR24 TR25
−11 v	−11 v	−5 v	−5 v	−7 v	−5 v	−6 v	−6 v	−6 v	+12 v	−17 v	+12 v	conduct	cut off
−11 v	0 v	−5 v	0 v	−7 v	−5 v	−3·5 v	−8·5 v	−3·5 v	−3·5 v	+12 v	−24 v	cut off	conduct
0 v	−11 v	0 v	−5 v	−11 v	−1 v	−8·5 v	−3·5 v	−3·5 v	−3·5 v	+12 v	−24 v	cut off	conduct
0 v	0 v	0 v	0 v	−10·5 v	−1·5 v	−6 v	−6 v	−6 v	+12 v	−17 v	+12 v	conduct	cut off

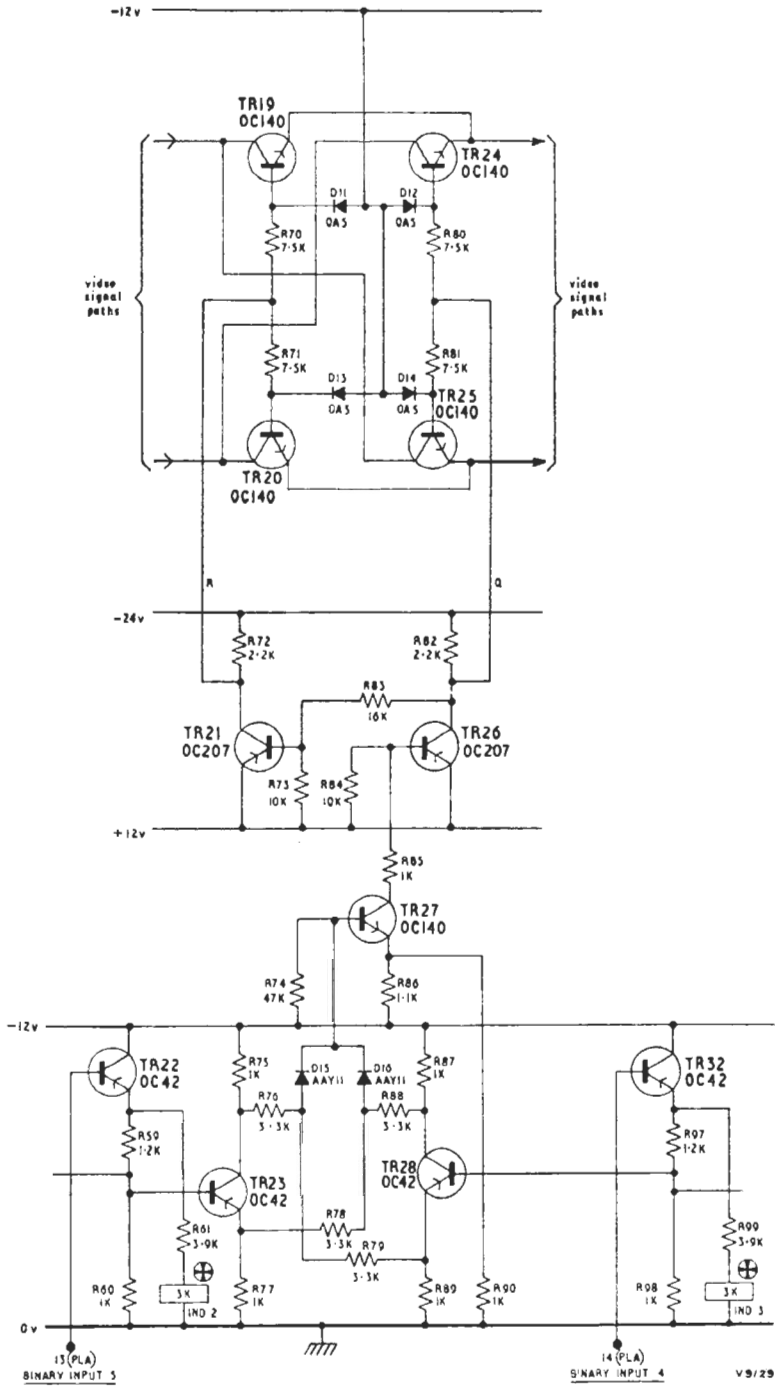
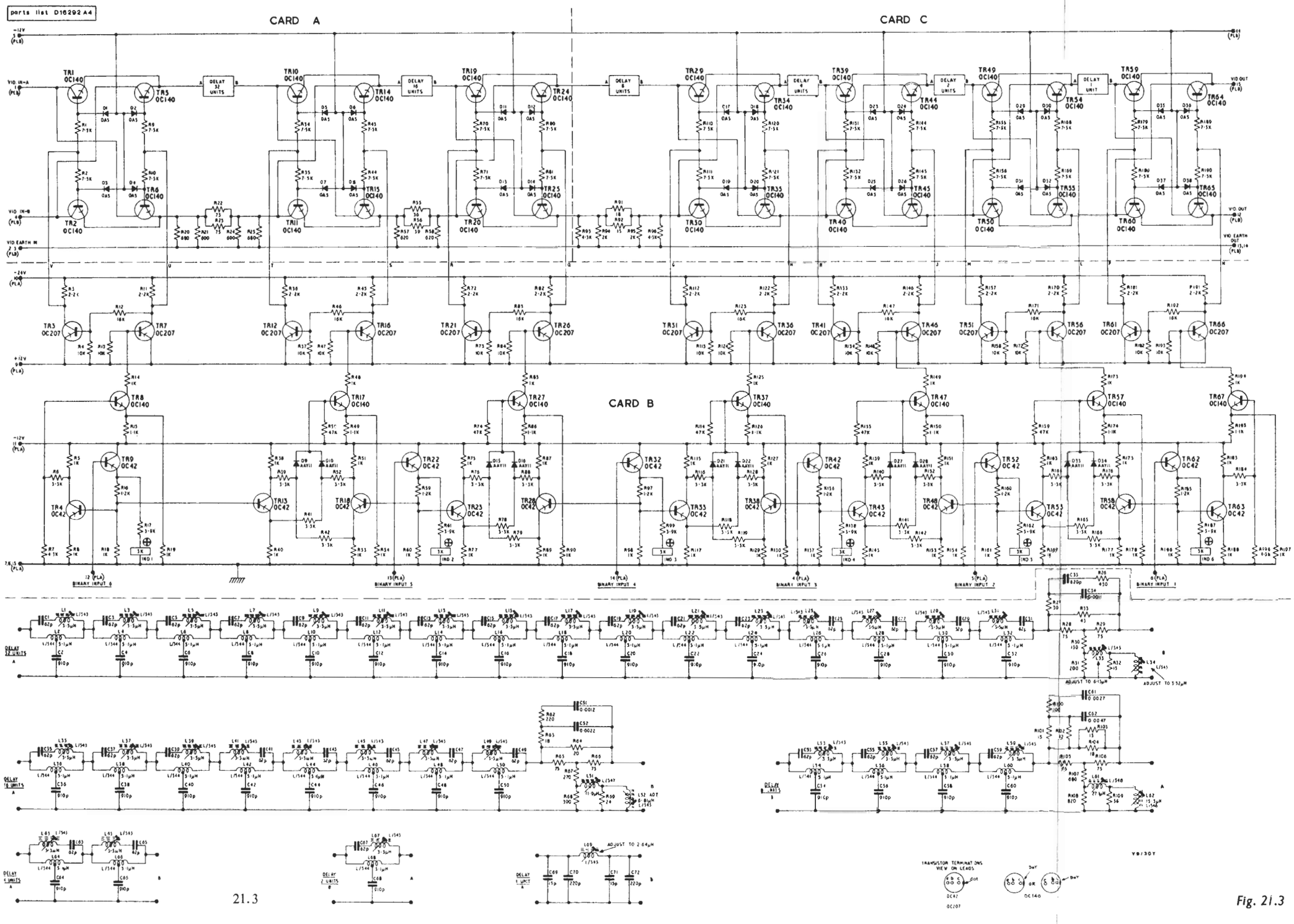


Fig. 21.2 Basic Circuit of the NE4/502



21.3

Fig. 21.3 Circuit of the NE4/502

The delay networks are designs based on data published in Designs Department Technical Memorandum No. 9.19(61); they have a delay of 70 ns per section, except for the unit delay. The unit delay network is a low-pass filter with a cut-off frequency of about 9 MHz.

Test Schedule

Apparatus Required

Tektronix oscilloscope Type 515.
24-volt and 12-volt (two) power supplies.
Pulse and Bar Generator GE4/504B.

Test Procedure

1. Connect the power supplies as shown in Fig. 21.3.
   Connect two 0·1 μF capacitors between pins PLB 3 and PLB 5 and between pins PLB 11 and PLB 13.
   Connect pins PLA 8 and PLB 13.
   Connect the output of the GE4/504B to video input B terminated in 75 ohms.
   Connect the oscilloscope input, terminated in 75 ohms, to video output B.
   Synchronise the oscilloscope from the input signal.
   Terminate both video input A and video output A in 75 ohms.
2. With a 1-volt input signal measure the amplitude of the output signal. It should be approximately 0·4 volts p-p. Connect pin PLA 11 to each of the pins shown in Table 2. Observe the output waveform and check that it is delayed by the amount shown in the table. Check also that the pulse-to-bar ratio is not less than 0·95 for any delay section and that the amplitude does not change by more than 0·2 dB.

TABLE 2

Pin 11 connected to pin	*Delay (approx.)* (μs)
12	1
13	0·5
14	0·25
4	0·125
5	0·06
6	0·03

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