OS1/516 LINE-LOCKED OSCILLATOR

Introduction

The OS1/516 forms part of the CO2/543 Line-to-Natlock Reference Converter and comprises:

(a) A locked oscillator which accepts mixed syncs and produces Natlock Frequency at a multiple (567/2) of the line component of the mixed sync input.

(b) Gating circuits which accept two separate feeds of PAL subcarrier and a set of control signals and provide one or neither of the two subcarrier feeds depending upon the combination of control signals present.

Power for the OS1/516 is provided by a PS2/22B Regulated Power Supply which is constructed integrally with the rest of the unit on a CH1/26B Chassis with Index-peg positions 30 and 32.

General Specification

Signal Input	625-line mixed syncs
Nominal Signal Input Level	2 volts p-p
Signal Input Impedance	75 ohms
Signal Output	Natlock Frequency sine-wave (567/2 x input line frequency)
Signal Output Level	1 volt p-p
Signal Output Impedance	75 ohms
Gate Inputs	Station Colour Subcarrier Synthetic Colour Subcarrier derived from the Natlock Frequency output of the OS1/516
Nominal Gate Input Level	1 volt p-p
Gate Input Impedance	75 ohms
Gate Output	Selected Colour Subcarrier or no output
Gate Output Level	As input
Gate Output Impedance	75 ohms
Gate Control inputs (0V/-12 V nominal)	Local/Genlock Burst/No Burst
Gate Control derived within OS1/516	Video/No Video
Mains Input	240 volts a.c. fused at 150 mA
Weight	1·4 kg (3 lb)
Temperature Range	0°C to 45°C

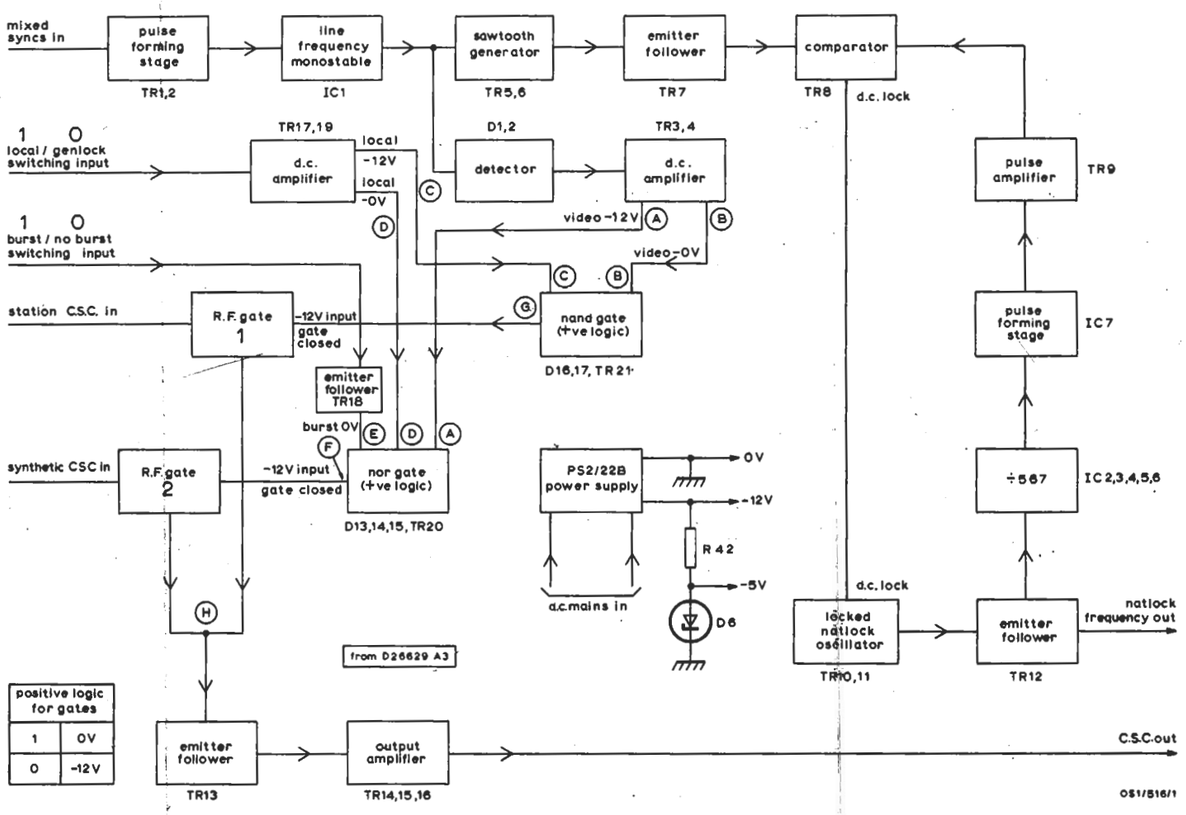

Fig. 1. Block Diagram of the OS1/516

General Description

Fig. 1 shows a block diagram of the OS1/516.

(a) Locked Oscillator

Syncs are shaped by a pulse-forming stage and used to trigger a 35-μs monostable IC1. IC1 output drives a line-frequency sawtooth generator, TR5 and TR6.

TR10 and TR11 form a Natlock Oscillator which operates at a nominal frequency of 4·4296875 MHz. This signal is divided by 567 (in IC2 to IC6) and then used to drive a monostable IC7. Pulses of duration 2.3 μs from this monostable occur at approximately half-line rate (depending on the accuracy of the Natlock Oscillator) and after amplification are used to sample the line-rate sawtooth in TR8.

The d.c. level sampled from the sawtooth is a direct indication of the phase-error between the sawteeth (derived from syncs) and the pulses from IC7 (derived from the Natlock Oscillator). The samples are integrated and used to adjust the bias on a varicap diode in the Natlock Oscillator to achieve phase-lock between the sawteeth and the pulses from IC7 and between line sync and the Natlock Frequency output.

(b) Gating Circuits

The Local/Genlock and Burst/No Burst control inputs are switched to 0 V or −12 V outside the OS1/516, but the Video/No Video control signals are derived within the unit. An output of monostable IC1 is applied to a detector formed by D1 and D2, the output of which is integrated and fed to a d.c. amplifier TR3 and TR4. TR3 output (designated *A* in Figs. 1 and 2) is −12 V when syncs are present at the input of the unit and 0 V when they are not. Conversely TR4 output (designated *B* in Figs. 1 and

2) is 0 V when syncs are present and −12 V when they are not. Points A and B are connected to the gating circuits as shown in Fig. 1.

The combinations of control signals possible and their effects on the gating circuits are summarised in Table 1

TABLE 1

Gate Conditions for Corresponding Control Signal Inputs

	Burst		*No Burst*		
	Video				*No Video*
Genlock	NOR gate inputs	1 0 0	NOR gate inputs	0 0 0	NOR gate inputs 0 0 0
	NOR gate output	0 (−12 V)	NOR gate output	1 (0 V)	NOR gate output 0 (−12 V)
	NAND gate input	1 1	NAND gate inputs	1 1	NAND gate inputs 1 0
	NAND gate output	0 (−12 V)	NAND gate output	0 (−12 V)	NAND gate output 1 (0 V)
	R.F. gate 1	closed	R.F. gate 1	closed	R.F. gate 1 open
	R.F. gate 2	closed	R.F. gate 2	open	R.F. gate 2 closed
	Output	nil	Output	synthetic c.s.c.	Output station c.s.c.
Local	NOR gate inputs	1 1 0	NOR gate inputs	0 1 0	NOR gate inputs 0 1 1
	NOR gate output	0 (−12 V)	NOR gate output	0 (−12 V)	NOR gate output 0 (−12 V)
	NAND gate inputs	0 1	NAND gate inputs	0 1	NAND gate inputs 0 0
	NAND gate output	1 (0 V)	NAND gate output	1 (0 V)	NAND gate output 1 (0 V)
	R.F. gate 1	open	R.F. gate 1	open	R.F. gate 1 open
	R.F. gate 2	closed	R.F. gate 2	closed	R.F. gate 2 closed
	Output	station c.s.c.	Output	station c.s.c.	Output station c.s.c.

Note: Gate inputs on this Table are in the order in which they are shown on Fig. 1, i.e. E, D, A for the NOR gate and C, B for the NAND gate.

Circuit Description

The circuit of the OS1/516 is shown in Fig. 2.

(a) Locked Oscillator

The mixed-sync input is amplified and inverted by TR1, differentiated by C2 and R5 and applied to emitter follower TR2. Positive-going spikes at the emitter of TR2 correspond to the leading edges of sync pulses at the input and are used to trigger the monostable IC1. The unstable period of IC1 is set to about 35 μs, i.e. greater than half a line period so that it is not triggered by equalising or broad pulse serration pulses during field syncs. Thus the output of IC1 (pin 8) is a continuous train of 35-μs duration pulses provided that either line or field syncs are being received.

IC1 output pulses are differentiated by C6 and R13 to produce positive and negative going pulses of about 1-μs duration. The positive-going pulses are removed by D3. The negative-going pulses, which are timed to the leading edge of syncs, are used to trigger a line-rate sawtooth generator formed by TR5, TR6 and C7. Transistor TR6 provides a constant current to charge C7 which thus has a roughly linear rise in voltage across it with time. Once per line, when TR5 is switched hard on by a negative pulse at its base, C7 is discharged through TR5 thus ending the sawtooth. At the end of the negative pulse TR5 turns off and the charging process re-starts. The sawtooth waveform is fed via emitter follower TR7 to the source of TR8.

TR10, TR11 and associated circuitry form a Natlock Oscillator the output of which is fed via emitter follower TR12 to the ÷ 567 system IC2 to IC6. A tap on the emitter resistor of TR12 provides the Natlock Frequency output of the unit.

IC2 to IC6 are identical dual J-K flip-flop integrated circuits. IC2 and IC3 are each connected as a synchronous modulo-3 counter[1] and together, therefore, divide by 9. The bistable elements of the remaining ICs (4, 5 and 6) are cascaded and so would divide by 2^6 (64). Knockback from IC6 output to the first bistable element of IC4 reduces this to 63.

IC6 output is fed to a monostable comprising IC7, C11 and R23. Pulses of approximate duration 2·3 μs from IC7 are d.c. restored by C10, R22 and D4 so that pulses on the base of TR9 are negative-going from earth. These pulses are amplified and inverted by TR9 before being applied to the gate of TR8 where they are used to sample the sawtooth on TR8 source. The drain of TR8 is connected via R29 and R30 to the varicap diode D5, the bias on which adjusts the frequency of the Natlock Oscillator. C9, R30 and C14 integrate the sampled sawtooth at the drain of TR8 to provide a steady bias for the varicap. R29 isolates C14 from the varicap to prevent the capacitance of C14 from affecting the oscillator frequency.

(b) Gating Circuits

Encircled letters on Fig. 2 correspond with those on Fig. 1 and indicate salient points in the gating circuitry.

The *Local/Genlock* control signal is inverted by TR17 to provide −12 V for *Local* and 0 V for *Genlock* suitable for application to one input of the NAND gate (point C). TR19 inverts the output of TR17 to provide 0 V for *Local* and −12 V for *Genlock* suitable for application to one input of the NOR gate (point D).

The *Burst/No Burst* control signal passes via emitter follower TR18 to another input of the NOR gate (point E).

Video/No Video control signals are derived by rectification of IC1 output pulses by D1 and D2. The rectified pulses are integrated by C5 and R8 to provide a steady d.c. bias which holds TR3 on which in turn holds TR4 off. This results in point *A* being at −12 V and point *B* at 0 V. In the absence of syncs at the input of the unit pulses at IC1 output cease, TR3 turns off and TR4 turns on. This results in point *A* being at 0 V and point *B* at −12 V.

The NOR gate comprises D13, D14, D15, R75 and TR20. The diodes and R75 perform an OR function, TR20 inverts the OR gate output. The NAND gate comprises D16, D17 and TR21.

The r.f. gates comprise D7 to D12 and associated circuitry. They are connected back-to-back, the subcarrier inputs being applied via C30 and C33. The common output from the two gates is taken from the junction of D9 and D10 (point H).

The circuit of a single r.f. gate (the synthetic

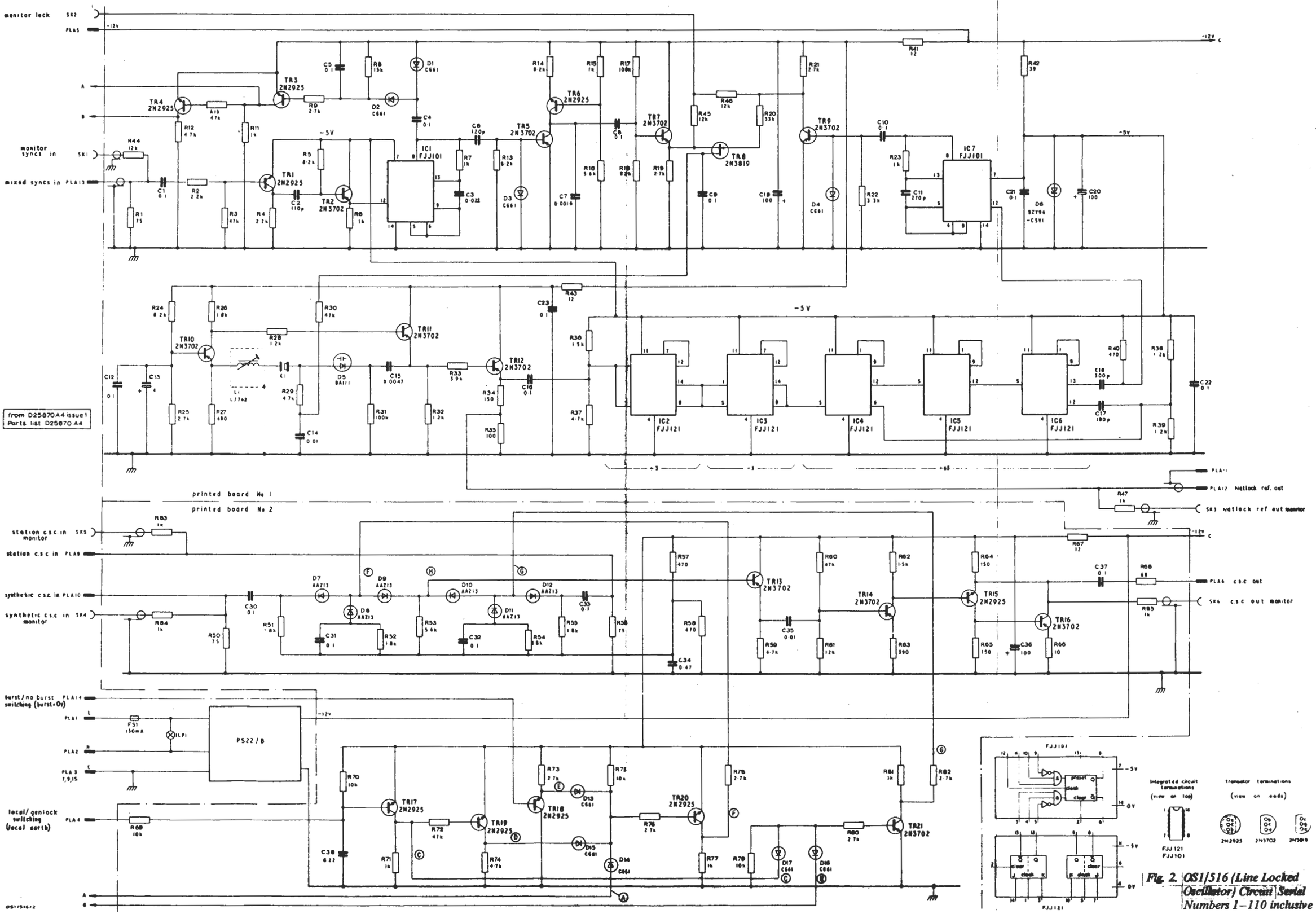

Fig. 2. OS1/516 (Line Locked Oscillator) Circuit Serial Numbers 1–110 inclusive

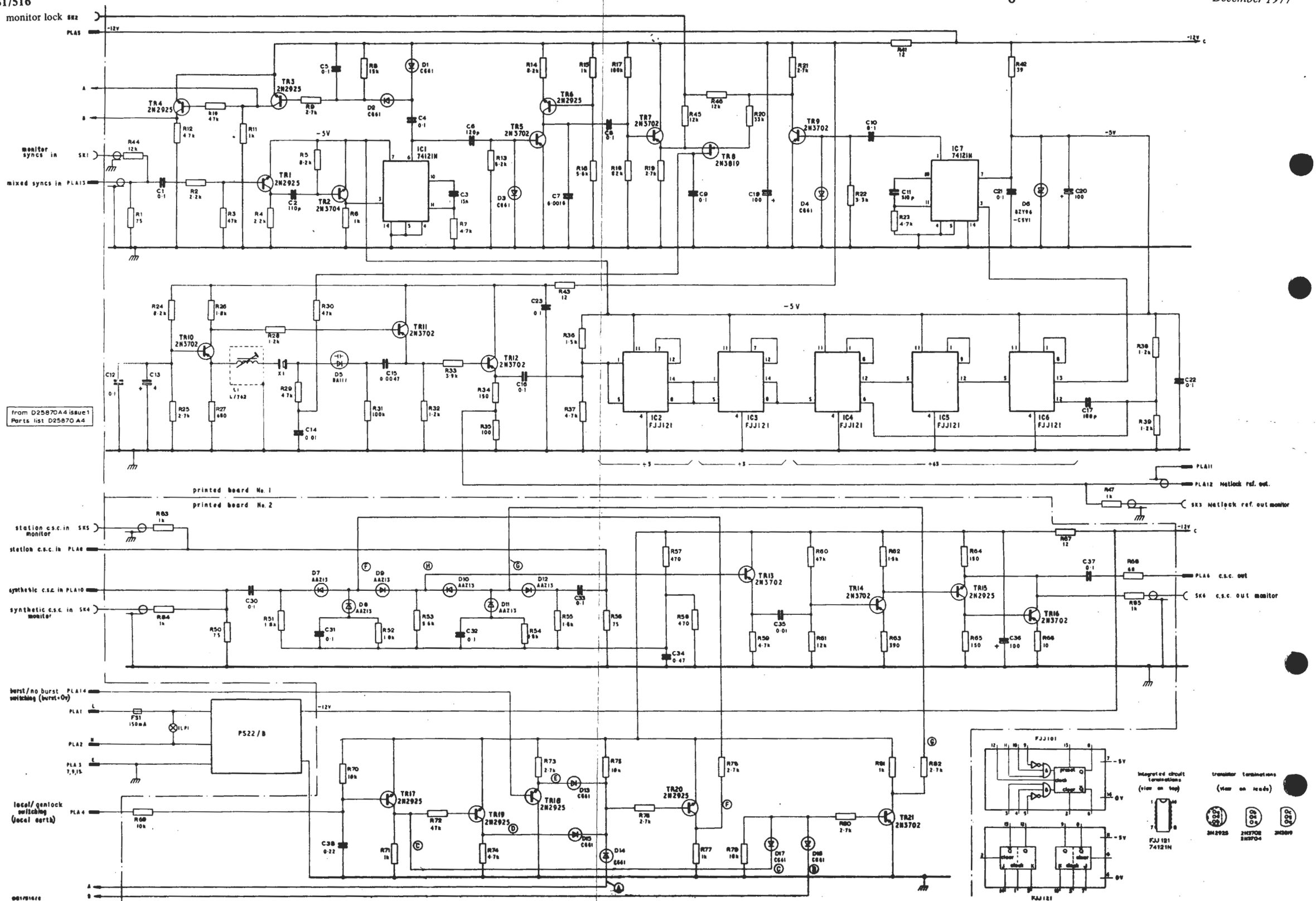

Fig. 2a OS1/516 (Line Locked Oscillator) Circuit Serial Numbers 111 on.

subcarrier gate) is shown in Fig. 3(a). The gate is opened by a control input of 0 V which forward-biases D7 and D9 and reverse-biases D8. The effective circuit of the gate is then as shown in Fig. 3(b). The gate is closed by a control input of −12 V which reverse-biases D7 and D9 and forward-biases D8. The effective circuit of the gate is then as shown in Fig. 3(c). Note that even when D7 and D9 are reverse-biased they still present an impedance, albeit high, between the input and output terminals of the gate. This problem is overcome by the action of D8, C31 and R52. When D8 is forward-biased C31 and C34 provide a low-impedance path to earth from the junction of D7 and D9 so shunting any subcarrier which breaks through D7. R52 provides a path for the d.c. control current through R8.

Test Procedure

The OS1/516 is tested as part of its parent unit.

References

1. Mullard TTL Integrated Circuits Applications, 2nd edition, p. 136.
CO2/543 Line-to-Natlock Converter.

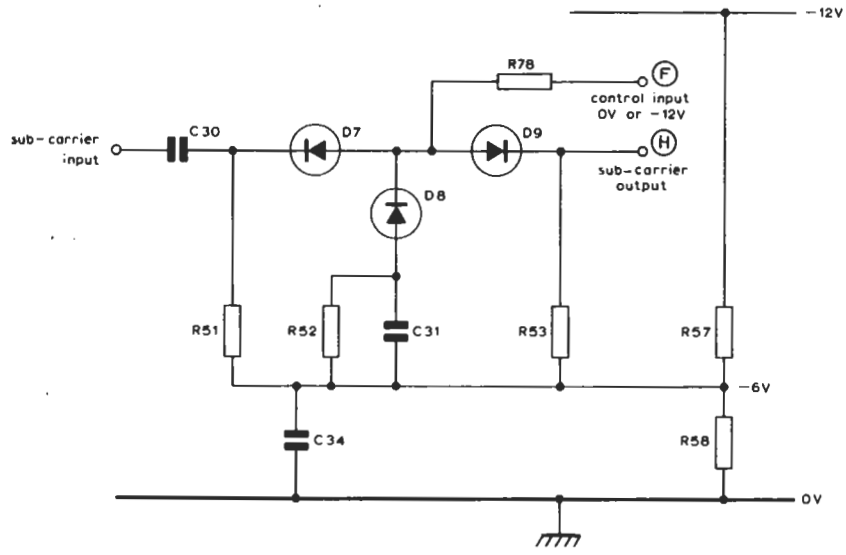

Fig. 3(a) R.F. Gate Circuit

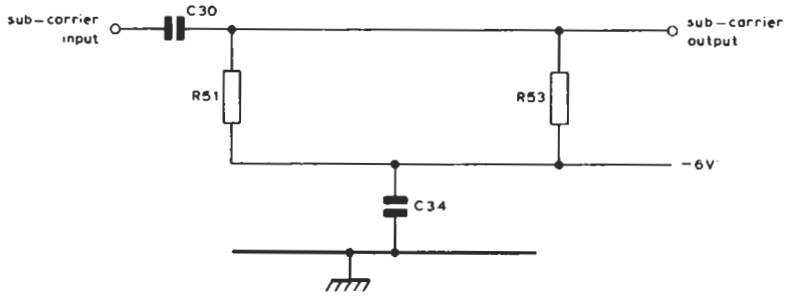

Fig. 3(b). R.F. Gate Effective Circuit with Control Input of 0 V

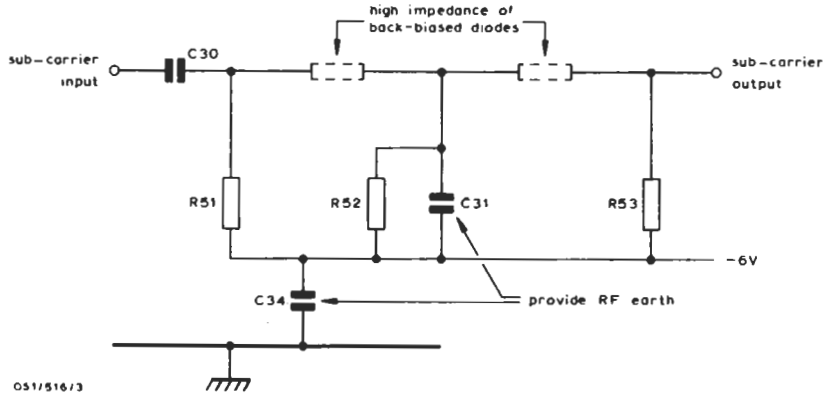

Fig. 3(c) R.F. Gate Effective Circuit with Control input of −12 V