SECTION 3

BLACK LEVEL CLAMP AND COMPRESSION UNIT UN13/503

Introduction

The UN13/503 accepts two independent but nominally-identical composite video signals, known as the *reference signal* (R channel) and the *compared signal* (C channel), clamps them at black level and, by means of transistor-switched attenuators, compresses higher levels of picture and sync signals leaving full gain at the lower levels. The unit operates on the 405 and 625 line-standards.

The C-input signal is compared with itself after being clamped and any low-frequency difference signal that results appears at a subsidiary output.

The unit is housed on a CH1/12A chassis with index peg positions 16 and 22. It forms part of a Television Automatic Monitor (Transmitter) MN2M/505 which is described in Instruction V.11.

General Specification

Input signal (both channels)	3 volts p-p $\pm$ 4 dB
Output signals (for nominal input)	1·75 volts p-p
Supply	80 mA at +24 volts

Circuit Description

The circuit of the unit is given in Fig. 3.1. Black level clamps are used on the inputs and, to ensure symmetry, a common clamping voltage is used fixed by the zener diode D2. D1 provides just sufficient voltage across the base-emitter junction of the clamping transistors to ensure that they are completely cut off when idling. The clamping pulses are obtained from emitter-coupled monostable pulse generators triggered by the trailing edge of the sync pulses. The triggering pulses are obtained from the inputs by the action of TR18, TR17 and TR16 for the R channel and of TR19, TR20 and TR21 for the C channel.

In the R channel, the signal is inverted by TR18 and passed to an impedance changer TR17. Sync separation is carried out by TR16, which operates by d.c. restoring on the tips of syncs, thus pushing the negative-going picture signal into the cut-off region. The sync signals at the collector of TR16 are differentiated by C12/R38 and the positive edge is used to trigger the pulse generator, TR15 and TR14. The positive pulse from the collector of TR14 is fed via the emitter follower, TR13, to operate the clamp.

After clamping, the signals are fed via emitter followers to the compression circuits, comprising TR4, TR5, TR6, and TR9, TR7, TR8.

During the picture period, the base of the output emitter follower TR4 (and TR9) is driven positively along with the emitters of TR5 and TR6. Above a certain reference level, set by the ratio of R9 and R10, TR6 starts to conduct and the resistance between the lower end of R2 and earth is progressively reduced. Thus, with respect to the signal at the input of the unit, the signal on the base of TR4 rises more slowly above the reference level than below. TR5 is cut off during the picture period.

During the sync period, the potential at the base of TR4 and at the emitters of TR5 and TR6, changes negatively. TR6 is cut off but TR5 starts to conduct at a point set by the ratio of R11 and R12. As the collector-emitter resistance of TR5 drops, the potential at the base of TR4 becomes static, the positive potential via TR5 balancing the negative potential due to the sync pulse. The amplitude of the sync pulses at the emitter of TR4 is thus limited.

A common reference potential is used for both compression circuits; thus any drift of black level with respect to the reference potential affects both channels equally.

Measurement of low frequency errors is made by comparing the signal in the C channel before and after it has been clamped. The comparison is made in a simple resistive T-network. The high frequency components of the signal are of no importance at this point and are attenuated by C18.

Test sockets on the front panel of the unit give access to clamped video and compressed video for both channels.

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See page 3.3 for Fig. 3.1.

parts list D16259A4

+24V 6

INPUT A 14 (reference)

C1 0·1

R1 120K

D1 OA200

D3 OA200

TR1 2N706A

TR2 2N706A

TR3 2N706A

R2 2·2K

D2 OAZ204

C2 50

R4 1K

R5 2K

C20 56p

TR4 2N2218

TR5 OC141

TR6 OC43

R6 470

R7 1K

R8 120

R9 1·8K

R10 5·6K

C3 50

R11 1·6K

R12 3·9K

C4 50

R13 1K

R14 1·6K

C5 50

R15 3·9K

C6 50

R16 1·8K

TR7 OC141

TR8 OC43

R17 5·6K

R18 120

R19 1K

TR9 2N2218

R20 470

C21 56p

R21 2K

R22 1K

TR10 2N706A

TR11 2N706A

TR12 2N706A

R23 2·2K

C7 50

R24 120K

C8 0·1

C9 100

R25 100

10 INPUT C (compared)

15

OUTPUT A 12

R27 53

SKT 1 CLAMPED REF

R26 33

SKT. 3 CLAMPED COMP

R29 33

R28 33

8 OUTPUT C

SKT 2 COMPRESSED REF

SKT. 4 COMPRESSED COMP

R59 100

R30 470

R58 470

R31 100

TR13 2N706A

TR14 2N706A

TR15 2N706A

TR16 2N706A

TR17 2N706A

TR18 2N706A

R33 4·7K

R35 18K

R37 6·8K

R39 180k

R41 3·3K

R43 5·6K

C10 50

C11 1500p

C12 100p

C13 4·7

R63 100

R32 4·7K

R34 1K

R36 2·2K

R38 18K

R40 3·3K

R42 2·2K

R44 3·3K

C18 150p

C19 150p

R45 5·6K

R47 3·3K

TR19 2N706A

TR20 2N706A

R46 3·3K

R48 2·2K

R50 180k

R51 6·8K

TR21 2N706A

TR22 2N706A

TR23 2N706A

TR24 2N706A

R53 18K

R55 4·7K

C15 100p

C16 1500p

R64 100

C14 4·7

R49 3·3K

R52 18K

R54 2·2K

R56 1K

R57 4·7K

C17 50

C18 47000p

4 LF ERROR

R60 4·7K

R62 10K

R61 10K

V14/57 T

Fig. 3.1 Circuit of the UN13/503