SYNC SEPARATOR UNIT UN16/514

Introduction

The UN16/514 forms part of a sound-in-syncs coder[1]; it accepts a composite video signal, together with a standby signal either of mixed-syncs or of line-drive, and provides the following outputs:

positive-going mixed-sync pulses
positive-going 1-μs pulses which have leading edges coincident with the leading edges of syncs
a sync-fail indication.

Sync pulses are separated from the video input signal by means of a circuit which clips the syncs at their mid-amplitude point. The clipping level is proportional to the amplitude of the sync-pulse component of the input signal and so clipping is carried out at the correct point for a wide range of input signal amplitudes.

If separated sync pulses fail to appear at the output of the clipper, a changeover circuit routes a standby feed of mixed-sync (or line-drive) pulses to the output of the unit. At the same time an indication is given that the separated-syncs feed has failed.

The unit is constructed on a printed-wiring board fitted with a 25-way ISEP connector and with index-peg positions 3, 11 and 13. Power supplies at +12V and −5V are required.

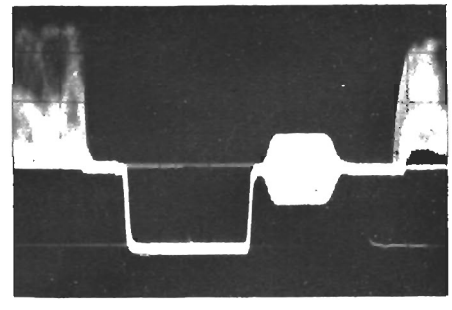
General Specification

Input Signals

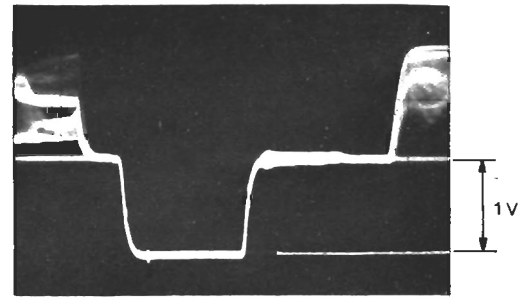
Video Input	1V p-p nominal (signal range +6 dB to −8 dB)
Standby Input (Mixed-syncs or Line-drive)	2V p-p negative-going
Input Impedances	10 kilohms
Maximum d.c. at Input	+4V to −6V
Output Signals	
Syncs	positive-going 3·5V p-p
1-μs Pulses	positive-going 3·5V p-p, leading edge coincident with leading edge of syncs
Sync-fail Indication	normally +3·5V, falling to 0V as separated-syncs fail
Delay (Input to Sync Output)	150 ns
Output Recovery Time	less than 10 ms (typically 4 ms) for a signal interruption of any duration
Failure Alarm Time-constant	Approximately 2·ms (30 lines)
Typical Signal Degradation Before Failure	
Peak Signal/r.m.s. Noise (unweighted white noise)	25 dB
50-Hz Hum	300 mV p-p
Added Square Wave	100 mV p-p
Operating Temperature Range	0°C to 45°C
Power Consumption	110 mA at +12V, 40 mA at −5V

Circuit Description

A circuit diagram of the UN16/514 is shown in Fig. 1. Typical waveforms of the signals present at the input, at the syncs output, and at test-point A are shown in Fig. 2.



(a) Video input signal



(b) Test point A

(c) Separated sync output (output unloaded)

Fig. 2 Waveforms

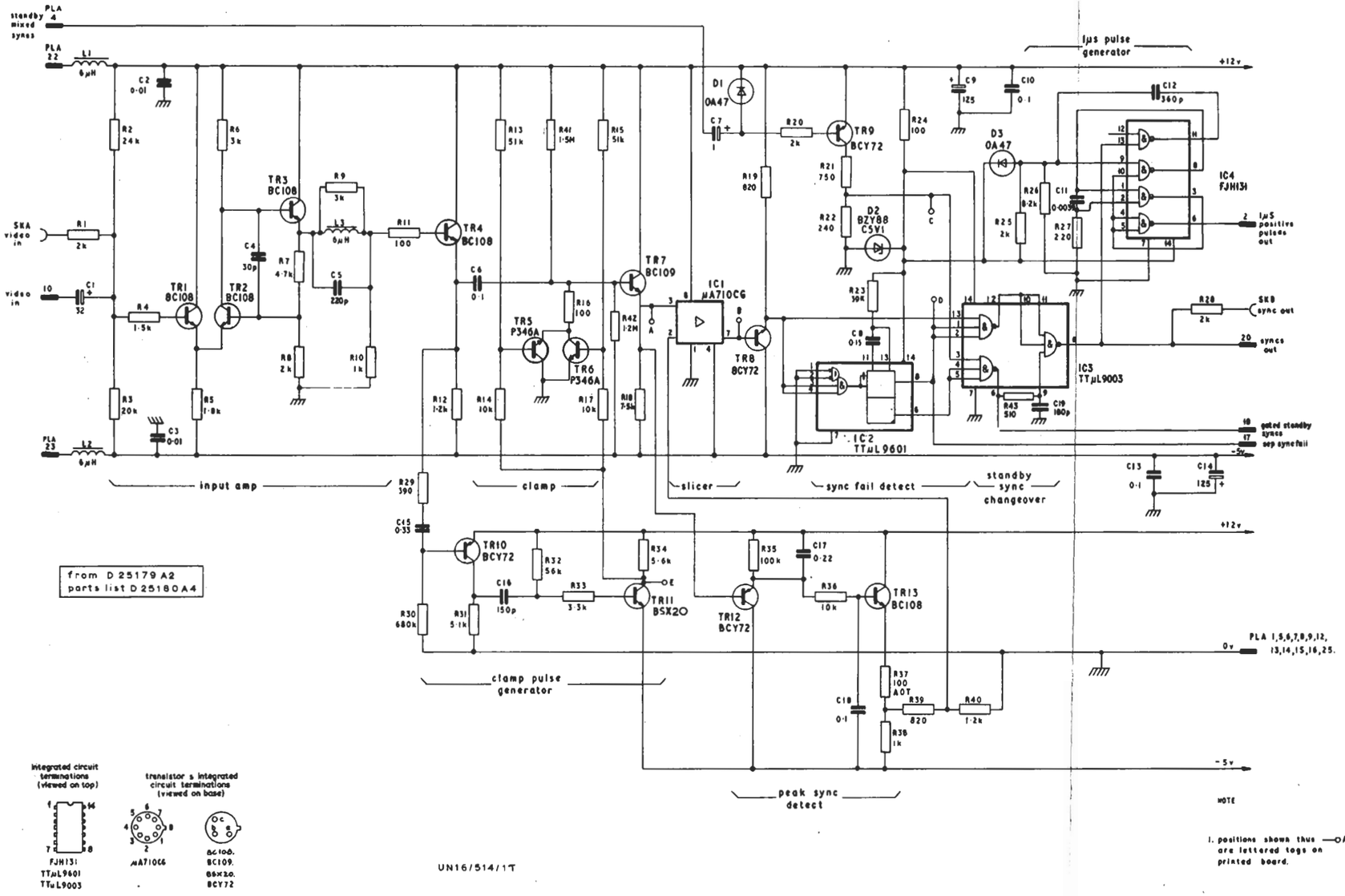


Fig. 1 Circuit of the UN16/514

Input Amplifier

The input amplifier is formed by transistors TR1 to TR3. Transistors TR1 and TR2 form a long-tailed pair and TR3 is an emitter-follower. Negative feedback is taken from TR3 emitter to TR2 base and the gain of the amplifier (about 10 dB) is determined by the ratio of R7 to R8. Frequency response is controlled by C4 and by the tuned circuit L3, C5, R9. These components provide a progressive roll-off starting at 2·2 MHz with a notch at 4·4 MHz, as shown by Fig. 2b. The amplifier is biased so that a certain amount of white-level clipping takes place.

Clamp and Clamp Pulse Generator

The output of TR3 is passed via emitter-follower TR4 to the base of TR7. At this point the signal is clamped by the action of transistors TR5 and TR6, these form a bi-directional switch that operates during the back-porch period. Depending on the polarity of the signal with respect to zero volts, the applied positive-going clamp pulses cause either TR5 or TR6 to conduct and the back porch of the video signal is clamped to zero volts.

Transistor TR10 is fed with composite video from the emitter of TR4 and functions as a sync separator. The sync pulses developed at the collector of TR10 are differentiated and the negative-going spikes (back edges) drive TR11 into cut-off. Thus the required positive-going clamp pulses are fed to TR5 and TR6.

Sync Clipper

Integrated circuit IC1 is a differential comparator which functions as a sync clipper. The device compares the sync-pulse amplitude of the clamped video signal with a d.c. reference signal which has half the amplitude of syncs and which is derived from the sync-level detector. When the sync component of the input signal goes more negative than the reference level, the output of IC1 goes positive and thus positive-going sync pulses with a peak-to-peak amplitude of 3·5 volts are developed; these pulses are fed via emitter-follower TR8 to the standby-sync-changeover stage.

Sync Level Detector

Transistor TR12 conducts during sync-pulse periods and charges capacitor C17 to a potential which is proportional to the peak sync-pulse amplitude. Smoothing is carried out by R36 and C18, and the offset potential due to TR12 is removed by TR13. The signal is then fed, via a potential divider network which reduces it to half-sync amplitude, to the sync-clipper stage.

Sync Failure Detector

The sync-failure detector consists of integrated circuit IC2 which functions as a re-triggerable monostable multivibrator; unlike a conventional monostable the timed state is commenced afresh by each input pulse so that, if the time interval between inputs is shorter than the time-constant of the circuit, the monostable remains in the timed state. In this instance the time-constant is 2 ms so that a change of state takes place only if a break of more than 30 lines occurs in the video input to the unit.

Standby Sync Changeover

Intergrated circuit IC3 accepts the clipper output together with the Q and $\overline{Q}$ outputs from the sync failure detector, and a feed of standby syncs. If the input syncs fail, this circuit routes standby syncs to the output of the unit to replace the clipper output and provides also a sync-fail signal. Resistor R43 and capacitor C19 compensate for the delay introduced into the normal signal path by the sync-separation process and so ensure that the correct sync-to-marker-pulse timing is maintained in the sound-in-syncs waveform when standby syncs are being used.

1- μs Pulses

Integrated-circuit IC4 is a monostable device which consists of four NAND gates; it is triggered from the leading edge of the output sync pulses and provides 1- μs pulses for use in an associated unit[2]. The operation of the circuit is given below.

Positive-going sync pulses are inverted in gate 11, 13 and are then fed via a differentiator to gate 9, 10, 8. The inputs to this gate are normally high (logic 1) and the output normally low (logic 0) but the negative-going edge of the differentiated pulse changes the state of the gate and causes a logic 1 to appear at 8. This is applied directly to input 1 of gate 1, 2, 3 and (via C11) to input 2; therefore the output of gate 1, 2, 3 falls to logic 0 and remains at logic 0 for a period (1 μs) which is determined by the time constant of C11 and R27. The logic 0 output from 3 is inverted by gate 4, 5, 6 to provide a positive-going 1-μs pulse output.

Maintenance and Alignment

Clipping Level Adjustment

The clipping level should be checked if components associated with TR12 or TR13 are changed, or if IC1 is replaced. To check the clipping level proceed as follows:

Monitor either test-point B or the *Sync Output* with an oscilloscope probe.

Switch the oscilloscope timebase to *Internal* and adjust the timebase so that the pulse occupies the full width of the display.

Operate the Y-timebase magnifier and observe the trailing edge of the pulse.

Reduce the level of the video input signal by 8 dB.

Adjust the value of R37 so that, when the input level is changed in this manner, the trailing edge of the pulse does not change position by more than 30 ns.

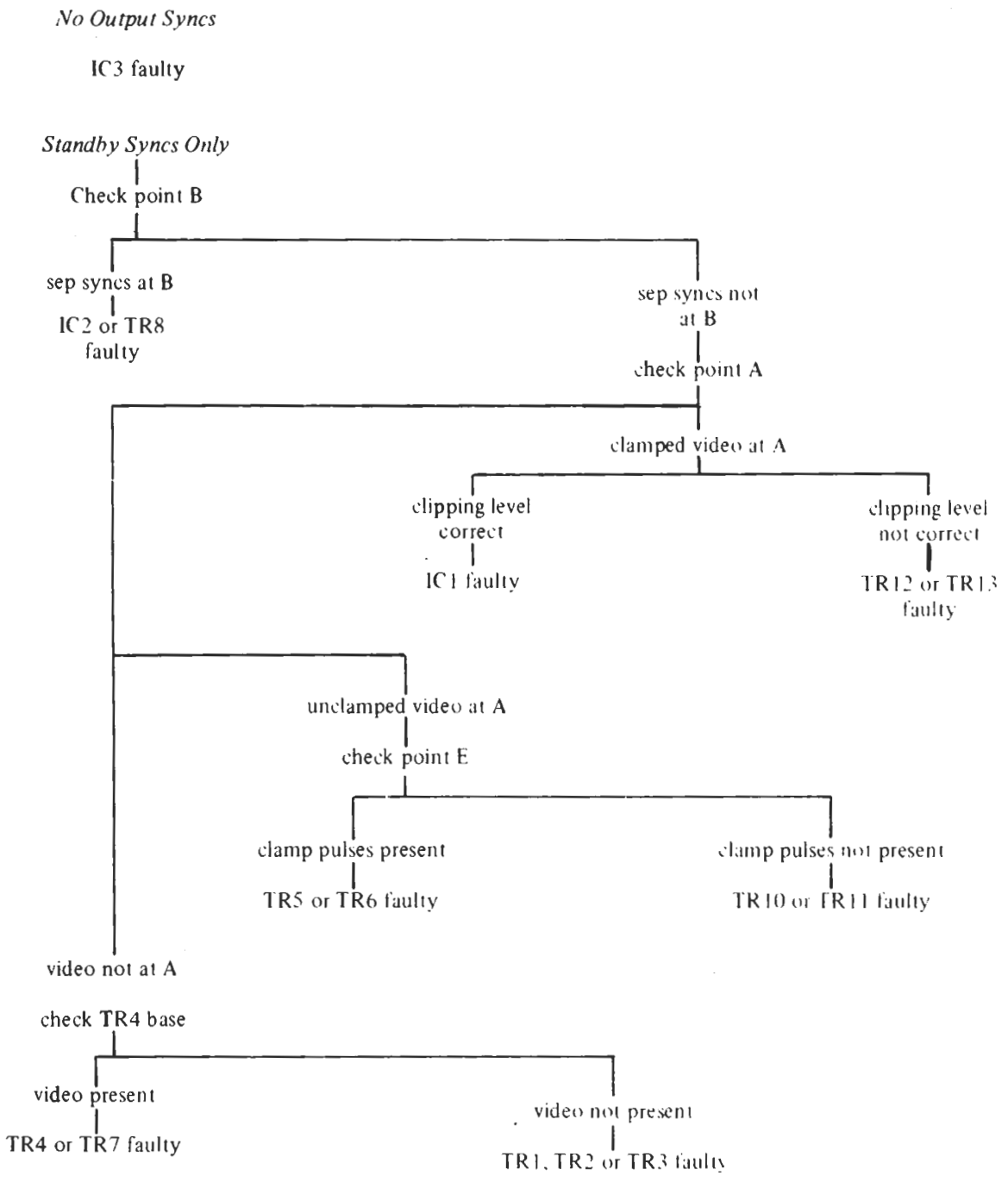
Fault Diagnosis

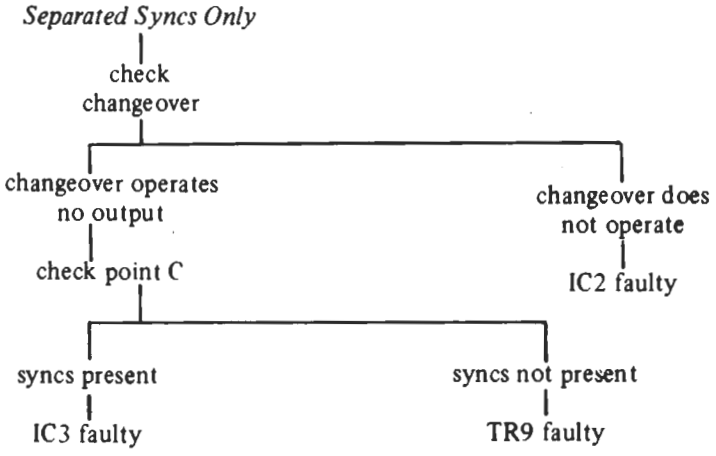
A flow chart is given below to assist in fault

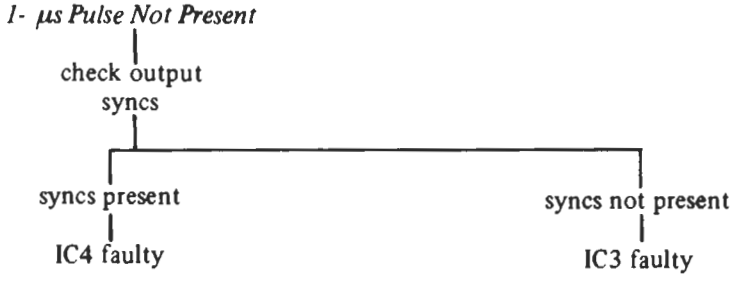
location. The chart assumes that all input feeds and supplies have been checked and are correct. Where the comment 'TRxx faulty' is made, this implies that the fault lies either with the transistor itself or with an associated component.

References to Typical Associated Equipment

1. Sound-in-syncs Coder CD2/505
2. Sound-in-syncs Timing Oscillator Logic Unit UN23/521




Separated Syncs Only
check changeover
changeover operates no output
changeover does not operate
check point C
IC2 faulty
syncs present
syncs not present
IC3 faulty
TR9 faulty


1- μs Pulse Not Present
check output syncs
syncs present
syncs not present
IC4 faulty
IC3 faulty

TES 9/71