S.I.S. SYNC SEPARATOR UNIT UN16/515

Introduction

The UN16/515 forms part of a sound-in-syncs decoder [1]; it accepts either a standard video signal or a video signal containing sound-in-syncs information and provides the following outputs:

positive going line-sync pulses
positive-going line frequency 1-μs pulses which have leading edges coincident with the leading edges of syncs
a sync-fail indication.

Sync pulses are separated from the input signal by means of a circuit which slices the syncs at their mid-amplitude point. The slicing levels are proportional to the amplitude of the sync-pulse component of the input signal and so slicing is carried out at the correct point for a wide range of input-signal amplitudes.

The unit is constructed on a printed-wiring board fitted with a 25-way ISEP connector and with index-peg positions 3, 9 and 13. Power supplies at +12V, +5V and −5V are required.

General Specification

Input Signal (Sound-in-syncs or normal video)	1V p-p nominal (signal range +6dB to −8dB)
Input Impedance	10 kilohms
Maximum d.c. at Input	+4V, −6V
Output Signals	
Positive-going Line Syncs	+3·5V p-p (alternate equalising pulses are widened to sync width)
1-μs Pulses	positive-going at line-rate, leading edge coincident with leading edge of syncs
Sync-fail Indication	normally +3·5V, falling to 0V if syncs fail
Delay (Input to Sync Pulse Output)	150 ns
Output Recovery Time	less than 4 ms for a signal interruption of any duration
Failure Alarm Time-constant	68 μs nominal
Typical Signal Degradation Before Failure	
Peak Signal/r.m.s. Noise (unweighted white noise)	22 dB
50-Hz Hum	300 mV
Added Square Wave (50 Hz)	100 mV
Operating Temperature Range	0° C to +45° C
Power Consumption	50 mA at +12V, 40 mA at −5V, 35 mA at +5V

Continued overleaf

Circuit Description

A circuit diagram of the UN16/515 is given in Fig. 1 and waveforms at various points in the circuit are shown in Fig. 2.

Input Amplifier

The input amplifier is formed by transistors TR1 to TR3. Transistors TR1 and TR2 form a long-tailed pair and TR3 is an emitter-follower. Negative-feedback is taken from TR3 emitter to TR2 base and the gain of the amplifier (about 10 dB) is determined by the ratio of R7 to R8. Frequency response is controlled by C2 and by the tuned circuit L3, C3, R9. These components provide a progressive roll-off starting at 2·2 MHz, with a notch at 4·4 MHz. The amplifier is biased so that a certain amount of white-level clipping is introduced.

Clamp

The output of TR3 is passed via emitter-follower TR4 to the base of TR7. At this point the signal is clamped by the action of transistors TR5 and TR6 which form a bi-directional switch that operates during the back-porch period. Depending on the polarity of the signal with respect to zero volts, the applied positive-going clamp pulses cause either TR5 or TR6 to conduct and the back porch of the video signal is clamped to zero volts.

Clamp Pulse Generator

Transistor TR10 is fed with composite video from TR4 and functions as a sync separator. The sync pulses developed at the collector of TR10 contain sound pulses; these are removed by the action of TR11 which is driven into conduction during the sound-pulse period by a signal obtained from the digit-blanking generator. The blanked sync pulses appearing at the collector of TR11 are differentiated and the negative-going edges are then used to drive TR12 into cut-off. Thus the required positive-going clamp pulses are developed at TR12 collector.

Sync Slicer

The clamped video present at TR7 emitter (see Fig. 2b) contains sound pulses in the sync-period; these sound pulses are removed by the action of TR8 before slicing takes place. During line-sync periods TR8 is driven into conduction by a positive-going pulse obtained from the digit-blanking generator and the sound pulses are gated out (see Fig. 2c). Because TR8 continues to operate during the field-blanking period, alternate equalising pulses are increased in duration to 4 μs.

Integrated circuit IC1 is a differential comparator which functions as a sync slicer. The device compares the sync-pulse amplitude of the clamped video signal with a d.c. reference signal which has half the amplitude of syncs and is derived from the sync-level detector. When the input syncs go more negative than the reference level, the output of IC1 goes positive and thus positive-going sync pulses with a peak-to-peak amplitude of 3·5 volts are developed; these pulses are fed via emitter-follower TR9 to the Separated Syncs output of the unit (see Fig. 2d).

Sync Level Detector

Transistor TR15 conducts during sync-pulse periods and charges capacitor C20 to a potential which is proportional to the peak sync-pulse amplitude. Smoothing is carried out by R48 and C21 and the offset potential caused by TR15 is removed by TR16. The signal is then fed, via a potential divider network which reduces it to half sync amplitude, to the sync slicer IC1.

Digit Blanking Generator

Separated sync pulses, derived from the output of IC1, are fed via a differentiating circuit to integrated circuit IC3a which functions as a monostable multivibrator. The timed state is initiated by the leading edge of the applied differentiated pulse; it lasts for more than half a television line and so prevents the generation of unnecessary blanking pulses at twice line frequency during the field-sync period. The output of IC3a is differentiated and its leading edge (i.e. the edge coincident with line syncs) used to trigger IC3b, another monostable circuit which generates line-frequency pulses with a duration of 4·6 μs The pulse outputs of IC3b are amplified and inverted by transistors TR13 and TR14; TR13 feeds positive-going pulses to TR8 and TR14 feeds negative-going pulses to TR11. Both feeds have an amplitude of 5V peak-to-peak.

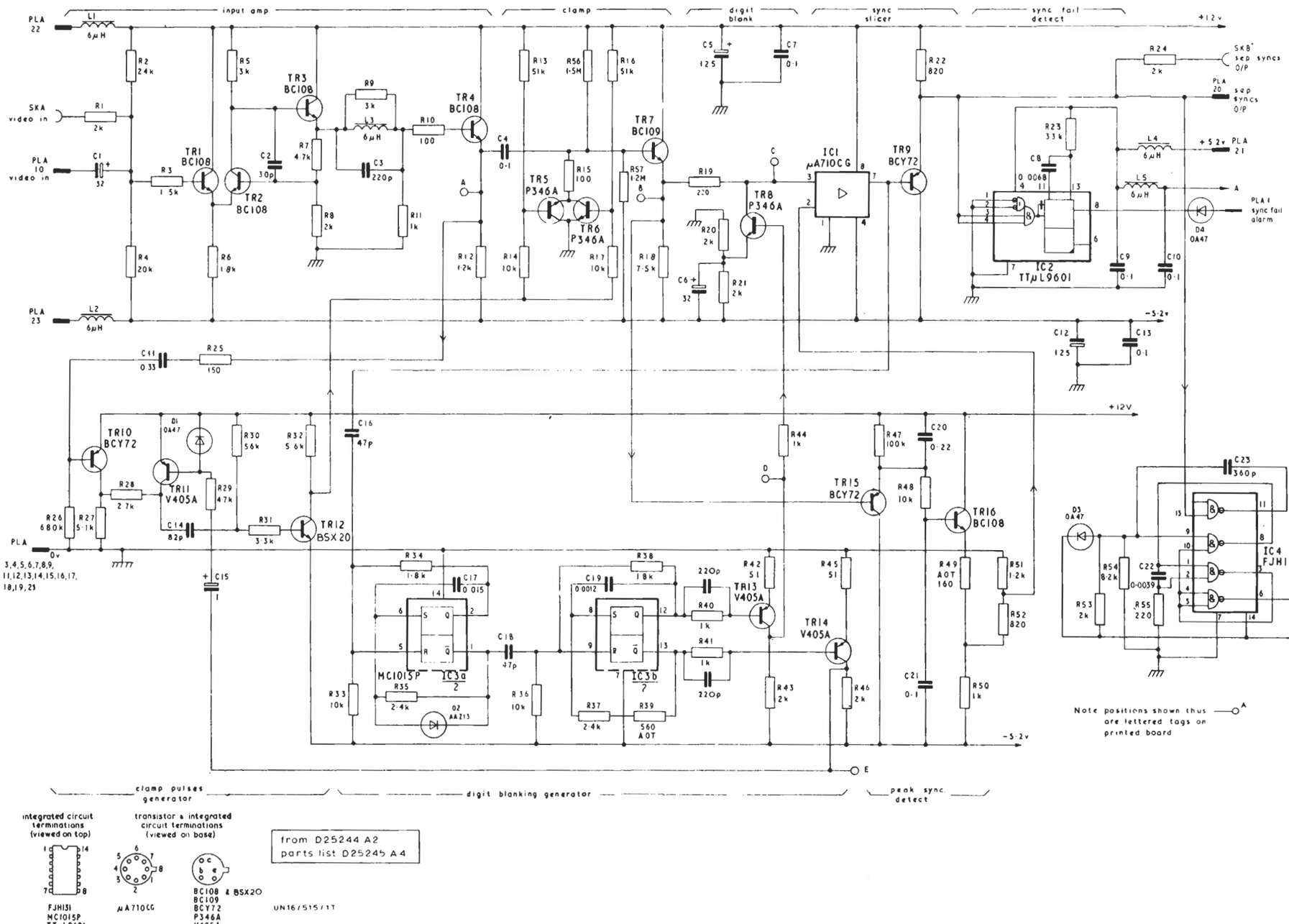
Sync-fail Detector

Integrated circuit IC2 functions as a re-triggerable monostable multivibrator; unlike a conventional monostable the timed state is commenced afresh by each input pulse so that, if the time interval between inputs is shorter than the time-constant of the circuit, the monostable remains in the timed state. In this instance the time constant is 68 μs so that a change of state takes place only if a break of more than one line occurs in the video input to the unit.

1-μs Pulses

IC4 is a monostable circuit which consists of four NAND gates; it is triggered from the leading edge of the output sync pulses and provides 1-μs pulses for use in an associated unit [2]. The operation of the circuit is given below.

Positive-going sync pulses are inverted in gate 11, 13 and are then fed via a differentiator to gate 9, 10, 8. The inputs to this gate are normally high (logic 1) and the output normally low (logic 0) but the negative-going edge of the differentiated pulse changes the state of the gate and causes a logic 1 to appear at 8. This is applied directly to input 1 of gate 1, 2, 3 and (via C22) to input 2; therefore the output of gate 1, 2, 3 becomes logic 0 and remains for a period (1 μs) which is determined by the time constant of C22 and R55. The output at 3 is inverted by gate 4, 5, 6 to provide a positive-going 1-μs pulse output.



integrated circuit terminations (viewed on top)

FJH131
MC1015P
TTµL9601

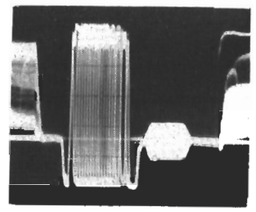
transistor & integrated circuit terminations (viewed on base)

µA710CG

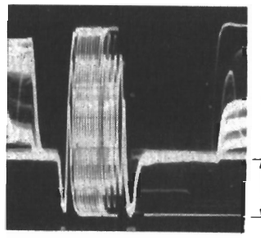
BC108 & BSX20
BC109
BCY72
P346A
V405A

UN16/515/1T

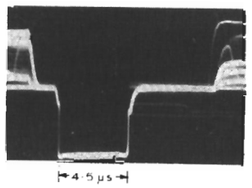
from D25244 A2
parts list D25245 A4



(a) Video input signal



(b) Test point B



(c) Test point C

(d) Separated sync output

UN16/515/2P

Fig. 2 Waveforms in the UN16/515

Fig.1. Circuit of the S-i-S Sync-separator UN16/515

Maintenance

Preset adjustments are provided for the slicing level and for the digit blanking duration. Readjustment may be required if circuit components are changed.

Slicing Level Adjustment

Monitor the *Separated Sync* output with an oscilloscope probe.
Switch the oscilloscope timebase to *Internal* and adjust the timebase so that the pulse occupies the full width of the display.
Operate the Y-timebase magnifier and observe the back edge of the pulse.
Reduce the level of the video input signal by 8 dB.
Adjust the value of R49 so that, when the input level is changed in this manner, the back edge of the pulse does not change position by more than 30 ns.

Digit Blanking Width

Monitor test-tag C with an oscilloscope probe and check that the waveform is as shown in Fig. 2(c). If the waveform is incorrect adjust the value of R39 to obtain a pulse duration of 4·6 μs

Fault Diagnosis

The adjacent flow charts are given to assist in fault location. The charts assume that all input feeds and supplies have been checked and are correct. Where the comment "TRxx faulty" is made this implies that the fault lies either with the transistor itself or with an associated component.

References to Typical Associated Equipment

1. Sound-in-syncs Decoder CD3M/504
2. Sound-in-syncs Timing Oscillator Logic Unit UN23/521

TES 6/71

No Output Syncs

- check point C
  - no clamped video at C
    - check point B
      - video absent
        - check point A
          - video absent
            - TR1, TR2, TR3 or TR4 faulty
          - video present
            - TR7 faulty
      - unclamped video at B
        - check TR12 collector
          - clamp pulses absent or irregular
            - check TR11 collector
              - syncs present
                - TR12 faulty
              - unblanked syncs present
                - TR11 or TR14 faulty
              - syncs absent
                - TR10 faulty
          - clamp pulses present
            - TR5 or TR6 faulty
      - clamped video at B
        - TR8 or TR13 faulty
  - clamped video at C
    - slicing level correct
      - IC1 or TR9 faulty
    - slicing level incorrect
      - TR15 or TR16 faulty

Output Syncs Irregular

- check point C
  - video unclamped
    - continue as for no output syncs
  - video clamped
    - TR15 or TR16 faulty

Output Syncs Unblanked

- check point D
  - blanking pulses absent
    - check TR13 base
      - blanking pulses absent
        - IC3 faulty
      - blanking pulses present
        - TR13 faulty
  - blanking pulses present
    - TR8 faulty

1–μs Pulses Absent

- check output syncs
  - syncs absent
    - continue as for no output syncs
  - syncs present
    - IC4 faulty