SOUND-IN-SYNCS SOUND PULSE SEPARATOR

Introduction

The UN16/517 forms part of a sound-in-syncs decoder[1] and accepts a composite sound-in-syncs signal. The unit has three functions, these are outlined below:

(a) It separates the sound pulses from the composite input signal by blanking out the video component. The sound pulse groups are then clipped at the half amplitude point; a measuring circuit ensures that the correct clipping level is maintained for a range of input levels.

(b) It provides a delayed output of the sound-in-syncs input signal for use in an associated stabilising amplifier[2].

(c) It contains an error-detection circuit which provides a sync-fault output if two or more *hold* signals are counted during a period of approximately 10 lines.

The UN16/517 is constructed on a printed-wiring card which is fitted with a 25-way ISEP connector. Index-pin positions are 3, 5 and 17. Power supplies at +12V, −12V and +5V are required.

General Specification

Input Signals

Sound-in-syncs	nominally 1V p-p, input impedance 75 ohms.
Line Drive	positive-going pulses (TTL logic) obtained from the UN23/522.
Sync Gate	negative-going line-repetitive pulses (TTL logic) obtained from the UN23/523.
Hold	TTL logic level 0, unless a sync fault is present, obtained from UN20/527.

Output Signals

Sound Pulses	negative-going line-repetitive pulse groups (TTL logic) for use in the UN23/524.
Delayed Sound-in-syncs	1V p-p nominal into 75 ohms, delay adjustable in 5-ns steps between 465 ns and 620 ns, for use in AM18/521.
Sync Fault	normally logic level 1, changing to logic level 0 for fault condition (TTL logic).
TTL Logic Levels	logic level 1, about +3·5V (+5V max.)
	logic level 0, about 0V (+0·4V max.).
Power Requirements	40 mA at +12V, 40 mA at −12V, 30 mA at +5V.

Circuit Description

A block diagram of the UN16/517 is given in Fig.1 and a circuit diagram in Fig.2.

Delayed Sound-in-Syncs

The sound-in-syncs input signal is applied to four cascaded delay networks to obtain a delayed feed for use in an associated sync stabilising amplifier. The delay obtained can be adjusted, by means of tapping points on DL4, in 5-ns steps between 465 ns and 620 ns.

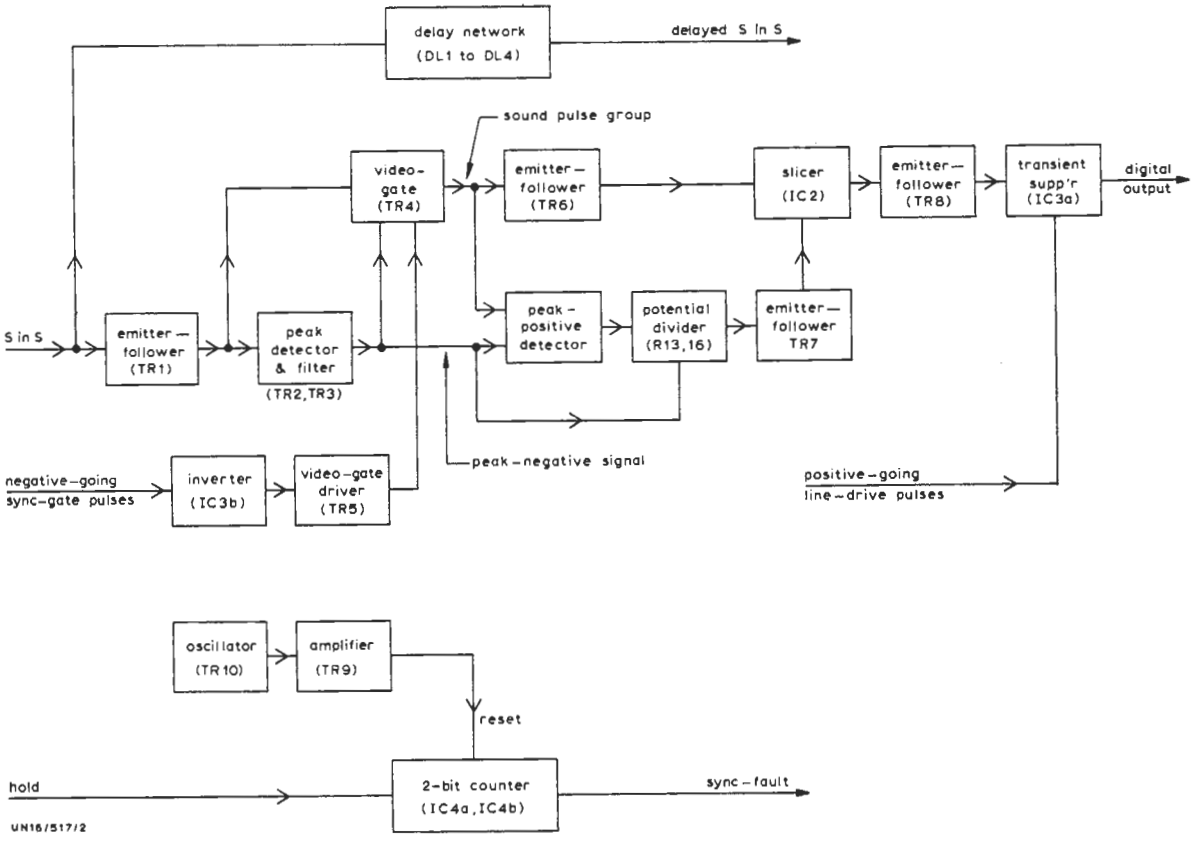

Fig.1 Simplified Block Diagram of the UN16/517

Sound Pulse Separator

The sound-in-syncs input signal is applied via emitter-follower TR1 to TR2 which functions as a peak detector and charges capacitor C5 to a value representative of the negative extremity of the incoming signal; i.e. the bottom of the sound pulses. The offset potential due to TR2 is removed by TR3 and the peak-detected signal is smoothed by capacitor C6 to provide a measure of the peak negative amplitude of the sound-in-syncs signal. This measured potential is applied to TR4 and IC1 as a reference potential.

In addition to feeding TR2, the signal developed at the emitter of TR1 is applied, via R4, to TR6 and IC1. The signal path is shunted by the field-effect transistor TR4 which conducts for the active part of each line period and so gates out the video information. However, during the sync-pulse period TR4 is cut off by the application of sync-gate pulses, and the sound-in-syncs information contained in the sync pulses is applied to TR6 and IC1. The sync-gate pulse starts 1-μs before the leading edge of separated syncs and has a duration of 6·2-μs.

Integrated circuit IC1 functions as a fast-acting voltage comparator; it accepts both the sound-in-syncs information and the peak-negative signal. When the amplitude of the sound pulses applied to pin 2 is greater than that of the peak-negative signal applied to pin 3, the comparator output is at logic level 1, and capacitor C7 charges via diode D2 until the potential at pin 3 is the same as the peak-positive amplitude of the sound pulses. The equal-value resistors R13 and R16 form a potential divider between the peak-positive output of IC1 and the peak-negative signal and so a potential which corresponds to half the peak amplitude of the sound pulses is fed from the junction of R13 and R16 to TR7.

Integrated circuit IC2 functions as a clipping stage; it accepts sound pulses from TR6 and a potential corresponding to half the pulse amplitude from TR7. The output of IC2 consists of sound pulses clipped at the half-amplitude point. These are fed, via emitter-follower TR8, to *Nand* gate IC3a where they are gated with positive-going line-drive pulses to remove transients and to produce a negative-going output at PLA 18.

Hold Error Detector

Bistable stages IC4a and IC4b are connected as a two-bit counter. Every ten lines the Q output of the counter is reset to logic 0 by a pulse which is generated by unijunction transistor TR10 and amplified to the required level by TR9. During the period between reset pulses the *Hold* input remains at logic level 0 unless a fault occurs. A fault changes the *hold* input to logic level 1; this change has no immediate effect on the counter but when the hold input returns to logic 0 the Q output of the first stage of the counter goes to logic 1; i.e. the counter is triggered on negative-going edges. If a second fault occurs before another reset pulse is generated, the second stage of the counter changes state also and a

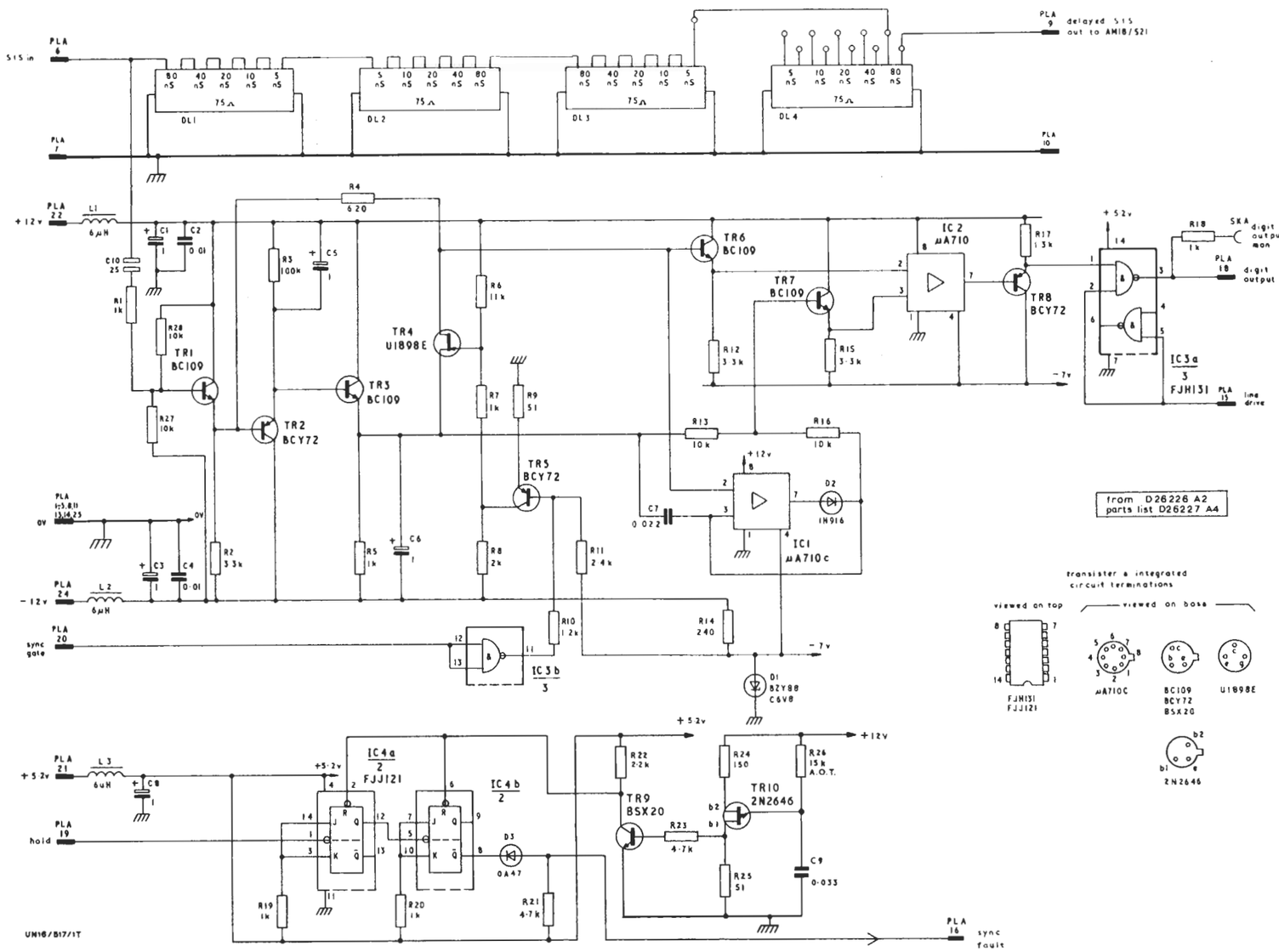

Fig.2 Circuit of the S.i.s. Sound-pulse Separator UN16/517

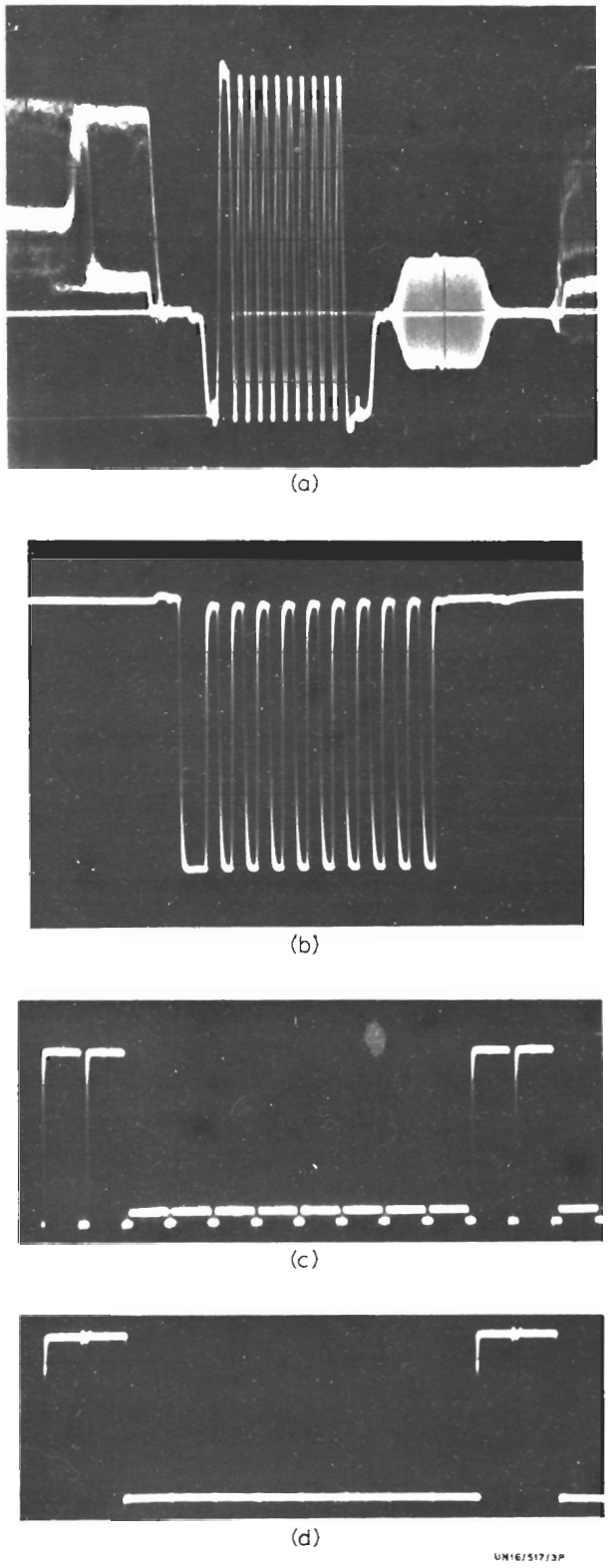

Fig.3 Waveforms in the UN16/517
(a) s.i.s. full-count waveform
(b) digit-output mon SKA
(c) hold-counter input
(d) hold-counter output

logic 0 is developed at its $\overline{Q}$ output to provide a sync-fault output at PLA 16.

Maintenance

To check the sound-pulse separator section of the unit:

1. Apply a full-count sound-in-syncs signal to the input of the parent decoder. (This waveform is shown in Fig.3a and can be produced by removing the UN23/528 unit from the associated coder[3].)
2. Check that a negative-going full-count sound pulse group, as shown in Fig.3b, is present at the output monitor socket SK A. If the output waveform is absent, check that a sound pulse group is present at IC2 pin 2 and a half-amplitude potential (see Circuit Description) at IC2 pin 3. The absence of either of these waveforms will indicate the location of the fault.

To check the error detector section of the unit:

1. Remove the sound-in-syncs signal from the decoder input and replace it with a composite video signal. This will result in a line-rate hold signal being applied to the UN16/517.
2. Check that the input to the hold counter (IC4 pin 1) consists of two negative-going edges which recur about every 10 lines, as shown in Fig.3c.
3. Check that the counter output (IC4 pin 8) is a positive-going pulse with a duration of 128-μs, as shown in Fig.3d.

References to Typical Associated Equipment

1. Sound-in-Syncs Decoder CD3M/504.
2. Sync Stabilising Amplifier AM18/521.
3. Sound-in-syncs Coder CD2M/505.

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