SYNC PULSE SEPARATOR UN16/518A

Introduction

The UN16/518A accepts a feed of 625-line composite video signal and provides the following outputs:

(a) mixed sync pulses in which the sync and equalising pulses are selected to be either 4·7 or 7·8 μs in length,

(b) clamp pulses, 2 μs long, each timed to occur within the back porch period.

The unit is designed to operate in the presence of sound-in-syncs information. It is built on a printed wiring card which can be incorporated on a chassis with other equipment.

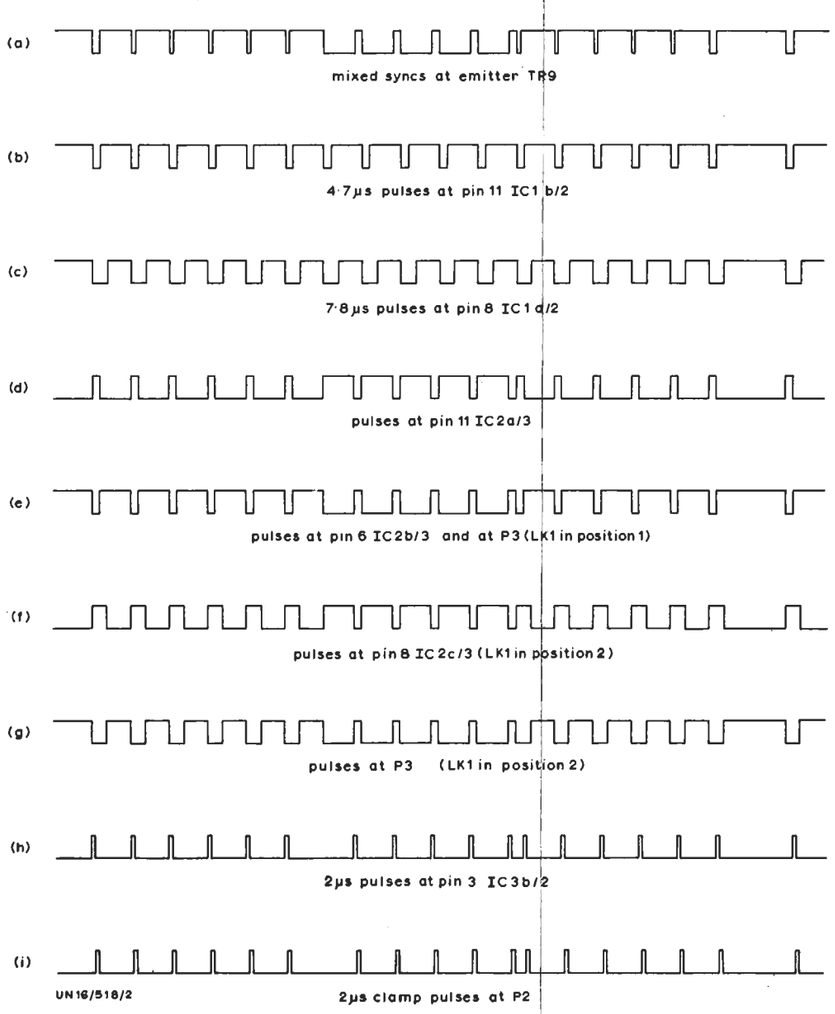

Fig. 2. Typical Waveforms

General Specification

Input	625-line colour or monochrome composite video signal.
Input Level (with respect to 1 volt across 75 ohms)	
With sound-in-syncs information	Between −6 and +3 dB.
Without sound-in-syncs information	Between −10 and +4 dB.
Input Impedance	10 kilohms.
Outputs	(a) Mixed sync pulses, 2 ±0·25 volts in amplitude. Duration of sync and equalising pulses either 4·7 or 7·8 µs. (b) 2-µs clamp pulses, amplitude about 12 volts, timed to occur during back porch period.
Output Impedance	75 ohms.
Return Loss	Greater than 40 dB from zero to 5·5 MHz.
Differential Gain and Phase Distortion	No measureable degradation when the unit is bridged across a video signal.
Edge Delay	The leading edge of the output sync pulses has a maximum delay of 0·5 µs.
Logic Potentials	
Logic 0: input	1·1 volts max.
output	0·4 volt max.
Logic 1: input	2 volts min.
output	2·6 volts min.
Operating Temperature Range	20 to 45 degrees C.
Power Requirements	12 volts 105 mA d.c. 6 volts 60 mA d.c.

Circuit Description (Figs. 1 and 2)

Fig. 1 is a circuit of the UN16/518A and Fig. 2 illustrates certain idealised waveforms. Letters in parentheses in the text refer to the waveforms in Fig. 2.

A composite video input signal is applied to terminal P1 and taken via f.e.t. TR1, which together with transistor TR2, forms a high-impedance input stage. The signal is passed through a low-pass filter to remove any chrominance information. The base of transistor TR6 is clamped to a positive potential of 7·5 volts. Transistor TR8 is a sync separator stage. The mixed sync waveform (a) appears at the emitter of transistor TR9.

Monostable circuits IC1a/2 and IC1b/2 are each made up of two NAND-gates using external timing components. The mixed sync waveform (a) is differentiated and the negative-going pulses are used to trigger the two monostable circuits.

The output of circuit IC1b/2 is a pulse 4·7 µs long (b) and that from IC1a/2 a pulse 7·8 µs long (c). The effect of the monostable action is to make the line-sync and equalising pulses all either 4·7 or 7·8 µs in length.

The output of monostable circuit IC1b/2 (b) together with mixed sync waveform (a) is applied to NAND-gate IC2a/3. The purpose of the gate is to remove any sound-in-syncs information and its output is shown in waveform (d).

Waveform (d) is inverted to give waveform (e) and, together with waveform (c), is applied to NAND-gate IC2c/3. The output of this gate depends upon the position of link LK1. If the link is in position 1, the output is shown at (d); if the link is in position 2 the output is shown in (f) where the sync and equalising pulses are all lengthened to 7·8 microseconds.

The output of gate IC2c/3 is amplified and presented at terminal P3. See waveforms (e) and (g).

The output of gate IC2a/3 (d) is applied to emitter-follower TR13. The output is differentiated and the negative edges are used to trigger a monostable circuit IC3b/2. The output (h) is a train of two-microsecond positive-going pulses. These pulses are differentiated and used to trigger a second monostable circuit IC3a/2. The output of circuit IC3a/2 is a train of two-microsecond clamp pulses (i) which are timed to occur during the back porch period. The clamp pulses are amplified by transistors TR11 and TR12 and passed through emitter-follower TR10 to the base of transistor TR5 and to terminal P2.

Setting-up Procedure

The only adjustments possible are the selection of resistors R24, R25 and R53. This entails the use of a Sound-in-Syncs Coder CD2M/505 and full details are given in Designs Department Specification 11.91(70).

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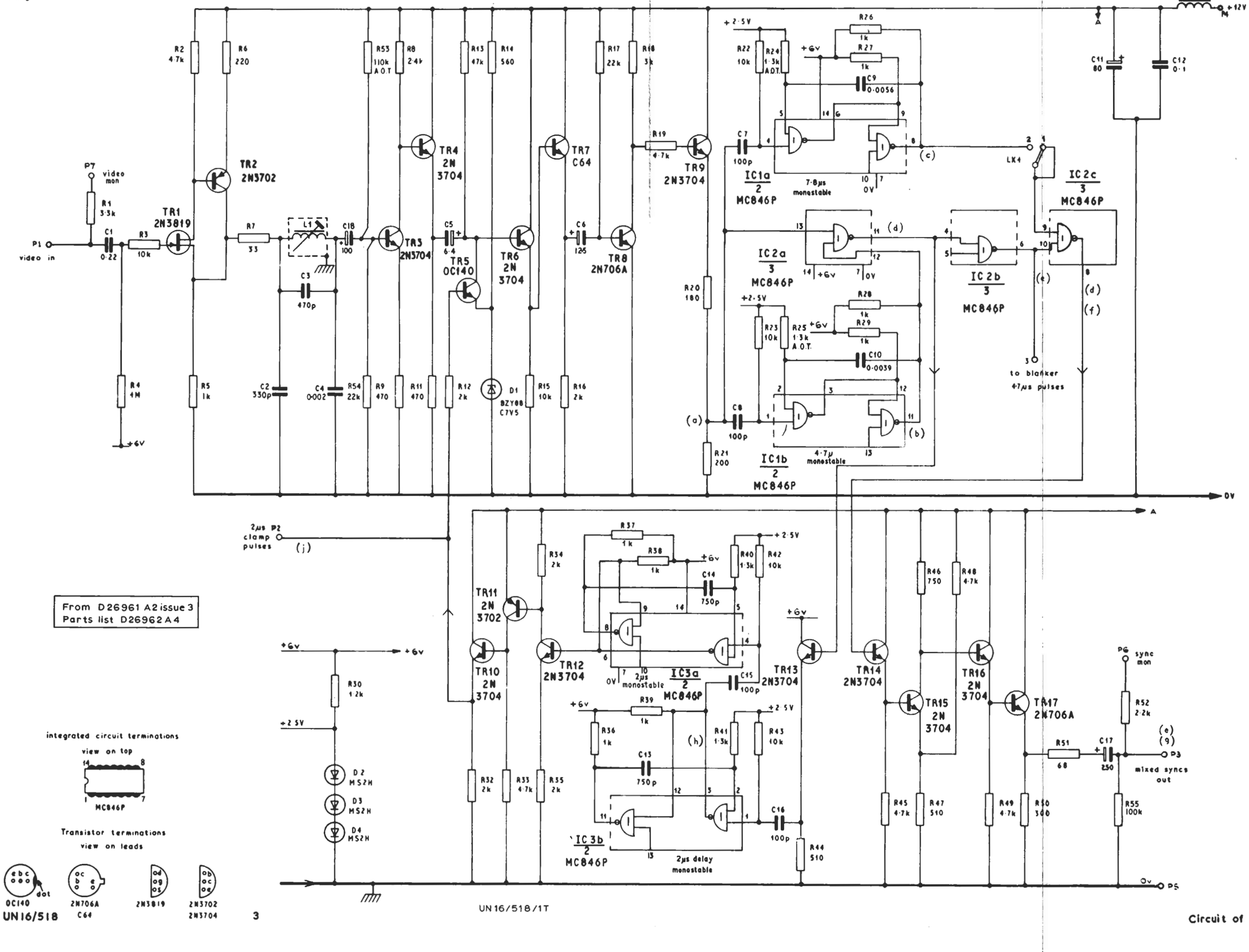

From D26961 A2 issue 3
Parts list D26962 A4

integrated circuit terminations
view on top

Transistor terminations
view on leads

UN16/518

UN16/518/1T

Fig. 1.
Circuit of UN16/518A