VARIABLE DIVIDER UN17/501

Introduction

The Variable Divider UN17/501 is used in a drive unit[1,2] to convert input error control signals into a required change of phase or frequency in an output signal. The circuit comprises an eleven-stage counter with a counter-control circuit to modify its normal division ratio of 1782.

The UN17/501 is constructed on a CH1/26A chassis with index peg positions 12 and 26.

Circuit Description

The circuit of the UN17/501 is given in Fig.1.

Counter

A 4·4296875 MHz Natlock reference frequency square-wave signal is fed to the eleven-stage counter (Bistable Units Nos. 1-4 and 6-12) via pin 2. The feedback pulses are not taken directly from the output of the counter but via Bistable Unit No. 5. The output of the counter causes output 1 of Bistable Unit No. 5 to go negative and 16 counter-input pulses later it is switched back to a positive state. This positive-going transistion is differentiated and used as a feedback pulse. This arrangement is necessary because the delay through the counter is of the order of the input-pulse period.

The feedback inputs of the first four counter-stages are d.c. coupled to the outputs of the counter control circuit. If one of these outputs is negative, the feedback-input diode D3 of the counter stage is biased off thus inhibiting the normal action of the feedback pulse.

Counter Control Circuit

The behaviour of the counter control circuit is summarised in the table below:

Bistable Units Nos. 13 to 15 are used to slow correction rates to change the counter ratio once in every picture period. Bistable Unit No. 13 converts the random timing of a picture-pulse input on pin 12 into a positive-going transition at the start of the next count. This transition enables Bistable Unit No. 14 to gate one feedback pulse per picture period to Bistable Unit No. 1 except under *Normal* conditions. It also enables Bistable Unit No. 15 to inhibit one feedback pulse per picture period to Bistable Unit No. 2 under *Retard* or *Fast Retard* conditions. This is shown in the waveforms given in Fig. 2.

When the F' signal alone is applied, the *Fast Advance* condition results.

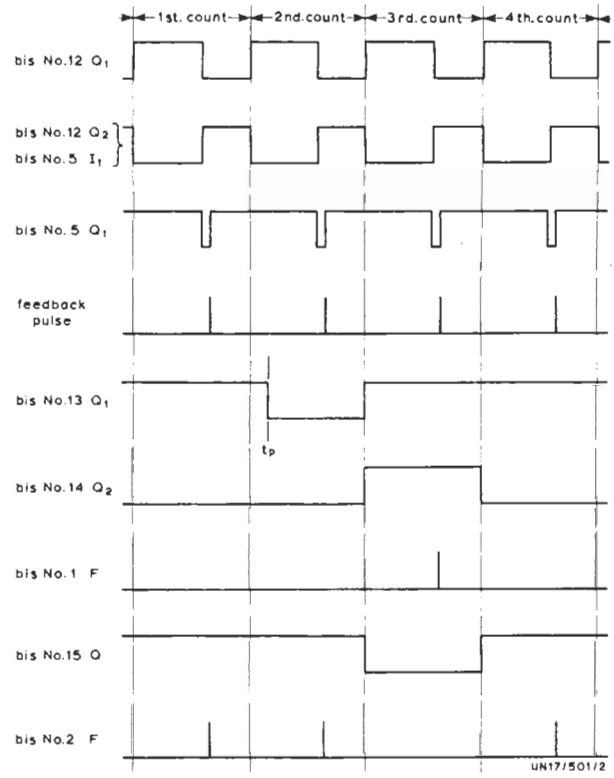


Fig. 2. Waveforms in the UN17/501 Illustrating how One Feedback Pulse per picture is Selected or Inhibited (Picture-pulse input at time t_p in the second count shown)

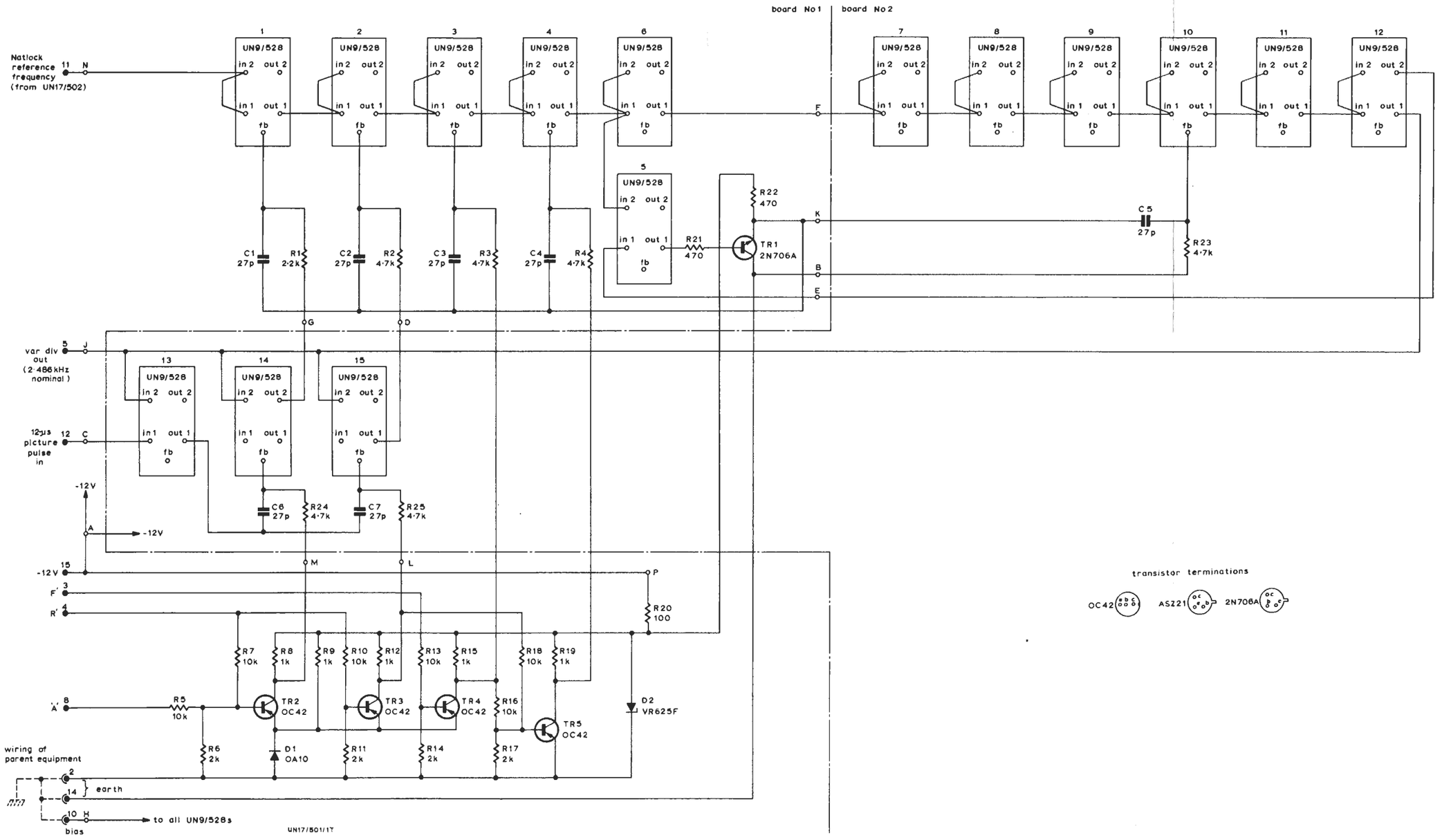
Test Procedure

The UN17/501 is tested as part of its parent equipment[1,2]

References to Typical Associated Equipment

1. Waveform Generator Drive Unit GE1/520
2. Waveform Generator Drive Unit GE1L/537

MJR 9/66
Revised RDH 11/71



transistor terminations

Fig. 1. Circuit of the UN17/501