SYNC PROCESS UNIT UN17/505

Introduction

The UN17/505 accepts two mixed sync pulse inputs and produces the following outputs:

Derived from first input

(a) Line-frequency pulses
(b) Inverted line-frequency pulses
(c) A negative voltage if there is an input signal (*No Sync*)
(d) Field-frequency pulses
(e) Picture-frequency pulses
(f) Line sample pulses (also at picture-frequency)

Derived from second input

(g) Line-frequency pulses
(h) A negative voltage if there is an input signal (*No Sync*)
(j) Picture-frequency pulses

The UN17/505 is constructed on a CH1/26A chassis with index-peg positions 12 and 19.

General Description

A block diagram for half the UN17/505 is given in Fig. 1. Mixed sync pulses are fed to a field sync separator and a 45-μs monostable multivibrator. This duration ensures that the multivibrator is not double-triggered during the line sync interval. Both normal (positive-going) (*X*) and inverted (*W*) line-frequency pulses are produced. Normal line-frequency pulses are fed to an inverting pulse-stretching circuit which merges the pulses to give a negative output (*Y*) when there are input pulses.

The output of the field sync separator triggers a 4-ms monostable multivibrator at the start of the second broad pulse to give field-frequency output pulses (*Q*). Field and line pulses are shortened and gated to give picture-frequency pulses which trigger a 12-μs monostable multivibrator. The output (*U*) of this multivibrator and inverted field pulses are fed to a bistable multivibrator to produce a 4-ms picture-frequency pulse output (*R*).

Fig. 2 gives some of the waveforms found in the UN17/505.

Fig. 3 shows the connections to both halves of the UN17/505.

Circuit Description

The circuit of the UN17/505, given in Fig. 4, comprises a number of simple basic circuits, but the following points should be noted:

(a) Capacitors C22 and C23 across the collector load of transistor TR1 and the input to the field sync separator circuit respectively slow up the pulse edges and thus provide a degree of immunity against impulsive noise.
(b) Diodes D1 and D4 are biased from the collectors of transistors TR5 and TR9 respectively to

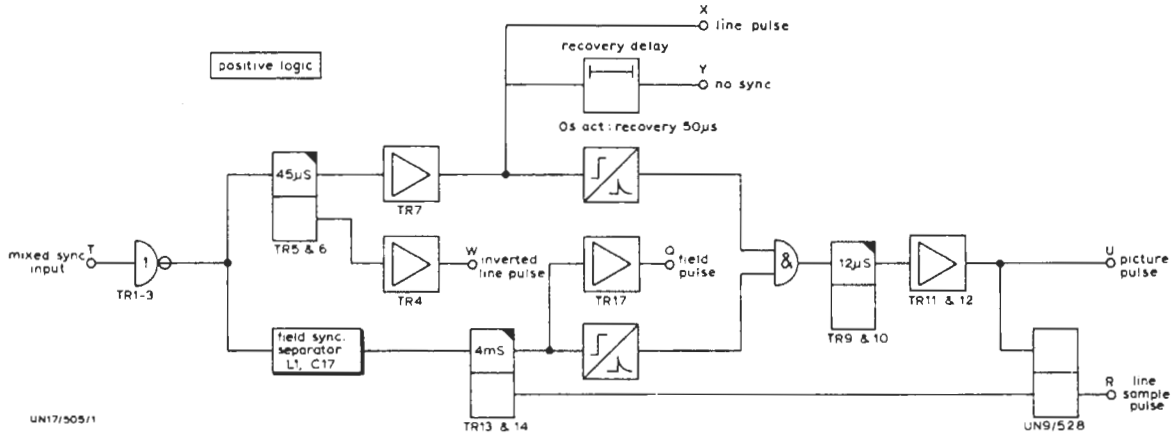

Fig. 1 Block Diagram of the UN17/505

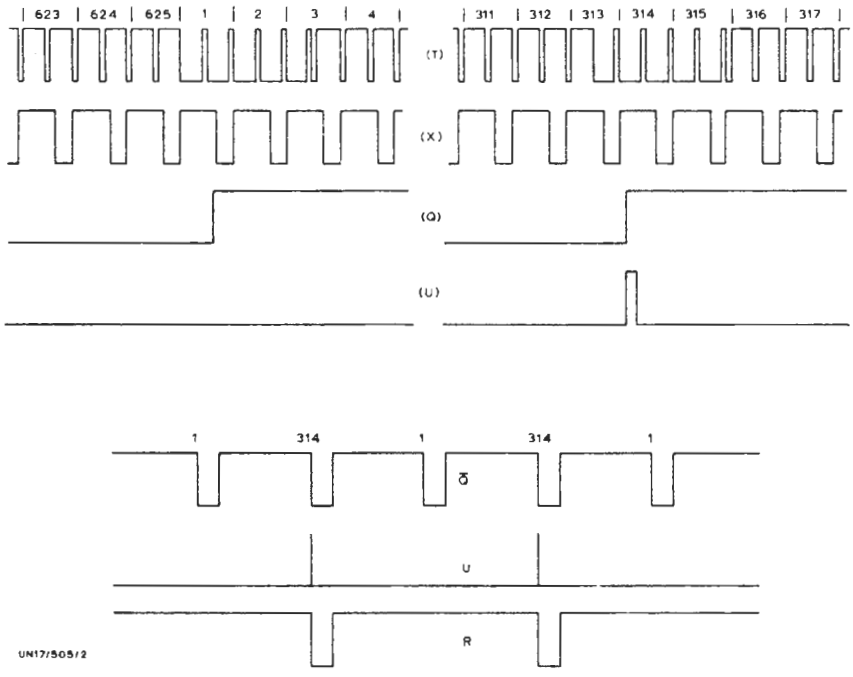

Fig. 2 Waveforms in the UN17/505

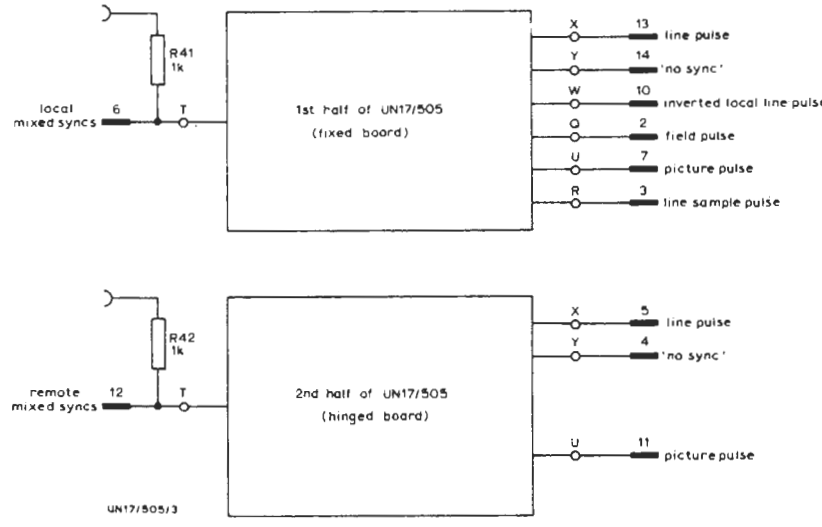

Fig. 3 Connections to the UN17/505

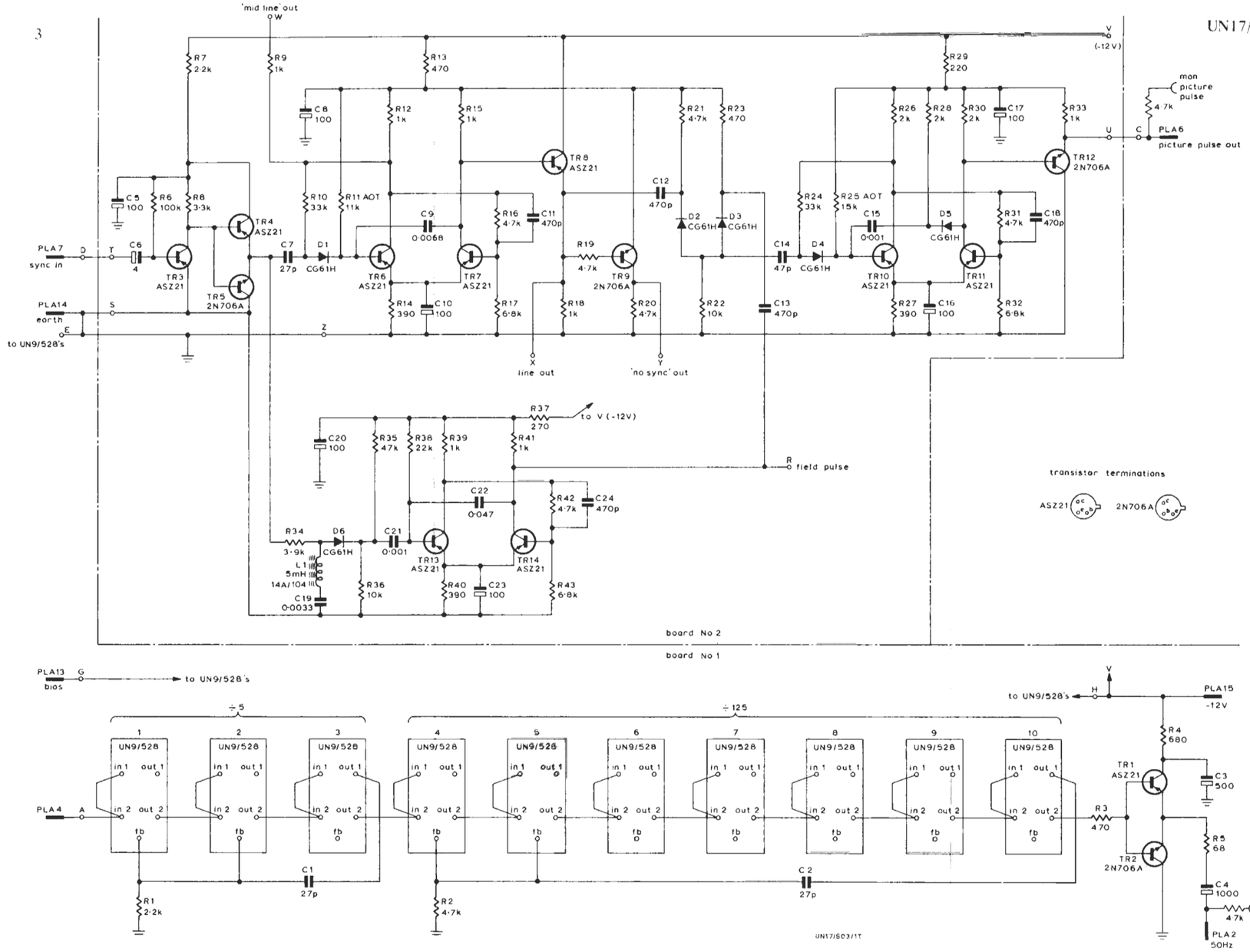

Fig. 1. Circuit of the UN17/503

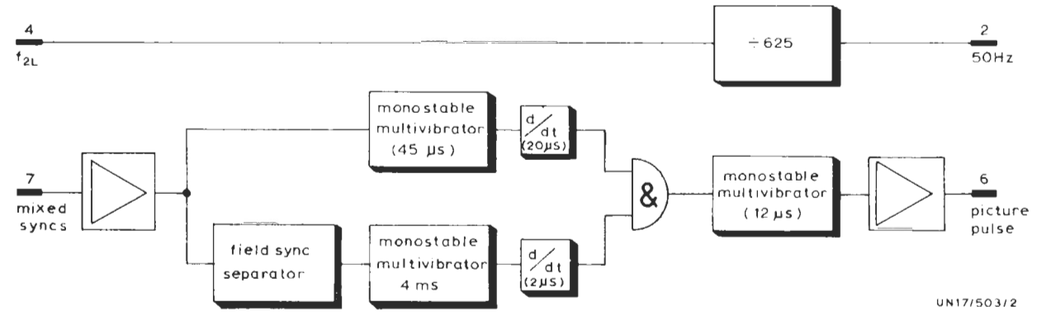

Fig. 2. Block Diagram of the UN17/503

ensure that they are cut off for the whole of the unstable period of their respective monostable multivibrators.

(c) The field sync separator circuit and its waveforms are shown in Fig. 5.

(d) The pulse stretch circuit and its waveforms are shown in Fig. 6.

Test Procedure

The UN17/505 is tested as part of its parent unit[1].

References to Typical Associated Equipment

1. Error Signal Generator (PAL) GE1L/532
   Error Signal Generator (PAL) Four-way GE1M/540
   Error Signal Generator (Genlock) GE1M/568

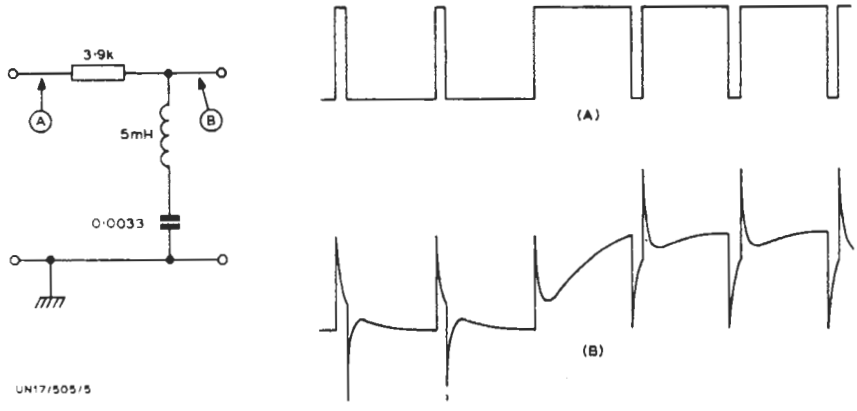

Fig. 5 Circuit and Waveforms for the Field-sync Separator

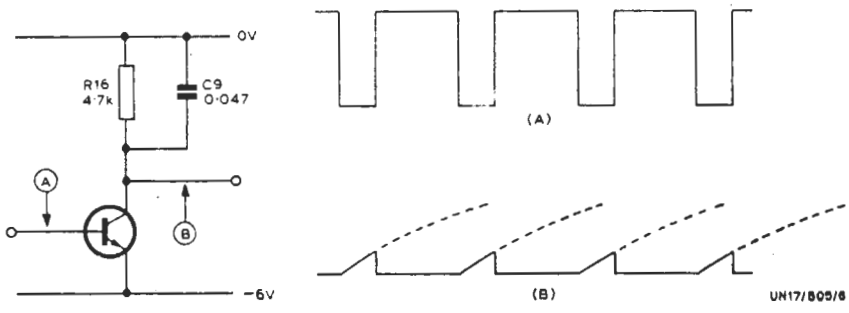

Fig. 6 Circuit and Waveforms for the Pulse-stretch Circuit

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