TONE DECODER AND PULSE COMPARATOR UNIT UN17/518

Introduction

The UN17/518 accepts reference and local 12·5-Hz squarewaves and the Natlock tone error signal from an associated tone coder[1]. The tone is decoded to provide error control-signals for an associated drive unit[2] and digital phase shift equipment[3]. A 25-Hz picture pulse derived from the local 12·5-Hz squarewave is also provided.

When the Natlock tone error-signal is not present a timing comparator derives *Fast* error control signals which describe the timing-error correction required to within 20 μs. The colour error control signal is not generated under these input conditions.

The front panel carries four lamps which have the colours and functions listed:

Routed	(green)	a tone line is connected to the unit;
Tone	(green)	tone is present on the line
Time Error	(amber)	an *Advance* or *Retard* error control signal is present at the unit output;
Colour Error	(amber)	a colour error control signal is present at the unit output.

The UN17/518 requires an external power supply[4] of 12 V at 400 mA d.c., and is constructed on three printed wiring boards accommodated in a CH1/38 (B-size) chassis using a 15-way connector in the central position. Index pegs used are 23 and 32, associated with the left connector position.

General Specification

Signal Inputs (can be reduced by 6 dB)	
12·5-Hz reference squarewave	1V p-p
12·5-Hz local squarewave	1V p-p
Natlock tone error signal	0 dB (w.r.t. 1 mW into 600 ohms)
Input Impedances	
12·5-Hz squarewaves	about 1 kilohm
Natlock tone error signal	600 ohms, balanced
Outputs	
Error control signals (Table 1 gives tolerances)	
a) A', R', F' (binary logic)	0V and −6V (nominal)
b) C' (ternary logic)	0V, −3V and −6V (nominal)
Picture pulses (positive-going)	5V p-p, 8 μs duration at 25-Hz repetition rate
Power Input	−12V d.c., 400 mA
Ambient Temperature Range	0°C to 45°C
Weight	1·45 kg

TABLE 1

Error Control Signal Tolerances

Nominal Voltage	*Actual Voltage Tolerance*	
	binary logic	*ternary logic*
0	more +ve than −1·5	more +ve than −1·5
−3	–	from −2·5 to −3·25
−6	more −ve than −4·5	more −ve than −4·5

Continued overleaf

General Description

A block diagram of the UN17/518 is given in Fig. 1. The unit can operate in one of two modes. When all signal inputs are present an earth-loop via the output transformer of the associated tone coder[1] is detected on the tone line, a *Decoder* mode is selected automatically and the unit provides error control signal outputs which correspond to the tone frequency as listed in Table 2. When the tone line is not connected, the unit operates in a *Comparator* mode.

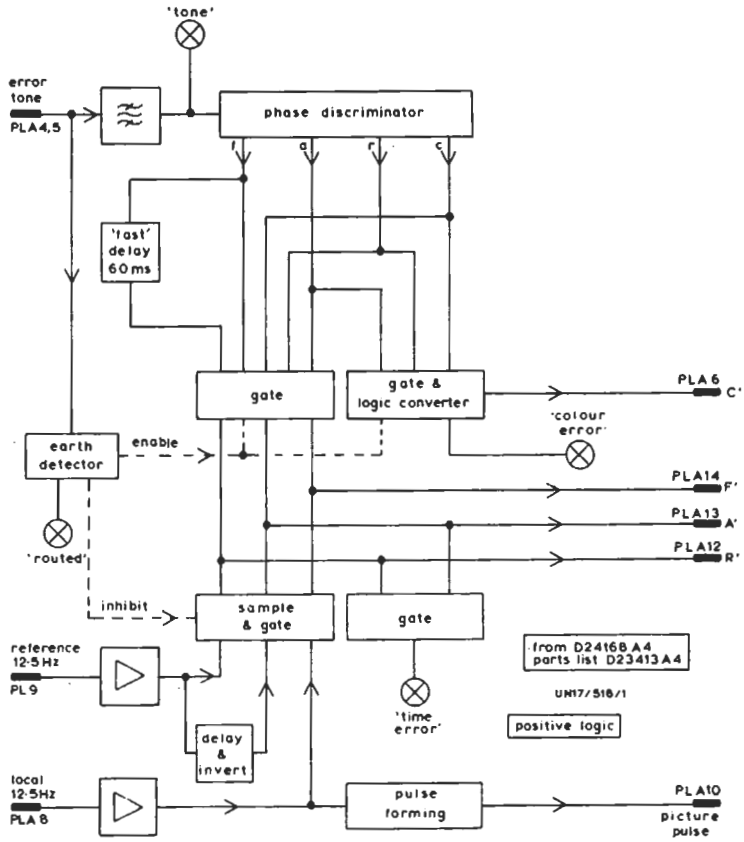

Fig. 1. Block diagram of the UN17/518

TABLE 2

Input Tone Frequency/Error Control Signal Outputs for Control Functions

Tone Frequency (Hz)	*Error-control Function*	*Error-control Signals (V)*			
		R' PLA12	A' PLA13	F' PLA14	C' PLA6
892	Fast Retard	−5	0	−5	0
977	Retard	−5	0	0	0
1071	Colour Retard	0	0	0	−2·5
1173	Normal	0	0	0	0
1285	Colour Advance	0	0	0	−6
1407	Advance	0	−5	0	0
1542	Fast Advance	0	−5	−5	0
1689	Test	0	0	−5	0

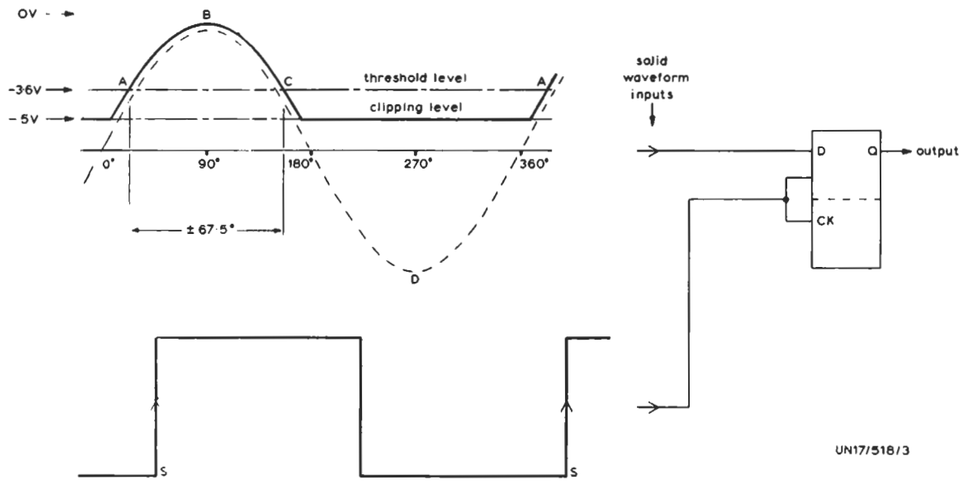

Fig. 2. Operation of the D-type bistable

Decoder Mode

Bandpass-filtered tone is fed to a phase-splitter network whose four outputs have relative phases of 0°, 90°, 180° and 270° over the whole tone error-signal frequency range. These outputs feed the D inputs of four D-type bistables[5]. The 90° output also feeds a network whose phase-shift is a function of frequency and which is an integral multiple of 45° for each tone error-signal frequency. The output of this network feeds a Schmitt trigger circuit which generates pulses to supply the *Clock* (CK) inputs of the four bistables. Thus the *Clock* inputs to the D bistables are delayed in phase relative to the D inputs by an angle proportional to tone frequency.

The D-bistable has the property that its Q output assumes the logic value of the D input at the positive-going edge of the clock pulse and maintains that value unitl the next clock pulse. This property is used in the UN17/518 to give a Q output of logic 1 whenever a positive-going clock-pulse edge occurs within ±67·5° of the peak-positive amplitude of the reference phase at the D input. (See Fig. 2.) This method of decoding is level-sensitive because the ±67·5° tolerance is determined by the positions of the threshold-crossing points on the D-input waveform. (The four reference phases are clipped below the threshold level to avoid reverse-biasing the D inputs.)

Each tone error-signal frequency can switch one or two bistables to give a logic 1 output. But, because each bistable responds to a different group of three frequencies, the logic combined outputs from the four bistables indicate unambiguously a specific frequency. The diagrams in Figs. 3 and 4 summarise this information.

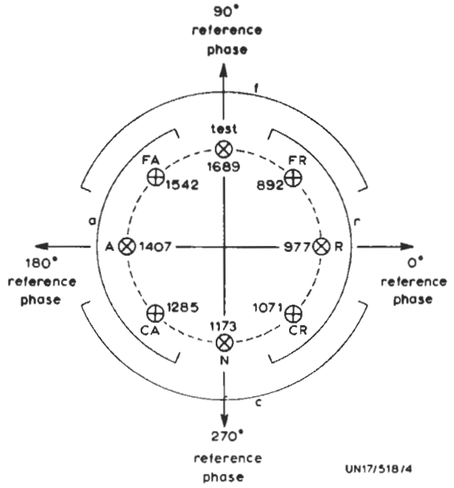

Fig. 3. Operation of the Phase Discriminator in the UN17/518

Notes:

1. The phase of each error signal frequency (from the frequency-variable phase-shifter) is shown on the dotted locus, relative to the four reference phases generated for each input tone.
2. The four arcs, labelled f, a, c, r indicate the phases over which a logic 1 will be generated by the associated bistable.
3. The decoder output control-functions FA, CR, etc., related unambiguously to the tone error signal frequencies 1542 Hz, 1071 Hz, etc., are shown adjacent to that frequency.

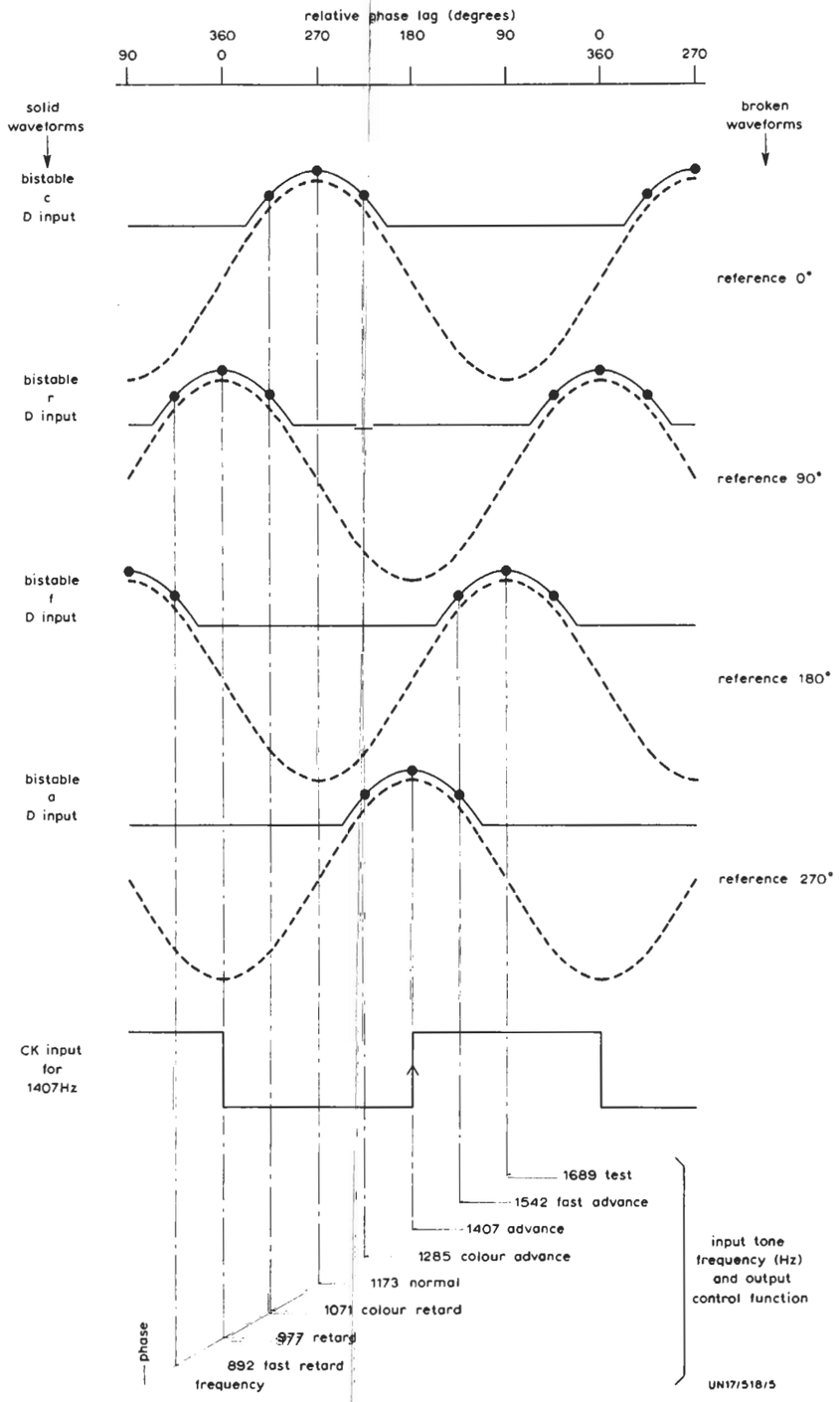

Fig. 4. Waveforms in the Phase Discriminator (showing as an example the clock-pulse phase for a 1407-Hz input)

Comparator Mode

Local 12·5-Hz squarewave is used to sample both reference 12·5-Hz squarewave and inverted reference 12·5-Hz squarewave, delayed by 20 μs. The output from the sampling gate, which uses two D bistables, indicates the presence and sense of any timing error greater than 20 μs between reference and local squarewaves as listed in Table 3. The *Comparator* mode is intended to provide approximate synchronism within a Common Clock area[6]. Hence only *Fast Advance* and *Fast Retard* error control signals are generated.

TABLE 3

Error Control Functions in the Comparator Mode

Relative Squarewave Phase	*Error-control Function*
Local Signal leads Reference Signal	Fast Retard
Local Signal lags Reference Signal by less than 20 μs	Normal
Local Signal lags Reference Signal by more than 20 μs	Fast Advance

Protection Circuits

The input Natlock error tone must not exceed the limits of 0 dB and −6 dB (w.r.t. 1 mW into 600 ohms) otherwise the decoding is liable to error. No executive action is taken in the UN17/518 to prevent this occurrence. Therefore tone not originated within the studio centre is usually fed to the UN17/518 via an equalising amplifier[7] with amplitude monitoring and cut-out facilities.

Protection operates in the *Fast* decoded output; a *Fast* signal must be decoded for about 60 ms before it is connected to the unit output. This precaution gives increased immunity from erroneously generated *Fast* signals.

In the timing comparator, loss of reference 12·5-Hz squarewave would result in a continuous error control signal at the output. To avoid this condition, a positive 60-ms pulse is generated from delayed reference squarewave so that the inverted output from the gate can go positive only during the 60-ms period.

Decoder-to-Comparator Changeover

Routing of error control signals to the output is done by logic gates connected to perform a change-over function operated by the earth-loop detector. Presence of a remote centre-tapped earth in the tone coder is detected at the centre tap of the input transformer. Error control signals from the *Decoder* section are then switched to the output.

Circuit Description

The circuit diagram of the UN17/518 is shown in Fig. 5. The following description relates to unit layout on numbered printed wiring boards.

Printed Wiring Board 1

The input band-pass filter L1, L2, L3, C1, C2, C3 accepts zero-level tone. The filtered tone is passed to a common emitter amplifier TR2 which has negative feedback applied via R102 and R2. The band-pass response at TR2 collector has 3-dB points at 800 Hz and 1800 Hz and +1 dB peaks near the band edges. Transistor TR1 is a so-called infinite-impedance detector feeding the *Tone* lamp circuit on Board 2. Resistor R6 in the emitter circuit of TR4 is set to operate the lamp with a −6 dB input signal. The base-emitter junction of TR1 is protected from reverse breakdown by D1.

Tone is fed to two phase-shifting circuits R12, C7 and R13,C9 from T2 in the collector circuit of TR2. The output from R12,C7 is taken to the base of emitter-follower TR8 on Board 2; the output from the junction R13,C9 is fed via emitter follower TR3 to T3. Outputs from this transformer are equal in amplitude to tone at the junction R12,C7.

The transformer T3 feeds the frequency-variable phase-shift network L4, L5, C12, C13, R17 and R18, the output from which is passed by emitter followers TR4 and TR5 to the Schmitt trigger TR6,TR7. Variable resistor R21 adjusts the bias on TR4 thereby altering the triggering phase of the Schmitt. Transistors TR5 to TR7 are fed from the −5V supply to suit the bistables.

Printed Wiring Board 2

Reference phase 0° is fed from Board 1 via emitter follower TR8 to the inverter stage TR9. All four reference phases are now available on Board 2:

0° at pin 12
90° at pin 14
180° at TR9 collector
270° at pin 16.

These signals are fed to four identical D-input drivers, TR10,TR11; TR12,TR13; TR14,TR15; TR16,TR17. The n-p-n stage in each driver enables the d.c. component of the output signal to be adjusted by R33. The p-n-p stage presents the correct driving impedance to the bistables.

The four bistables labelled *f, a, r, c* deliver logic-level outputs in accordance with the relative phases at their inputs, as described above for the *Decoder* mode.

A logic 1 output from bistable *f* (indicating that a *Fast* error tone frequency is present at the unit input) is passed by two routes to NAND gate IC4a. One is direct and the other via the *Fast* delay. Transistor TR36 (normally on) is turned off by a logic 1 from bistable *f*. Capacitor C37 discharges through R96 until, after about 60 ms, TR37 conducts and the Schmitt trigger TR38,TR39 operates thus turning off

POSITIVE LOGIC CONVENTION

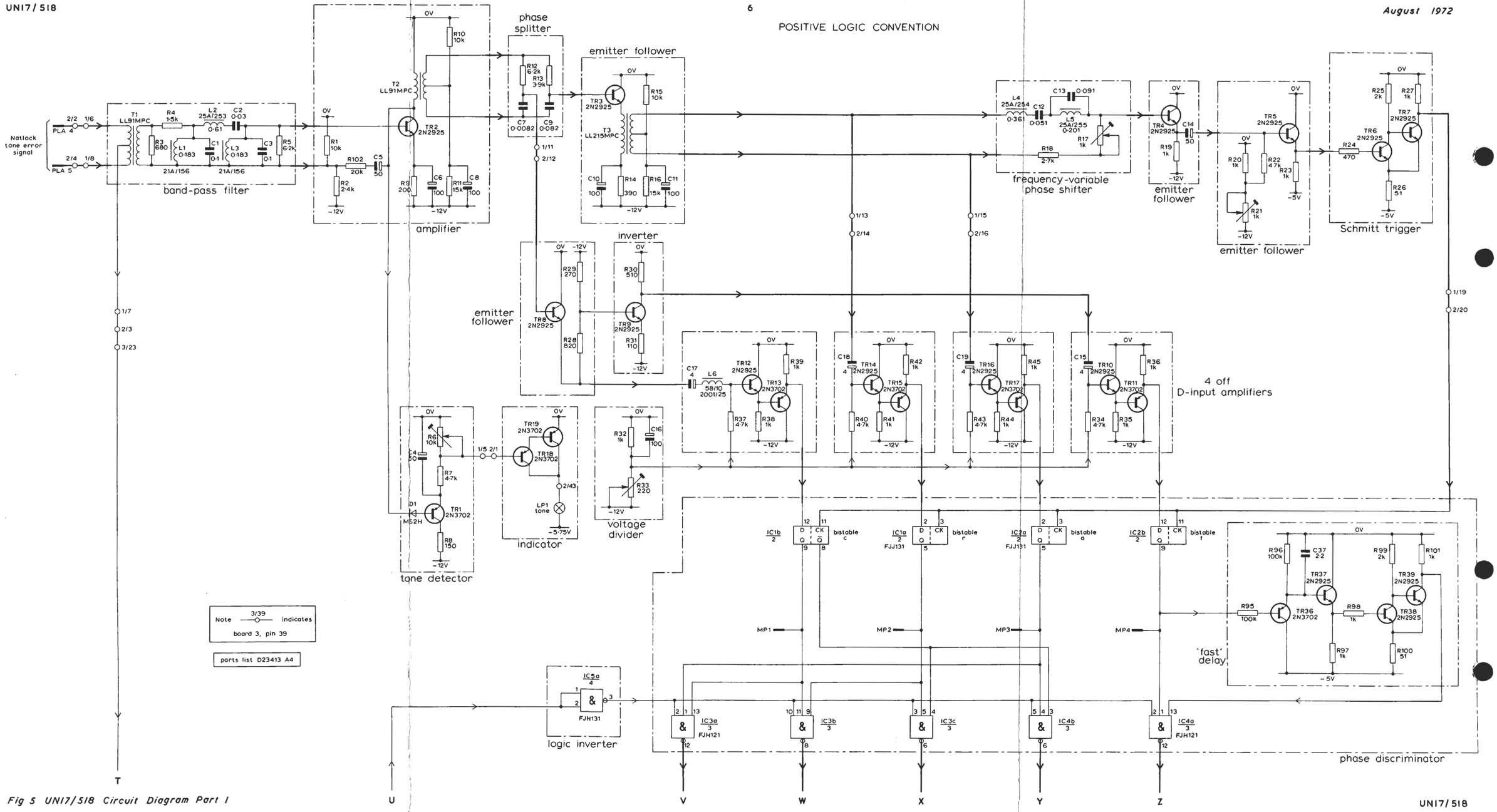

Fig 5 UNI7/518 Circuit Diagram Part 1

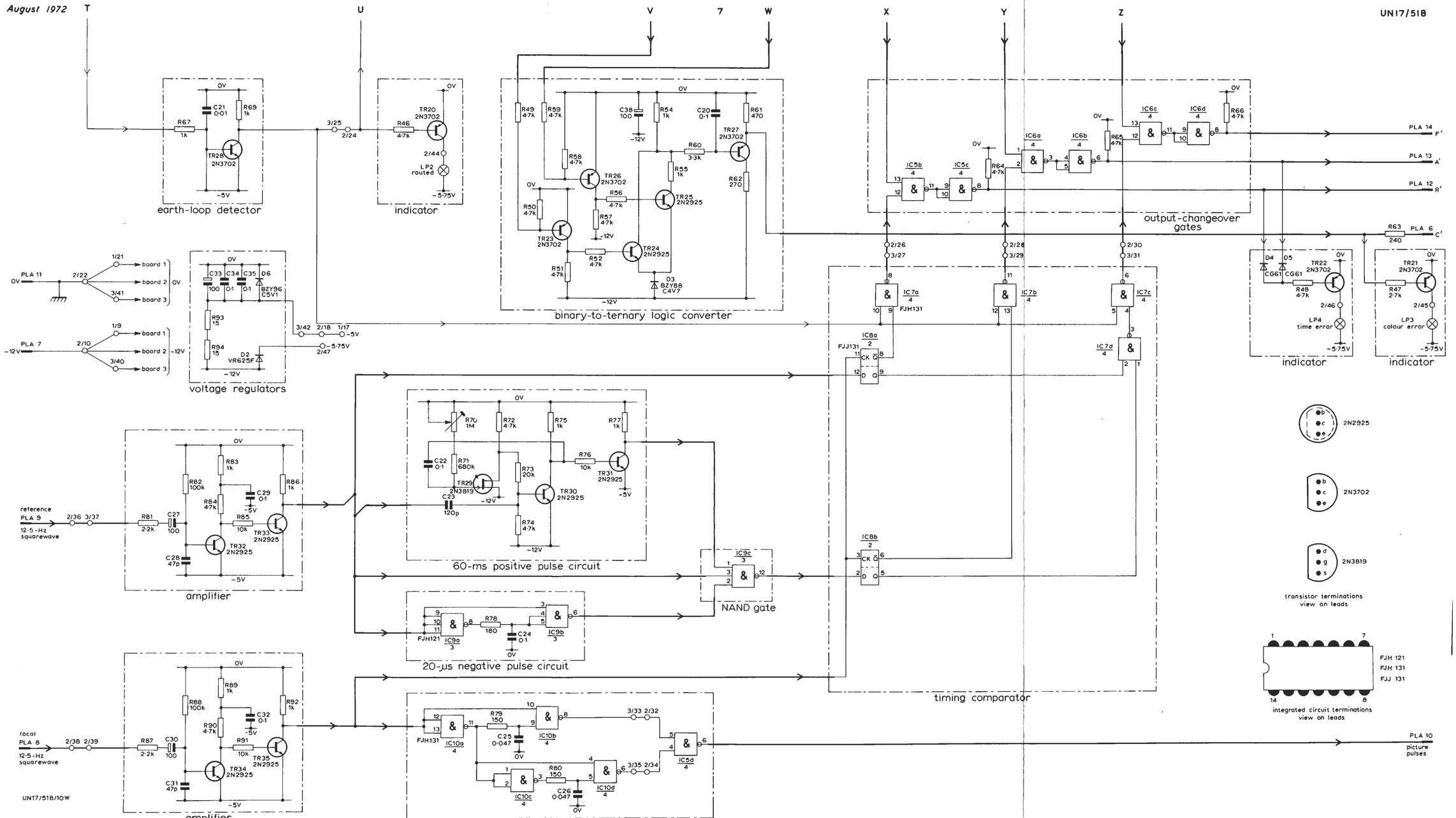

Fig 5 UN17/518 Circuit Diagram Part 2

Outputs from the four bistables *c, r, a, f* pass via monitoring points MP1-4 to logic gates whose outputs are binary-logic error-control signals C'_a, C'_r, R', A' and F'. The binary colour-error signals C'_a and C'_r are taken from IC3a and IC3b to the binary-to-ternary logic converter TR23-27.

When the bistables deliver signals to the converter which correspond to *Colour Advance* tone the inputs are −5V (C'_a = logic 0) from IC3a and 0V (C'_r = logic 1) from IC3b. The −5V signal turns on TR23 and so bottoms TR24 whose collector goes to about −6V. This potential is passed to the C' output on PLA6 via the low-pass filter R60,C20 and emitter follower TR27. Transistors TR25 and TR26 are both cut off.

Conversely, with a *Colour Retard* tone input, the outputs from IC3a and IC3b are 0V (C'_a = logic 1) and −5V (C'_r = logic 0) respectively. The −5V input turns on TR26 and so bottoms TR27. The −3V (approx.) potential at the junction R54,R55 is passed to the C' output. Transistors TR23 and TR24 are both cut off.

Gates IC3a, IC3b, IC3c, IC4b and IC4a receive a logic 1 from the inverter gate IC5a when an earth loop on the tone line is detected by TR28 on Board 3. This allows the gates to pass decoded error signals to the outputs. Decoded signals R', A', and F' are combined by changeover with comparator-generated signals in the gates IC5b, IC6a and IC6c. A logic inversion is performed by gates IC5c, IC6b and IC6d respectively to give the correct logic convention.

The Darlington pair, TR18,TR19 monitors detected tone level from Board 1 and powers LP1 *(Tone)* when the input level exceeds −6 dB.

TR20 conducts and LP2 *(Routed)* lights when an earth loop is detected by TR28.

TR21 conducts and LP3 *(Colour Error)* lights when a C', error-control signal of −3 or −6V is present on PLA6.

TR22 conducts and LP4 *(Time Error)* lights when R' or A' error-control signals of −6V are present on either PLA12 or PLA13. (D4 and D5 form an OR gate.)

Printed Wiring Board 3

Local and reference 12·5-Hz squarewaves from PLA8 and PLA9 feed two overdriven amplifiers TR34,TR35 and TR32, TR33 respectively. These amplifiers have a propagation delay of up to 15 μs.

Local 12·5-Hz squarewave from TR35 collector at 5V p-p and in phase with the input on PLA8 feeds both the *Clock* (CK) inputs of bistables IC8a and IC8b and also the short-pulse circuit IC10a,IC10b; a 4V p-p negative-going pulse of 8-μs duration is generated and this is triggered by the positive-going edge of the input.

A simplified diagram of the short-pulse circuit is given in Fig. 6. It performs a monostable function but the circuit is termed short-pulse because the gate input-tolerances are such that only short pulses can be generated by this technique. Both gates have a defined input threshold level and when the gate input signal crosses this level the gate output switches between logic levels. A logic 0 at the input of the circuit gives logic 1 outputs from both gates. When

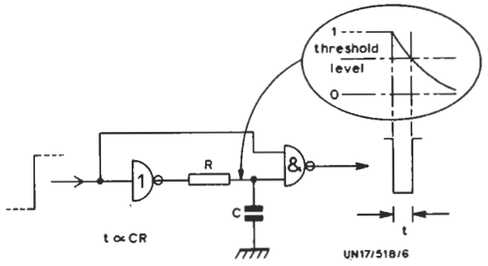

Fig. 6. The short-pulse circuit

the input changes to logic 1, gate A output goes to logic 0 immediately but the input to gate B remains above the threshold level for a duration depending on the time-constant CR. Gate B output therefore changes to logic 0 with the input transition but returns to logic 1 after the period determined by CR. There is no effect on the output when the input reverts to logic 0.

The inverted squarewave at IC10a output feeds an identical short-pulse circuit IC10c,IC10d to give a 4V negative-going pulse of 8-μs duration triggered by the negative-going edge of local squarewaves. Pulses from IC10b and IC10d are combined in IC5d on Board 2 to provide 4·5V positive-going pulses of 8-μs duration at 25-Hz repetition rate on PLA10.

Reference 12·5-Hz squarewave from TR33 collector at 5V p-p, in phase with the input on PLA9, is fed direct to the D input of IC8a. In addition the positive-going edge triggers both a monostable TR29 TR30, to give a 60-ms positive-going pulse from TR31, and also a short-pulse circuit IC9a,IC9b to give a 20-μs negative-going pulse from IC9b. The monostable is conventional but uses the high input impedance of a field-effect transistor to give the required time-constant without using a high-value electrolytic capacitor. The two pulses from TR31 and IC9b are combined with reference 12 5-Hz squarewave in IC9c to give an inverted reference squarewave with its negative-going edge delayed by 20 μs.

The *Clock* (CK) inputs of bistables IC8a and IC8b carry local squarewave which samples the logic values of both normal and inverted-delayed reference squarewaves at the D inputs; IC8a gives a $\overline{Q}$ = 1 output when *Retard* correction (of local-squarewave timing relative to reference) is required and IC8b gives a $\overline{Q}$ = 1 output when *Advance* correction is required. (See Figs. 7 and 8.)

The *Fast* signal is made by combining the Q outputs of bistables IC8a and IC8b in the NAND gate IC7d. Thus a *Fast* output is generated whenever a timing error is detected between squarewave inputs.

When an earth is detected on the centre tap of T1, transistor TR28 bottoms; this applies a logic 0 to to gates IC7a, Ic7b and IC7c (thereby holding their outputs to logic 1) and also to IC5a on Board 2. This process inhibits the *Comparator* mode and switches *Decoder* error signals to the outputs.

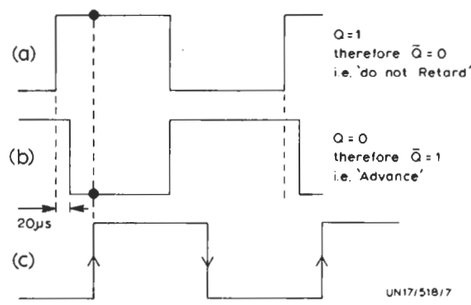

Fig. 7. Example of Waveforms causing Fast Advance Error-control Signals
(a) Reference 12·5-Hz squarewave (D input of IC8 a)
(b) Inverted and delayed reference 12·5-Hz squarewave (D input of IC8b)
(c) Local 12·5-Hz squarewave (Clock inputs of IC8a and IC8b)

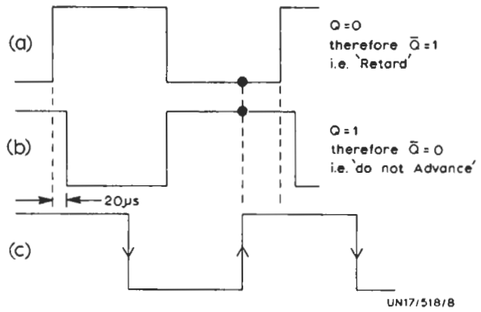

Fig. 8. Example of Waveforms Causing Fast Retard Error-control Signals
(a) Reference 12·5-Hz squarewave (D input of IC8a)
(b) Inverted and delayed reference 12·5Hz squarewave (D input of IC8b)
(c) Local 12·5-Hz squarewave (Clock inputs of IC8a and IC8b)

Alignment

Equipment Required

Dual-trace Oscilloscope with input addition and subtraction facilities
Natlock Tone Test Equipment EP14L/503
Feed of PAL subcarrier at 1V p-p across 75 ohms
Test circuit as shown in Fig. 9.

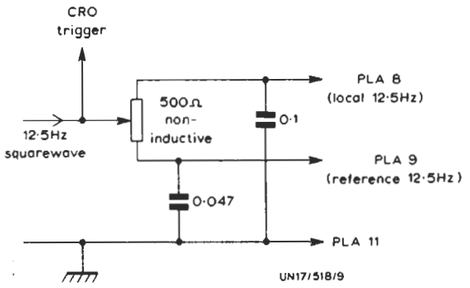

Fig. 9. Test circuit for the UN17/518 (Comparator section)

Procedure

a) General

1. Connect the tone output from the EP14L/503 to PLA4,5.
   Select *1173 Hz* and adjust the input level to −6 dB (w.r.t. 1mW into 600 ohms) using R31 in the Tone Encoder CD2/501 (part of the EP14L/503). The signal level at TR2 collector should be 8V p-p.
   Adjust R6 so that the *Tone* lamp just lights.

b) Frequency-variable phase-shifter

2. Adjust the input level to −4 dB. The signal level at TR2 collector should be 10V p-p.
   Trigger the oscilloscope from pin 11 on Board 1. Put one probe on pin 11 and the other on pin 13. Check (by noting zero crossings) that the waveform on pin 13 leads by 90° ± 3°.
3. Put both probes on pin 13 and adjust for equal gain. Move one probe to TR4 base and adjust the oscilloscope to add the inputs.
   Adjust L5 for minimum signal. (This sets the signals to be equal in amplitude with 180° relative phase shift.)
4. Select *1689 Hz* on the EP14L/503 and subtract the inputs on the oscilloscope.
   Adjust L4 for minimum signal. (This sets the signals to be equal in amplitude and phase.)
5. Move the probe from pin 13 to pin 11. Select *1407 Hz* and add the oscilloscope inputs.
   Adjust R17 for minimum signal.
6. Trigger the oscilloscope from pin 19 and switch to alternate trace; move the probe from pin 11 to pin 19.

Adjust R21 so that the positive-going edge of the squarewave occurs precisely at the positive-going zero-crossing of the sinewave.

c) Decoder

7. Remove *Strap C* in the CD2/501 and select *1071 Hz.* (This gives an output frequency of 1026 Hz from the Tone Encoder which is phase-shifted by 22·5° relative to 1071 Hz by the frequency-variable phase-shifter in the UN17/518.)
   Adjust R33 so that MP1 is on the point of going negative, or the lamps indicate that a *Colour Error* is about to change to *Time Error.* Replace *Strap C.*
8. Check that the Tone Decoder section gives error control signal outputs corresponding correctly to tone input frequency as indicated in Table 2.

d) Comparator

The squarewave input amplifiers introduce a delay of up to 15 μs. This must be allowed for when checking pulse coincidences.

9. Connect the 12·5-Hz squarewave to PLA8.
   Check PLA10 for 8-μs, 4·5-V positive-pulses occuring at both positive-going and negative-going edges of the input.
10. Connect the 12·5-Hz squarewave to PLA9.
    Check IC9 pin 12 for an inverted 4-V p-p squarewave with the negative-going edge delayed by approximately 20 μs from the positive-going edge of the input signal.
11. Check that 60-ms positive-going pulses triggered from the positive-going edge of the input appear at TR31 collector. Adjust the pulse duration with R70.
12. Use the test circuit in Fig. 9 and trigger the oscilloscope from the positive-going edge of the input.
    Monitor the waveforms at TR33 and TR35 collectors. Disconnect the tone input to PLA4,PLA5 and check that the outputs obey Table 3 (page 4) as the 500-ohm resistor is varied.
13. Connect the EP14L/503 tone output to PLA4,PLA5 and select *1173 Hz.*
    Check that all error control signals are 0V for all conditions of relative squarewave phase.

References

1. Tone Encoder CD2/501
2. Waveform Generator Drive Unit GE1L/537
3. Colour Subcarrier Phase Shifter EP1L/509
4. Stabilised Power Supply PS2/13F
5. *Switching and Logic Circuits*; Instruction G.3, Section 2.
6. *Picture Source Synchronising*; Instruction P.1
7. Natlock Tone Equalising Amplifier AM7/509

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