VARIABLE DIVIDER (GENLOCK) UN17/522

Introduction

The UN17/522 is used with the fixed divider UN17/502 in a waveform generator drive unit[1,2] to derive twice-line frequency from Natlock reference frequency. By using error control signal inputs the variable divider output signal can be changed in phase or frequency according to the combination of error signals. This divider differs from the UN17/501, for which it is a direct replacement, by providing fast genlock[3] operation.

The unit contains 15 bistable units UN9/528, separately described under that code, and is constructed on a CH1/26A chassis using index pegs 12 and 26.

General Specification

Signal Inputs

Natlock reference frequency	greater than 3 V p-p
rise-time of positive edge	less than 100 ns
Picture pulse	2 V p-p, positive pulse, 8 to 12 μs duration

Control Inputs

A', R', F', XF'	do nothing: 0V nominal change count: −6V nominal (Table 1 gives tolerances)

TABLE 1

Nominal voltage	*Actual voltage*
0	more +ve than −1·5
−6	more −ve than −4·5

Signal Output	5 V p-p squarewave
Normal frequency	2·486 kHz
Step correction	±0·2 degrees per picture period (translated to ±18 ns at output of UN17/502)
Fast correction	±5·6 Hz change
Extrafast correction	±108 Hz change
Power Input	−12 V, 250 mA d.c.
Temperature Range	0°C to 45°C ambient
Weight	0·75 kg (1 lb 10 oz)

Logic Description

The logic diagram of the UN17/522 is given in Fig. 1. The divider comprises two functions: an eleven-stage binary ripple-through divider and divider control gating to provide knockback pulses which change the division ratio of the divider. The operating modes and corresponding division ratios are listed in Table 2.

TABLE 2

Operating Mode	*Division Ratio*
Normal	1782
Retard	1783 once per picture, then 1782
Advance	1781 once per picture, then 1782
Fast Retard	1786
Fast Advance	1778
Extrafast Retard	1864
Extrafast Advance	1708

Divider

The divider is in two series-connected sections: bistables CM1-4 which have a maximum count of 16, followed by CM6-12 which have a maximum count of 128. These maxima are never reached because both counts are modified by some or all of three groups of knockback:

- once per picture period after a picture pulse has reset CM13, when the counter output next goes positive, bistables CM1 can be reset by CM14 and bistable CM2 *not* reset by CM15; this knockback occurs during all modes except *Normal* but assumes significance only for *Advance* and *Retard* modes;
- once in each counter output period, when the output goes negative CM5(Q1) also goes negative and 16 input pulses later goes positive; this positive transition forms knockback pulse (a) which modifies both the count of CM2-4 and CM6-10; this is used in *Fast* and *Extrafast* modes;
- once in each counter output period, when the output goes positive the transition not only sets CM13-15 (for the first group of knockback) but also resets CM3 with knockback pulse (b) according to the *R.XF* signal; this is used only in the *Extrafast* mode.

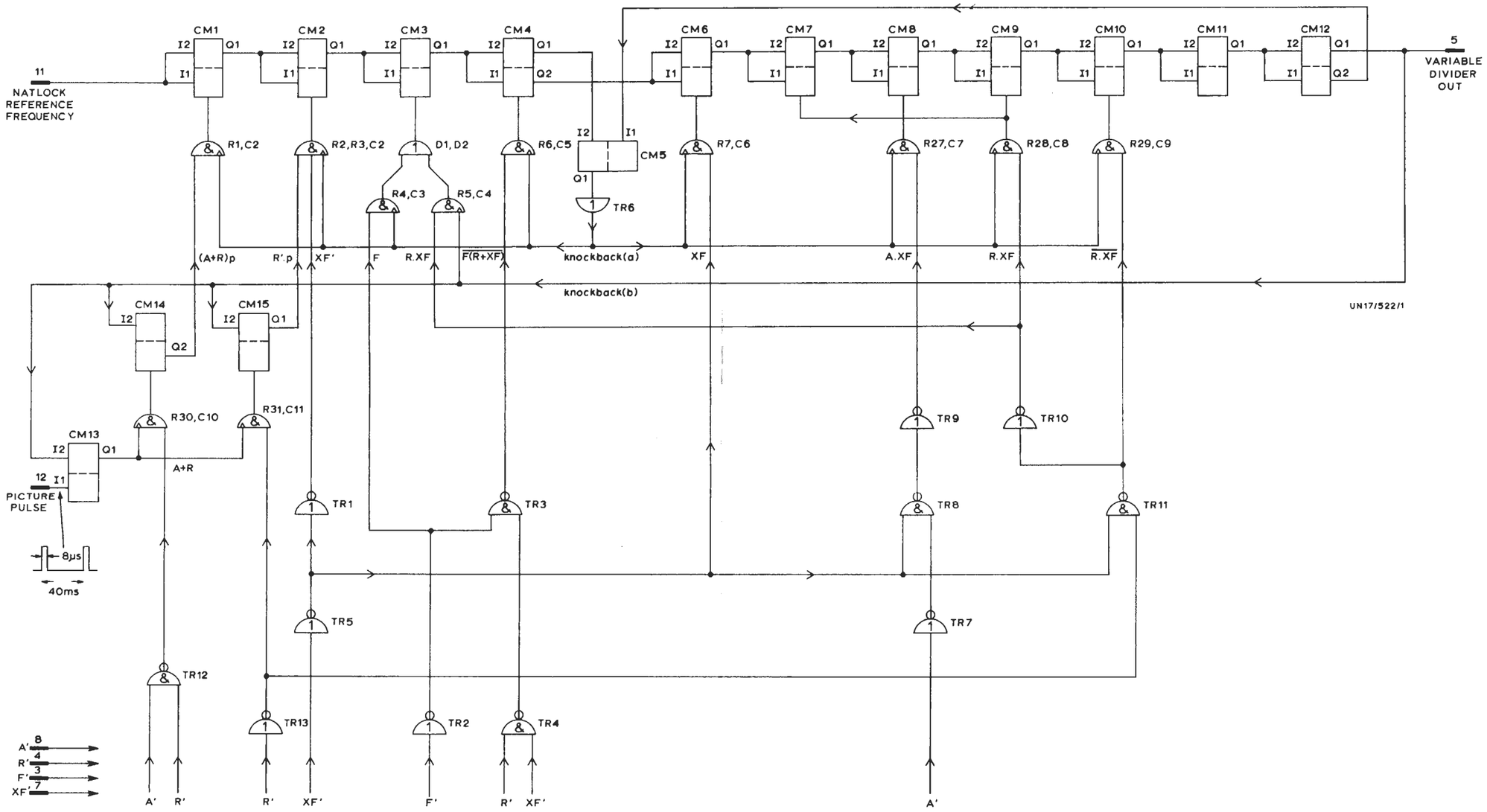

Fig. 1. Logic Diagram of the UN17/522

Counter Control Circuit

Bistables CM13 to 15 are used to change the division ratio once in every picture period for *Advance* and *Retard* modes. Bistable CM13 converts the random timing of a picture-pulse input into a positive transition at the start of the next count. This transition enables CM14 to gate one feedback pulse per picture period to CM1 except in *Normal* mode. It also enables bistable CM15 to inhibit one feedback pulse per picture period to CM2 in *Retard* or *Fast Retard* modes. This action is shown in Fig. 2.

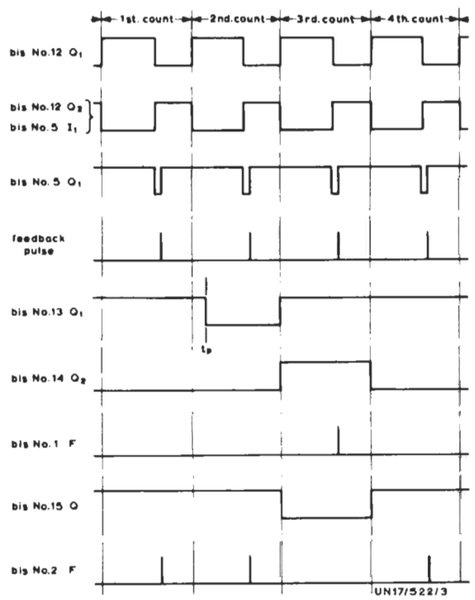

Fig. 2. Waveforms in the UN17/522 illustrating how one knockback pulse per picture is selected or inhibited; (picture-pulse input at time t_p in second count shown)

The remaining control circuitry uses conventional transistor gating to provide control signals which are gated to the appropriate bistable by the knockback pulses (a) and (b).

Fig. 3 summarises the final stage of gating and gives the binary count weighting in each section of the divider. Table 3 lists the control signals applied at that stage. The following division ratios can be derived from Fig. 3 and Table 3. (Use the fact that when knockback is applied to bistable in a divider the maximum count is reduced by the binary weighting of that bistable in the divider.)

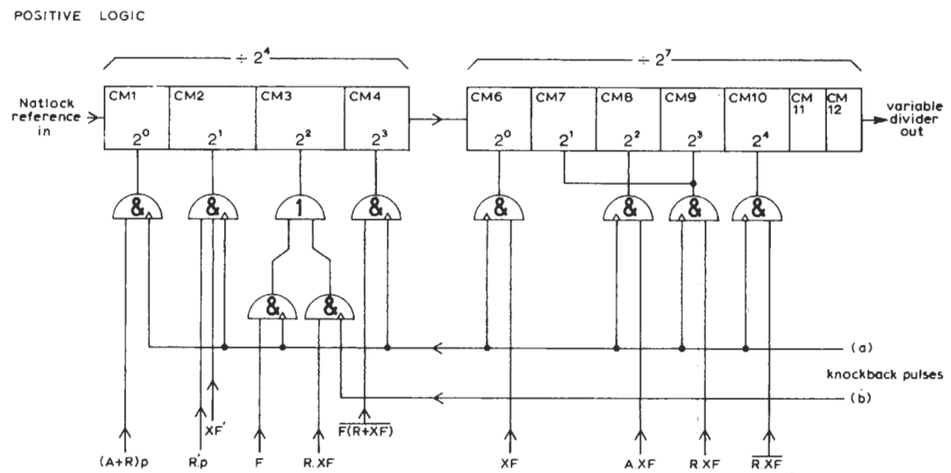

Fig. 3. Final Stage of Feedback Gating in the UN17/522

TABLE 3

Operating Mode	*A'*	*R'*	*F'*	*XF'*	*(A+R)p*	*R'.p*	*XF'.a*	*F.a*	*R.XF.b*	$\overline{F(R+XF)}.a$	*XF.a*	*A.XF.a*	*R.XF.a*	$\overline{R.XF}.a$
Extrafast Retard	1	0	0	0	(1) 0	(0) 1	0	1	1	0	1	0	1	0
Fast Retard	1	0	0	1	(1) 0	(0) 1	1	1	0	0	0	0	0	1
Retard	1	0	1	1	1 (0)	0 (1)	1	0	0	1	0	0	0	1
Normal	1	1	1	1	0	1	1	0	0	1	0	0	0	1
Advance	0	1	1	1	1 (0)	1	1	0	0	1	0	0	0	1
Fast Advance	0	1	0	1	(1) 0	1	1	1	0	1	0	0	0	1
Extrafast Advance	0	1	0	0	(1) 0	1	0	1	0	0	1	1	0	1
													2^1	
					2^0	2^1		2^2		2^3	2^0	2^2	2^3	2^4
						knockback weighting in maximum count of 2^4						knockback weighting in maximum count of 2^7		

a: gated by knockback (a)
b: gated by knockback (b)
p: gated by picture pulse
Bracketed digits are the significant gating for that mode

(a) *Normal*

Count is $2^4(2^7 - 2^4) - (2^1 + 2^3) = 1792 - 10 = 1782$

normal count of CM1-4 — count of CM5-12 with knockback (a) to CM10 — picture-pulse gated knockback (a) to CM2&4

(b) *Retard*

Count is *Normal* except once per picture period when the counts of CM1 and 2 are modified (see Fig. 2) to give the count:

$$2^4(2^7 - 2^4) - (2^0 + 2^3) = 1792 - 9 = 1783$$

(c) *Advance*

Count is *Normal* except once per picture period when the counts of CM1 and 2 are modified (see Fig.2) to give the count:

$$2^4(2^7 - 2^4) - (2^0 + 2^1 + 2^3) = 1792 - 11 = 1781$$

(d) *Fast Retard*

Count is $2^4(2^7 - 2^4) - (2^1 + 2^2) = 1782 - 6 = 1786$

(e) ***Fast Advance***

Count is $2^4(2^7 - 2^4) - (2^1 + 2^2 + 2^3) = 1792 - 14 = 1778$

(f) *Extrafast Retard*

Count is $2^4 \left[2^7 - (2^0 + 2^1 + 2^3)\right] - (2^2 + 2^2) = 16(128 - 11) - 8 = 1864$

normal count of CM1-4 — count of CM5-12 with knockback (a) to CM6,7,9 — knockback (a) gated to CM3, knockback (b) gated to CM3

(g) *Extrafast Advance*

Count is $2^4 \left[2^7 - (2^0 + 2^2 + 2^4)\right] - 2^2 = 16(128 - 21) - 4 = 1708$

normal count of CM1-4 — count of CM5-12 with knockback (a) to CM6,8,10 — knockback (a) gated to CM3

Circuit Details

Fig. 4 gives the circuit diagram of the UN17/522.

All the bistable elements used are UN9/528 and are described separately under that code. The resistor-capacitor AND gates used in the final stage of knockback gating are also described in that Instruction.

Combinational gating of the control inputs is performed by conventional transistor circuitry.

Maintenance

The UN17/522 is tested as part of its parent unit[1,2]. The knockback gating may be checked if necessary by observing the waveform at the output of the appropriate bistable. Trigger the oscilloscope from the negative transition at pin G and check that the bistable is reset at the time pin G goes positive.

References

1. Waveform Generator Drive Unit GE1/520A
2. Waveform Generator Drive Unit GE1L/537A
3. *Picture Source Synchronising;* Instruction P.1, Section 4

RDH 6/72

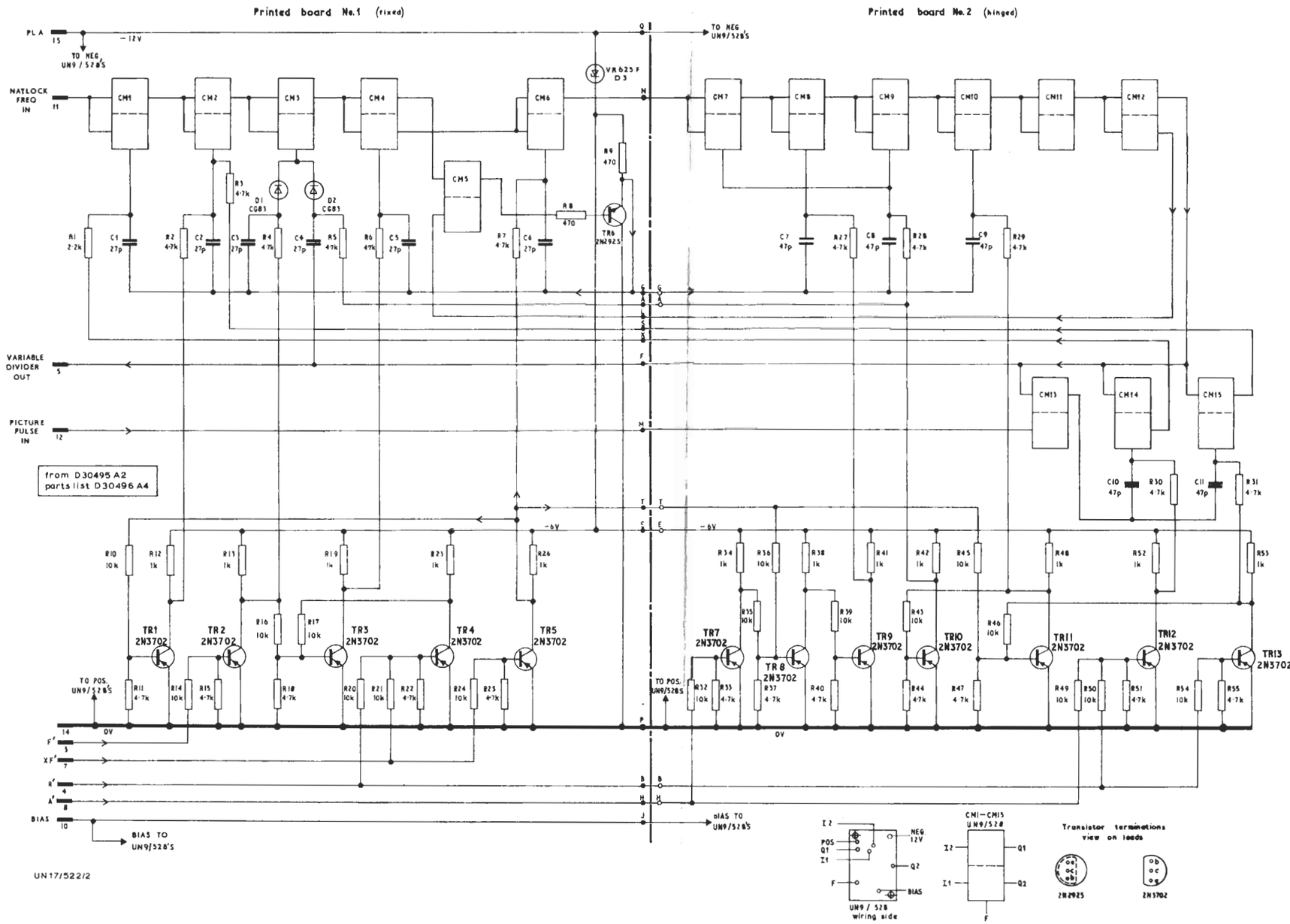

Fig. 4. Circuit Diagram of the UN17/522