PAL DECODER CHROMINANCE UNIT UN18/504

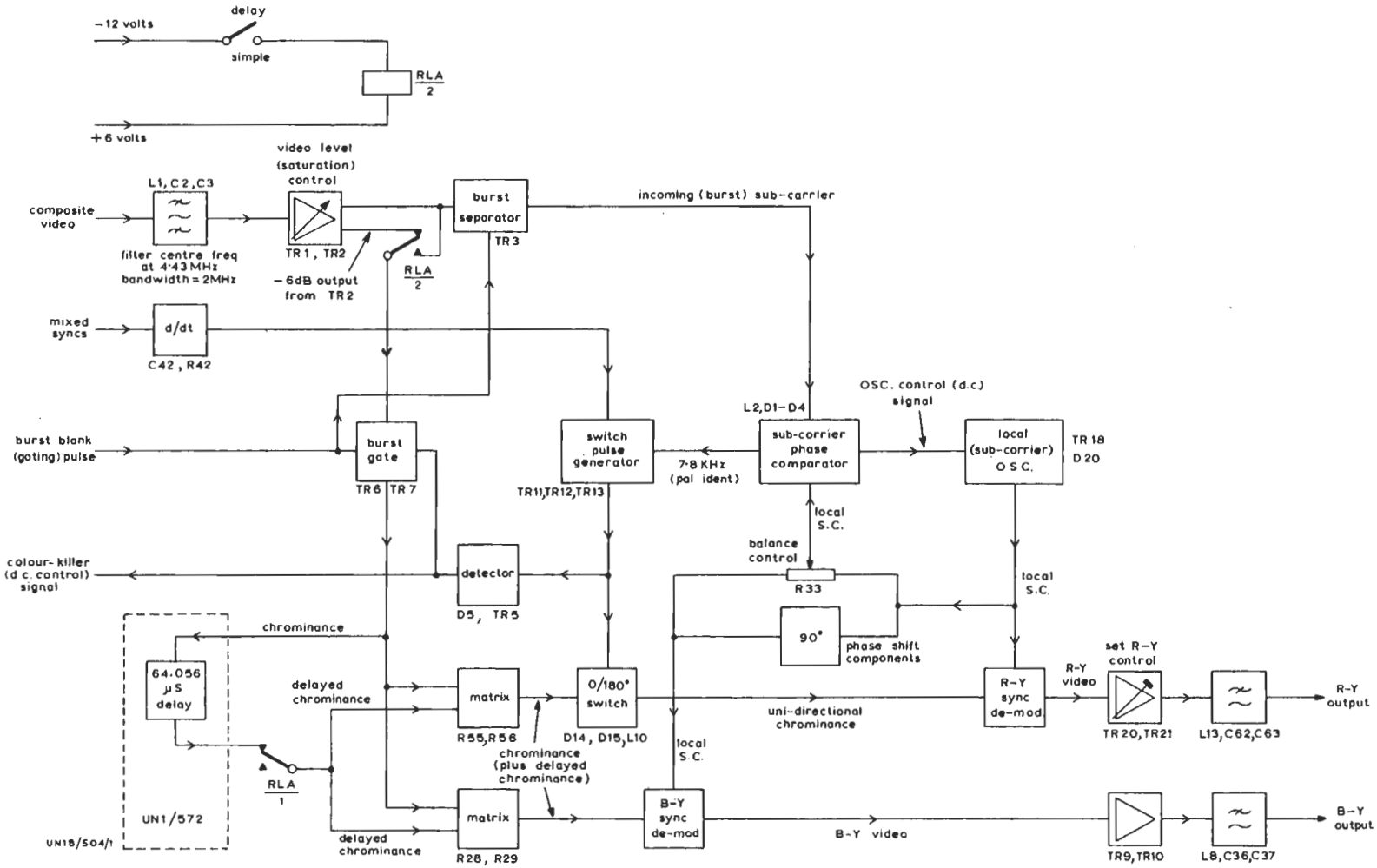

Fig. 1. Block Diagram of the PAL Decoder Chrominance Unit UNIB/504

Introduction

The UN18/504 accepts a colour-coded composite video signal at standard level and produces two colour-difference signals (R–Y) and (B–Y) at about 1·8 volts p-p and 1·3 volts p-p, respectively. Two subsidiary inputs are required by the unit; these consist of a feed of negative-going mixed-sync pulses and a feed of positive-going line-rate pulses of 4-μs duration which are used in burst-gating and burst-blanking circuits.

The UN18/504 normally forms part of a 625-line PAL decoding equipment[1,2]; for use in the delay-line method of chrominance-signal interpolation therefore the unit also produces a chrominance-signal output which is routed to a one-line delay circuit (contained in a separate unit[3]) and returned from there to the UN18/504 without loss of level.

The unit is constructed on a CH1/12A chassis with index-peg positions 3 and 39. It requires power supplies of +6 and −6 volts, together with a relay-operating supply of −12 volts[4].

General Specification

Input Level	1·3 volts p-p
Input Impedance (at 4·43MHz ± 1MHz)	greater than 68 ohms.
Output Levels	
(R–Y) signal (normal)	1·8 volts p-p
(B–Y) signal (normal)	1·3 volts p-p
Amplitude/Frequency Response	
Chrominance signal (w.r.t. level at 4·43MHz)	−2 dB at ±1MHz −6 dB at ±1·6 MHz
Colour-separation signals	Flat to 1·5 MHz
Chrominance Signal Level (to and from 1-line delay)	1·5 volts p-p
Mixed-sync Pulse Input Level	2 volts p-p
Burst-blanking Pulse Input Level (positive-going pulse; 4μs half-amplitude duration)	6 volts p-p
Colour-killer Signal Output (d.c.)	
For monochrome video input	−1·5 volts
For colour-coded video input	−3 volts
Power Supplies	
Regulated	+6, −6 volts, 110 mA
Unregulated (relay supply)	−12 volts, 35 mA

General Description

Fig. 1 is a block diagram showing the main circuit functions of the UN18/504.

Composite video signals are applied first to a band-pass filter which accepts only the chrominance signal components and thence to a two-stage variable-gain amplifier. The amplified and filtered signal is then fed to a burst-blanking circuit where the burst is removed and two chrominance-signal outputs in phase opposition are produced; these signals are fed to separate matrix circuits. A feed of one of the signals is also taken to a delay-line in another decoder unit[3] so that, when the delay method of decoding is used (for which the relay contacts are as shown in Fig. 1), a chrominance signal delayed by one television line-period is available to form a second input to each of the two matrices.

The incoming chrominance signal is also fed to a burst-gating amplifier (operated by the same pulses as the burst-blanking circuit) which provides an output of separated reference bursts to a phase-comparator where they are compared with the signal from a local crystal-controlled oscillator. One resultant of the comparison process is a d.c. control signal which is applied to a capacitance diode (varactor) forming part of the oscillator circuit. The oscillator is thus included in a phase-control loop. This loop also contains variable resistor R33 (BALANCE) which enables the phase of the locally-generated sub-carrier to be initially set so that it is suitable for direct application to the R–Y and B–Y synchronous demodulators.

A second output from the phase comparator is the 7·8-kHz PAL squarewave signal the polarity of which identifies the phase of the swinging reference burst. The signal is first processed in a tuned amplifier and the resulting 7·8-kHz sinewave, together with a train of differentiated line-sync pulses, is then applied to a multivibrator which generates the correctly-timed pulses (also of square waveform) required to operate the switched signal-inverting circuit interposed in the chrominance-signal feed to the R–Y demodulator.

The squarewave switching pulses are also routed

to a diode detector and d.c. amplifier circuit which thereby produces one of two voltages depending on whether or not pulses are present. These alternative voltages form the colour-killer signal which is used to inhibit the chrominance-signal output of the burst-blanking circuit if the incoming video is not colour-coded. The colour-killer signal is also fed out of the UN18/504 to operate an electronic switch in another decoder unit[3].

The matrix circuits mentioned earlier provide the chrominance-signal outputs which are applied to two synchronous demodulators for decoding the R–Y (fed via the inverting switch) and B–Y colour-difference signals. The required phase difference of exactly 90 degrees between the two demodulator local-subcarrier feeds is provided by components associated with the BALANCE control (R33).

The two colour-difference signals are amplified (with pre-set adjustment of the R–Y amplifier gain) and fed through low-pass filters before being routed to another decoder unit[5] for derivation of the G–Y colour-difference signal and final translation to the colour-separation signals, R, G and B.

Circuit Description

Fig. 2 shows the complete circuit diagram of the UN18/504.

Input Circuit

Composite video signals entering the unit are applied to a filter comprising L1, C2 and C3, and thence to emitter follower TR1. The filter has a pass band centred on the chrominance subcarrier frequency (4·43 MHz) and a bandwidth of about 2 MHz; transformer L1 is over-coupled so that peaks occurring at 3·4 MHz and 5·4 MHz compensate for losses in the overall chrominance-signal response of the unit. (These losses are mainly associated with transformers L4 and L5 in the burst-blanking gate.)

The circuit of TR1 contains variable resistor R5, which is used for pre-set level adjustment of chrominance signals fed to the remainder of the unit. This is the saturation (SAT) control.

TR2 is also an emitter-follower and provides two outputs. One is routed to the burst-gating amplifier and phase-comparator driver stage TR3, and the other goes to a burst-blanking circuit comprising TR6 and TR7. The feed to TR6 and TR7 is taken from a variable tapping point on TR2 emitter load so that a necessary 6-dB difference in signal level (between the tapping point and the direct connection to TR2 emitter) can be obtained (see *Burst-blanking Gate*).

Burst-blanking Gate

Chrominance signals from TR2 are fed to the primary of transformer L4 via contacts on relay RLA which are changed over when the decoder is switched between the SIMPLE and DELAY modes of operation.

The gate circuit comprising L4, L5, TR6 and TR7 is used to remove the reference burst from the chrominance signal. TR6 and TR7 are non-conductive in the presence of the positive-going pulses routed to the UN18/504 from another decoder unit[4]; these pulses are of 4 μs duration and have leading edges coincident with the trailing edges of line-sync pulses. The gate is of the balanced type so that switching transients can be reduced to an acceptable minimum by adjustment of R26.

Two outputs of burst-blanked chrominance signal are taken from transformer L5 via matrix circuits R28, R29 and R55, R56; one of these outputs is inverted with respect to the other because they are taken from opposite sides of the transformer centre tap.

A feed of the burst-blanked chrominance signal is routed to a 64·056-μs delay line located in another decoder unit[3]. When the equipment is used with delay-line interpolation of chrominance signals, the returned (delayed) signal passes through a second set of relay RLA contacts before being mixed with undelayed signals in the two matrices. The 6-dB change in chrominance-signal level (see *Input Circuit*) which occurs when the relay is operated compensates for signal addition in the matrices when these are fed with delayed signals.

The (mixed) chrominance-signal outputs of the matrix circuits are applied to two synchronous demodulators which are described later.

Phase Comparator and Burst-locked Oscillator

Chrominance signals from the emitter of TR2 are fed to TR3 in parallel with a feed of the pulses used in the burst-blanking circuit. TR3 is biased so that only the more positive parts of the base signal (subcarrier burst superimposed on the 6-volt positive pulse) are amplified and available as an output from the tuned transformer L2; neutralising capacitor C10 reduces break-through of chrominance information.

L2 applies the incoming reference bursts to two phase-comparison circuits containing diodes D1, D2 and D3, D4. A feed of subcarrier from the burst-locked oscillator TR18 is also routed to the comparator circuit via the BALANCE control R33, buffer amplifier TR4 and tuned circuit L3.

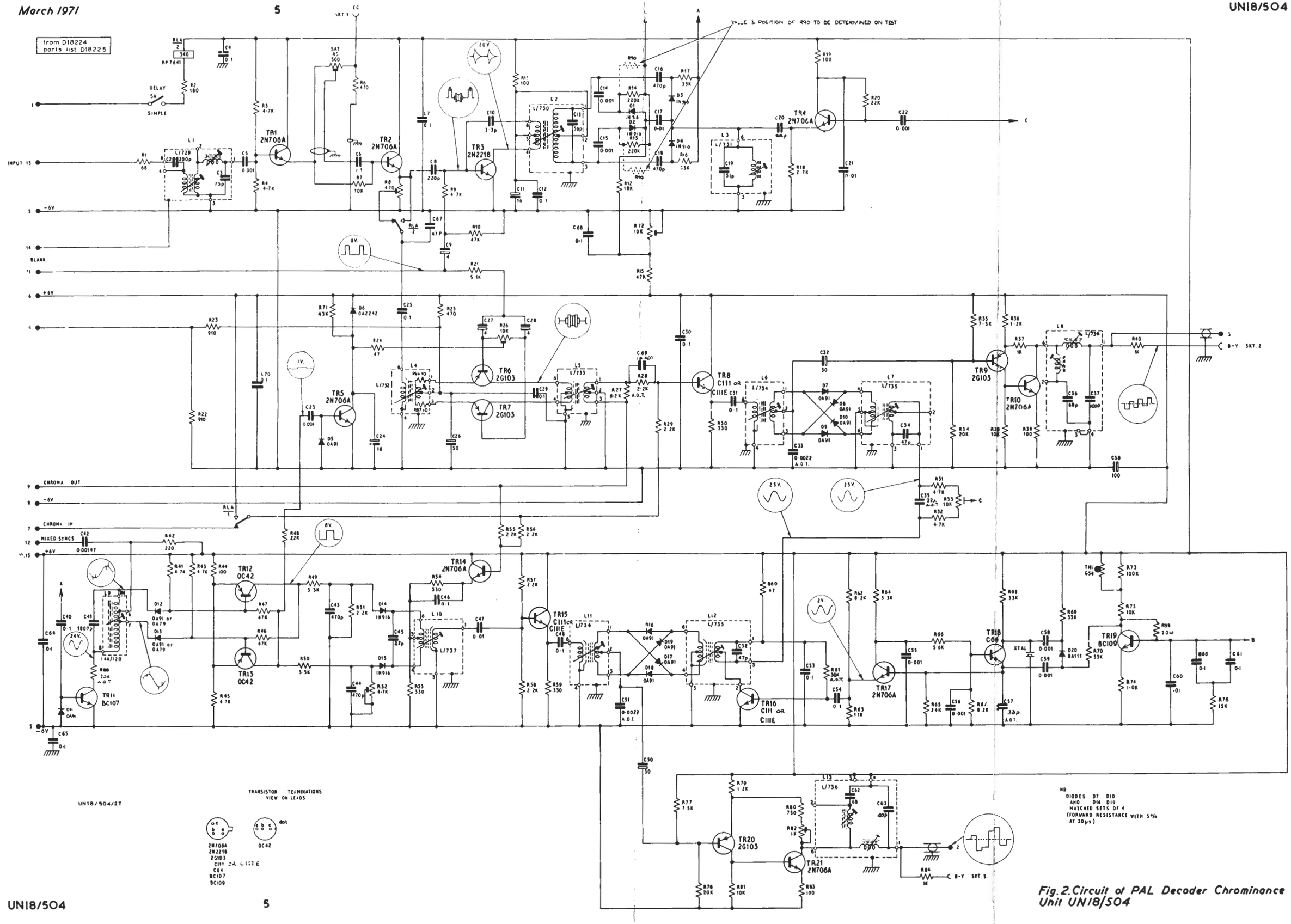

Fig. 2. Circuit of PAL Decoder Chrominance Unit UN18/504

Diodes D1 and D2 operate as peak synchronous phase detectors and produce an output which is pro portional both to the burst amplitude and to the phase difference between the two subcarrier signals. This varying d.c. output is direct-coupled via an integrating circuit to d.c. amplifier TR19. The output from TR19 is used to vary the capacitance of diode D20 which acts as a frequency-controlling feedback component for crystal-controlled oscillator TR18. The oscillator is thus included in a phase-control loop with the phase of the locally-generated signal adjusted (by means of R33) so that it is suitable for use in the R–Y demodulator (i.e. the output from TR16 is arranged to be in the V-axis phase of the quadrature-modulated incoming chrominance signal).

7·8-KHz Switch-pulse Generator

The second phase-detector circuit (D3, D4) has a sufficiently short time-constant to resolve the changes of incoming burst phase occurring on consecutive lines, and therefore produces an output of pulses with square waveform and of 7·8 kHz fundamental frequency. These pulses are fed to the base of TR11 which has a collector load (L9) tuned to 7·8 kHz; diode D1 ensures that any asymmetry in the 7·8-kHz signal from the phase comparator does not cause mis-triggering of the following bistable circuit.

A feed of differentiated mixed-sync pulses is connected to a tapping point on L9 so that the output signal applied to diodes D12 and D13 appears as a sine wave with superimposed spikes (as shown by the appropriate waveform-diagram inset on Fig. 2). D12 and D13 are biased to pass only those negative-going spikes which occur near the negative half-cycle peaks of the sine wave. These spikes are used to trigger a bistable circuit (TR12, TR13) which thereby produces a regenerated PAL square-wave signal with both negative and positive-going transitions accurately timed by the leading edges of line-sync pulses.

A subsidiary output from the multivibrator is taken to a detector circuit comprising D5, TR5 and C24. When a colour-coded signal is received by the unit, the PAL squarewave signal is present, and TR5 conducts on alternate half cycles of the applied signal. The resulting change in TR5 collector voltage represents the colour-killer signal which is used to inhibit the passage of chrominance signals through the burst-blanking gate (TR6, TR7) if the input video is monochrome. Zener diode D6 prevents saturation of TR5 so that a suitable bias exists both for the correct operation of TR6 and TR7, and for an electronic switch elsewhere in the decoder equipment[3].

Signal-inverting Switch

The switching signal developed by TR12 and TR13 controls the conduction of diodes D14 and D15. The output from one of the two matrices used to mix delayed and undelayed chrominance signals (for delay-line decoding) is applied to emitter-follower TR14. A centre-tapped transformer L10 forms the load on this stage and the signal path is completed through either D14 or D15 depending on which is made conductive by the switching signal. The conduction sequence of these two diodes is arranged so that the chrominance-signal output from L10 secondary changes polarity in such a way as to counteract the line-by-line phase reversal of the V-axis modulation which carries R–Y information in the incoming colour-coded signal.

Emitter-follower TR15 feeds the output from L10 to a synchronous demodulator which decodes the R–Y colour-difference signal.

R – Y and B – Y Synchronous Demodulators

The R–Y and B–Y signals are extracted from the incoming chrominance signal by two identical balanced-ring demodulator circuits. The R–Y demodulator mainly comprises diodes D16 to D19 together with transformers L11 and L12; diodes D7 to D10, with transformers L6 and L7, form the B–Y demodulator.

The chrominance signal from the switched inverting circuit described above are fed to the primary of L11 from emitter-follower TR15. A subcarrier signal from the burst-locked oscillator is applied to the centre-tap through TR17 and TR16. The peak levels of the incoming modulated subcarrier are sampled every half-cycle by the diodes as they are biased into conduction by the constant-level local subcarrier signal. The voltage which appears between the transformer secondary centre taps varies in proportion to these samples, and is therefore the original modulating colour-difference (R–Y) signal.

The B–Y demodulator operates in an exactly similar manner to that given above. One important difference in the application of the two demodulating processes, however, concerns the 90-degree phase shift which affects the feed of local subcarrier applied to L7 (in the B–Y demodulator). This phase shift is obtained by critical coupling (via C35) of tuned circuits L12 and L7 and is necessary because of the quadrature relationship between the two incoming modulated subcarrier signals.

Colour-difference Signal Video Amplifiers

The R–Y and B–Y signals represent the main unit outputs. They are produced by two similar cir-

cuits each of which receives an input from one of the synchronous demodulators and feeds the resulting colour-difference signal to another unit[5] for recovery of the R, G and B components.

TR20 and TR21 are connected as a complementary pair with variable resistor R82 in the collector circuit of TR21 providing pre-set adjustment for the R–Y output signal level. L13 and associated components form a low-pass filter network which removes any unwanted signals which are outside the chrominance band.

The B–Y signal output circuit is identical to that described above except that it does not include a pre-set gain control.

Alignment and Maintenance

The UN18/504 is normally aligned and maintained as part of a complete decoder. In the Instruction for the parent equipment[1], some notes are given on maintenance of this unit.

References to Typical Associated Equipment

1. PAL 625-line Colour-signal Decoder GE1L/528
2. PAL/N.T.S.C. 625/525-line Colour-signal Decoder GE1L/529
3. PAL Filter and Delay Unit UN1/572
4. Sync Separator Unit UN1/540
5. Colour-signal Decoder Luminance Unit UN19/503

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