# N.T.S.C. COLOUR-SIGNAL DECODER CHROMINANCE UNIT UN18/505

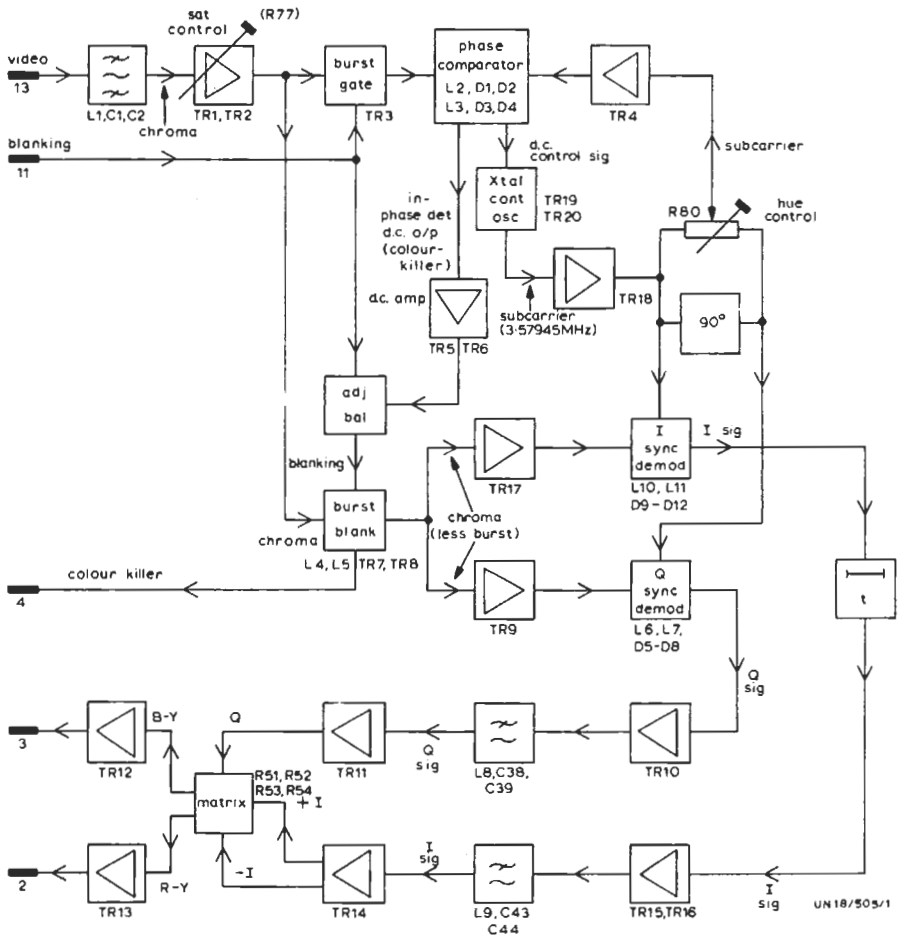


*Fig. 1 Block Diagram of the UN18/505*

**Introduction**

The UN18/505 accepts a colour-coded video signal at standard level and produces two colour-difference signals (R–Y and B–Y) at about 1·4 volts p-p. A subsidiary input required by the unit consists of a train of positive-going, line-rate pulses (Burst-blanking Pulses); each pulse is of 4 μs duration and has its leading edge coincident with the trailing edge of a line-sync pulse.

The UN18/505 normally forms part of a 525-line N.T.S.C. decoding equipment[1,2] and, as a subsidiary output, produces a d.c. signal (the colour-killer signal) which adopts one of two possible voltage values depending on whether or not the local subcarrier oscillator is locked in frequency to the incoming video-signal subcarrier.

The unit is constructed on a CH1/12A chassis with index pins at positions 4 and 38. It requires power supplies at +6 and –6 volts.

**General Specification**

| | |
|---|---|
| *Input Level* | 1·4 volts p-p |
| *Output Levels* | |
| B–Y Output (normal level) | 1·3 volts p-p |
| R–Y Output (normal level) | 1·5 volts p-p |
| *Amplitude/Frequency Response* | |
| I Channel | –2 dB at 1·3MHz<br>–6 dB at 1·8MHz |
| Q Channel | –2 dB at 400 kHz<br>–6 dB at 600 kHz |
| *Signal Delay* | 0·7 μs approx. |
| *Burst-blanking Pulse Input Level* (positive-going pulse of 4 μs duration) | 6 volts p-p |
| *Colour-killer Signal Output (d.c.)* | |
| For monochrome video input signals | –1·5 volts approx. |
| For colour-coded video input signals | –3 volts approx. |
| *Power Supplies* | +6, –6 volts (regulated) |

**General Description**

Fig. 1 is a block diagram of the UN18/505. The incoming video signal is applied to a chrominance band-pass filter and thence through a variable-gain amplifier to burst-gating and burst-blanking circuits.

Colour-bursts separated from the incoming video by the burst-gating amplifier are compared in phase with a locally-generated subcarrier signal to produce two varying d.c. outputs. One of these represents an error signal and acts to alter the phase of the local oscillator output as necessary (i.e. it completes an automatic phase-control loop[4]).

The second phase-comparator d.c. output is used to indicate when correct phase-locked conditions have been established. It is applied to the burst-blanking amplifier to disable this circuit in the presence of a monochrome input signal. This comparator output ultimately forms the colour-killer output signal mentioned previously.

A feed of band-limited chrominance signal passes through the burst-blanking amplifier (where the burst is removed) and thence to two synchronous detectors to be demodulated by means of separate reference subcarrier signals (which are in phase quadrature).

The two demodulator outputs are the I and Q signals. These are amplified and fed through low-pass filters before being applied to a matrix circuit to produce the colour-difference output signals R–Y and B–Y.

Note that an extra delay is included in the I-signal path to equalise signal-transit times.

**Circuit Description**

Fig. 2 shows the complete circuit diagram of the UN18/505.

*Input Circuit*

Video signals entering the unit are applied to a band-pass filter comprising L1, C1 and C2 which limits signals fed to the input amplifier to a bandwidth of 3·579545 ± 1·3 MHz (2-dB points) for the I-channel. TR1 is an emitter-follower which feeds the chrominance signal to a second emitter-follower TR2 from a variable tapping point on R77 (forming part of the emitter load of TR1). R77 is mounted on the unit front panel, and is labelled SAT (for saturation); the gain of the input amplifier can be varied by adjustment of R77 over a range of ±3 dB with respect to the gain at the normal setting. Two outputs from TR2 are used as shown below.

*Phase Comparators*

An output of chrominance signals from TR2 is applied to the base of TR3 which is also fed with 6-volt, positive-going back-porch (blanking) pulses. TR3 is biased so that only the subcarrier burst superimposed on each blanking pulse is effective in producing an output from the tuned secondary of collector load, L2. Neutralising capacitor C10 in this circuit

acts to reduce break-through of chrominance signals during the intervals between blanking pulses.

Subcarrier bursts from L2 are applied to two phase comparator circuits comprising D1, D2, and D3, D4. These circuits are also fed with a reference subcarrier signal derived from the local crystal-controlled generator via R80, emitter-follower TR4 and tuned transformer L3. The connections between L3 and the comparators are arranged so that the reference subcarrier feed to the circuit containing D1 and D2 is in phase quadrature with respect to the reference signal applied to D3 and D4.

Note that the phase of the reference signal from TR4 is variable (with respect to the oscillator output) because it is taken from a resistor, R80, connected across the phase-shift network which creates the necessary quadrature relationship between the two reference-subcarrier signal feeds to the synchronous demodulators (see *Synchronous Demodulators*). Ultimately, R80 provides adjustment of the basic burst-locked oscillator phase.

*Burst-locked Oscillator*

The output from D3 and D4 is filtered to remove subcarrier-signal components, and the resulting d.c. is a phase-error signal. This is applied as a correction signal to variable-capacitance diode D13 which forms a feedback path across the crystal-controlled oscillator TR20; thus, by automatically controlling the effective capacitance of D13, the oscillator is locked in frequency and phase to the incoming colour sub carrier.

A standing d.c. bias is also applied to D13 from variable resistor R81, which thereby provides a preset control of the oscillator phase; suitable adjustment of R81 also allows the comparator-circuit and capacitance-diode combination to be operated in the correct range.

A non-locking push button mounted on the front panel and marked APC MUTE allows the automatic phase-control circuit to be temporarily disabled by connecting the correction-signal path to the −6-volt rail.

The d.c. conditions of the oscillator are stabilised by TR19, which also passes the reference subcarrier output via voltage amplifier TR18 to the synchronous demodulators.

*Colour-killer Signal Generation*

Because of the 90-degree subcarrier-feed phase difference produced by L3 (mentioned previously), the filtered output voltage from D1 and D2, which is applied to the base of TR5, moves negatively when the reference subcarrier generator is locked to the incoming burst. Thus, TR5 and TR6 are biased into conduction, and the current drawn by TR6 under such conditions produces a 0-volt potential at the junction of R29 and R30. This voltage biases TR7 and TR8 into conduction (except during the burst period, see *Burst-blanking Amplifier*). One result of conduction through TR7 and TR8 is a change of potential at the junction of R11 and R32; this change represents the output colour-killer signal fed to another decoder unit[3].

*Burst-blanking Amplifier*

Common-base, push-pull amplifiers TR7 and TR8 form the balanced burst-blanking gate circuit, and are fed with the chrominance signal from TR2 via transformer L4. Positive-going, back-porch pulses of 4 μs duration are applied to the two bases through the balance-adjustment circuit of R78, C31 and C32, to bias-off the transistors during the burst period. Thus the output from the secondary of transformer L5 is the chrominance signal with burst removed.

R78, which also carries the d.c. colour-killer signal described above, is used to adjust the gate-circuit balance so as to reduce switching transients (as the transistors are switched off and on) to a minimum.

*Synchronous Demodulators*

The burst-blanked chrominance signal from L5 secondary is fed in parallel to two emitter-followers. TR17 and TR9, and thence to the balanced-bridge, synchronous demodulators for recovery of the I and Q components of the colour signal. Diodes D9 to D12, with transformers L10 and L11 form the I-signal demodulator; a similar circuit comprising D5 to D8, L6 and L7 produces the Q signal.

Each of the demodulator circuits is fed with reference subcarrier from TR18; top-capacity coupling via C49 creates the necessary 90-degree phase difference between these reference feeds. Tapped resistor R80 samples both phases, and thereby provides a variable-phase feed of reference subcarrier to the automatic phase-control comparator; thus, the phase of the reference signal can be adjusted so that, ultimately, the resulting colour-separation signals produce the required hue. R80 is mounted on the unit front panel and labelled *Hue*.

*Colour-difference Signal Output Circuits*

The Q-signal output from the synchronous demodulator is fed via TR10 to a low-pass filter (L8, C38, C39) which removes the subcarrier - frequency components and limits the residual signal to the required

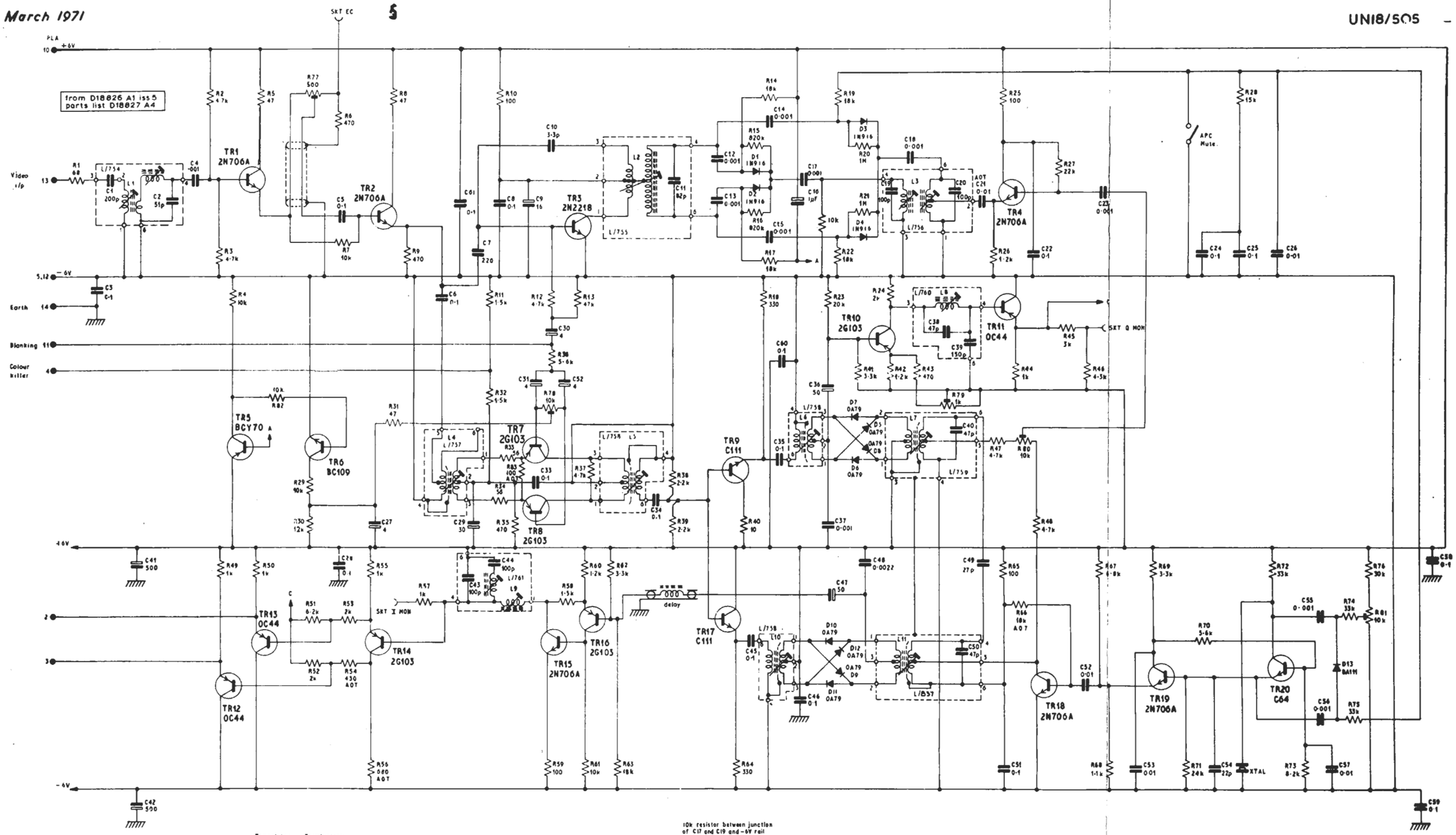




Fig. 2. Circuit of NTSC Colour-signal Decoder Chrominance Unit UNI8/505

Q-signal bandwidth. Emitter-follower TR11 feeds the filter output to a resistive matrix where it is combined with the I signal to produce the R–Y and B–Y colour-difference signals.

The demodulated I signal is also fed to a low-pass filter to remove subcarrier components; the signal-path here includes a delay line and a complementary feedback pair, TR15 and TR16. Note that the I-channel filter does not further reduce the signal bandwidth (which has already been sufficiently limited; see *Input Circuit*), and the delay is included to compensate for extra signal transit time through the narrower-band Q-channel filter. Thus, the two signals arrive at the matrix in time-coincidence.

Two outputs from the I-channel filter, the I signal and its inversion, are applied to the matrix through transistor TR14. The resulting colour-difference signals R–Y and B–Y are produced as outputs from the unit by identical emitter-followers TR12 and TR13.

**Alignment and Maintenance**

The UN18/505 is normally aligned and maintained as part of a complete decoder [1,2]

**References**

1. NTSC 525-line Colour-signal Decoder GE1/527
2. PAL/NTSC 625/525-line Colour-signal Decoder GE1/529
3. NTSC Filter and Delay Unit UN1/571.
4. *Design of Automatic Phase Control in NTSC-type Decoders;* D.D.T.M.8.163/(64).

**JN 12/70**

## MODIFIED NTSC COLOUR-SIGNAL DECODER CHROMINANCE UNIT UN18/505 (72)
### (Field-Store Standards Converter)

**Introduction**

The modified UN18/505 accepts a non-composite, band-limited colour-coded signal (i.e. chrominance) at a level of 0·89 volts p-p (for 100-percent colour bars). The outputs from the unit are two colour-difference signals (R–Y, B–Y) at a level of about 1·4 volts p-p.

Two subsidiary inputs are required by the unit. One of these is a train of positive-going, line-rate pulses which is used to operate a burst-blanking circuit. The other subsidiary input is a feed of reference subcarrier (from a burst-locked oscillator Type OS1/502A; key ref 109, address 1/5/3), which replaces a signal generated by the integral burst-locked oscillator operative in unmodified UN18/505 units.

The unit has been modified to form part of an N.T.S.C. decoder contained in the input section of a Field-store Standards Converter Type C06/506, and receives an N.T.S.C. chrominance signal from a 'comb' filter (actually from the Adder and Subtractor Unit; key ref 6, address 1/13/4). Colour-separation signals are ultimately produced from the unit R–Y and B–Y outputs (by a Luminance Unit Type UN19/503, key ref. 74), and these R, G and B components are then re-coded onto the 4·5 MHz Intermediate-signal subcarrier.

In the C06/506 equipment, the modified UN18/505 has the address 1/10/2 (see block diagram C).

**General Specification**

The specification given for the unmodified UN18/505 is applicable to the modified unit except in the following items.

| | |
|---|---|
| *Input Impedance* | High (but with external 75Ω term). |
| *Burst-blanking Pulse Input* (10·5 μs pulse in line-blanking interval) | 4 volts p-p (positive going) |
| *Colour-killer Signal Output* (d.c.) | No output. |

**Circuit Modifications**

Fig. 3 is a complete circuit diagram of the modified UN18/505. It should be compared with the circuit diagram of the normal unit given in Fig. 2.

*Input Circuit*

Non-composite chrominance signals from the comb filter are applied directly (via C4) to the input emitter follower, TR1. The band-pass filter required in the unmodified unit (to separate the chrominance-signal components) is unncesssary, and has been removed.

*Phase Comparators*

Neither of the phase-comparator d.c. outputs is used. Note, however, that a feed of 4 μs back-porch pulses remains as an input to the unit, even though it is not required.

*Burst-locked Oscillator*

This circuit is disabled in the modified unit. A feed of reference subcarrier is obtained from a separate unit (OS1/502) via pins 6 and 8 of the connector.

*Colour-killer Signal Generation*

There is no colour-killer signal output from the modified unit. In the C06/506, the NTSC decoder can only be fed with chrominance signals. Therefore, the junction of R29 and R30 is connected to chassis so that TR7 and TR8 are permanently biased into conduction (except during the line-blanking interval; see *Burst-blanking Amplifier*).

*Burst-blanking Amplifier*

Operation of the burst-blanking amplifier in the modified UN18/505 is similar to that described for the normal unit. The input and output transformers (L4 and L5) have, however, been changed to wide-band components. Further, the blanking pulses which effect the gating action are longer in duration, occupying nearly the whole of the line-blanking interval (i.e. each pulse is of about 10·5 μs duration, and timed to start 1 μs before the normal position of a line-sync pulse). These special blanking pulses are produced by a Blanking Generator Mk. 2 (key ref 12, at an address of 1/8/2).

The remainder of the circuit is identical in operation to the standard unit.

Note that the *Hue* control and APC MUTE pushbutton (both on the front panel) are inoperative because the reference subcarrier is supplied from an external generator.

In practice, a separate hue control is provided and takes the form of a switched delay unit (key ref.33) the delay value of which is variable in steps of 0·5 ns (i.e. an increment of delay equal to a phase change of about two-thirds of a degree at the subcarrier frequency of 3·58 MHz); the total delay available is 235 ns. This unit is interposed between the burst-locked oscillator and the modified UN18/505 chrominance unit; it has the address 1/5/5.

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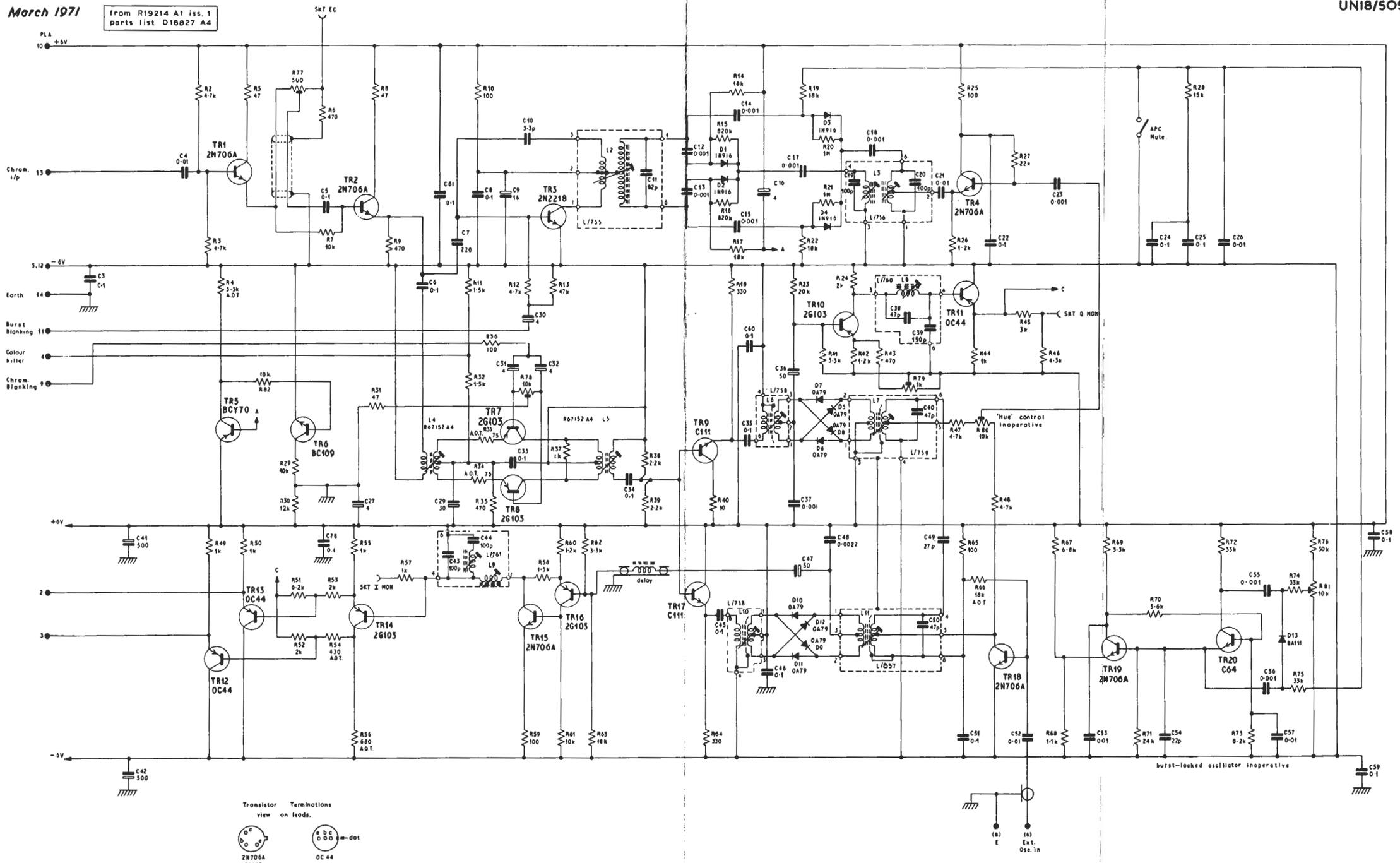


Transistor Terminations
view on leads.




2N706A
2G103
C64
C111
2N2218
BC109
BCY70

OC 44

UNI8/505/3T





*Fig. 3. Circuit of Modified NTSC Colour Decoder Chrominance Unit UNI8/505 (for F.S.S.C.)*