

A.F.R. SERVICE UNIT UN1/127

Introduction

The UN1/127 was designed as part of automatic fault reporter PA2M/7A, to facilitate on-site testing.

The unit is built on a printed wiring board which is mounted on a CH1/18C chassis with coding pins in positions 47 and 69.

Brief Specification

Generated Tone Frequency	1.5 kHz \pm 20 Hz
Power Supplies Required	+12 volts, 115 mA; -6 volts, 115 mA
Logic Potentials, with respect to earth	
Logic 0	equal to, or more negative than, -1.5 volts
Logic 1	equal to, or more positive than, -0.8 volt

Circuit Description (Fig. 1)

General

The circuit comprises three sections, a dialling monitor, a 30-minute and 10-second timer, and a 1.5-kHz tone generator. The 12-volt supply to the unit is controlled by switch SA.

Dialling Monitor

The dialling monitor comprises transistors TR1 to TR5 and an electromechanical decade counter. Normally, pin PLA10 is at earth potential, and PLA12 is at 12 volts positive. TR2 and TR3 are conducting, and TR1 and TR4 are cut off. When the associated PA2M/7A units initiate a dialling sequence an earth connection is made to pin PLA12; transistor TR1 then conducts and applies a d.c. bias to TR2. Dialling pulses are generated by the conduction and cut-off of a transistor in another unit¹; the collector of this transistor is connected to pin PLA 10 and hence to TR2. Transistors TR2, TR3 and TR4 are separate common-emitter amplifiers; a coil in the decade counter forms part of the collector load of transistor TR4. The counter registers the number of pulses in each dialling operation and hence the digits of the number being called. In order to register each digit separately the counter must be reset after each train of pulses. This is done by operating a *Reset* button, SB, which applies an 18.5-volt r.m.s. 50-Hz a.c. supply to the base of TR5 and hence to terminals U and S of the counter.

30-minute and 10-second Timer

The purpose of this section is to render the PA2M/7A unresponsive to incoming ringing signals or to changes of state in the monitored apparatus. The muting lasts for 30 minutes after which there is a 10-second audible burst of tone.

Unijunction transistors (u.j.t.s) TR9 and TR11 are

used in separate timing circuits. The u.j.t. is normally cut off until its emitter potential is raised above its base-1 potential. In the circuit of TR9, the components C10 and R43 control the timing. When capacitor C10 is charged sufficiently TR9 conducts and C10 is discharged; the cycle then repeats.

In the simple circuit arrangement employed there is a limit on the maximum value of timing resistor, R43, that can be used. A peak-point current* of at least two μ A must be maintained to ensure that the u.j.t. operates correctly, and this limits the maximum value of R43 to about nine megohms ($18V/2\mu A$), which is not enough to provide the required 30-minute timing interval.

One way of overcoming this problem is momentarily to reduce the potential at base-2 of the u.j.t., so that the peak-point voltage* is reduced and hence the u.j.t. is triggered into conduction. Such a method is used to make TR11 timing circuit operate. Timing resistor R38 has a value of 150 megohms. A train of negative-going pulses is derived from TR9, through components C9 and R67, and applied to base-2 of TR11. When capacitor C8 has charged sufficiently and the base-2 potential is reduced, TR11 conducts and C10 is discharged. This occurs after about 30 minutes. Resistor R67 gives a fine control of the timed period.

The action of the circuit is as follows:

(a) In the quiescent, mute off, state:

The Q output of each bistable circuit, IC1, is at logic level 0. Transistors TR6, TR9, TR10, TR12 and TR13 are cut off. Transistors TR7 and TR8 are conducting. Transistor TR11 is switching on and off at a frequency of about 2 Hz.

(b) The mute circuit is started by operating *Mute Start* switch SC.

(1) A logic 0 pulse is applied to the C_d terminals, pin 13, of IC1. A logic 0 signal is applied to the S_d terminals, pin 10, which sets the Q output, pin 8, of the first stage of IC1 to logic level 1. Capacitor C8 is discharged through components D9, R39, R21 and switch SC.

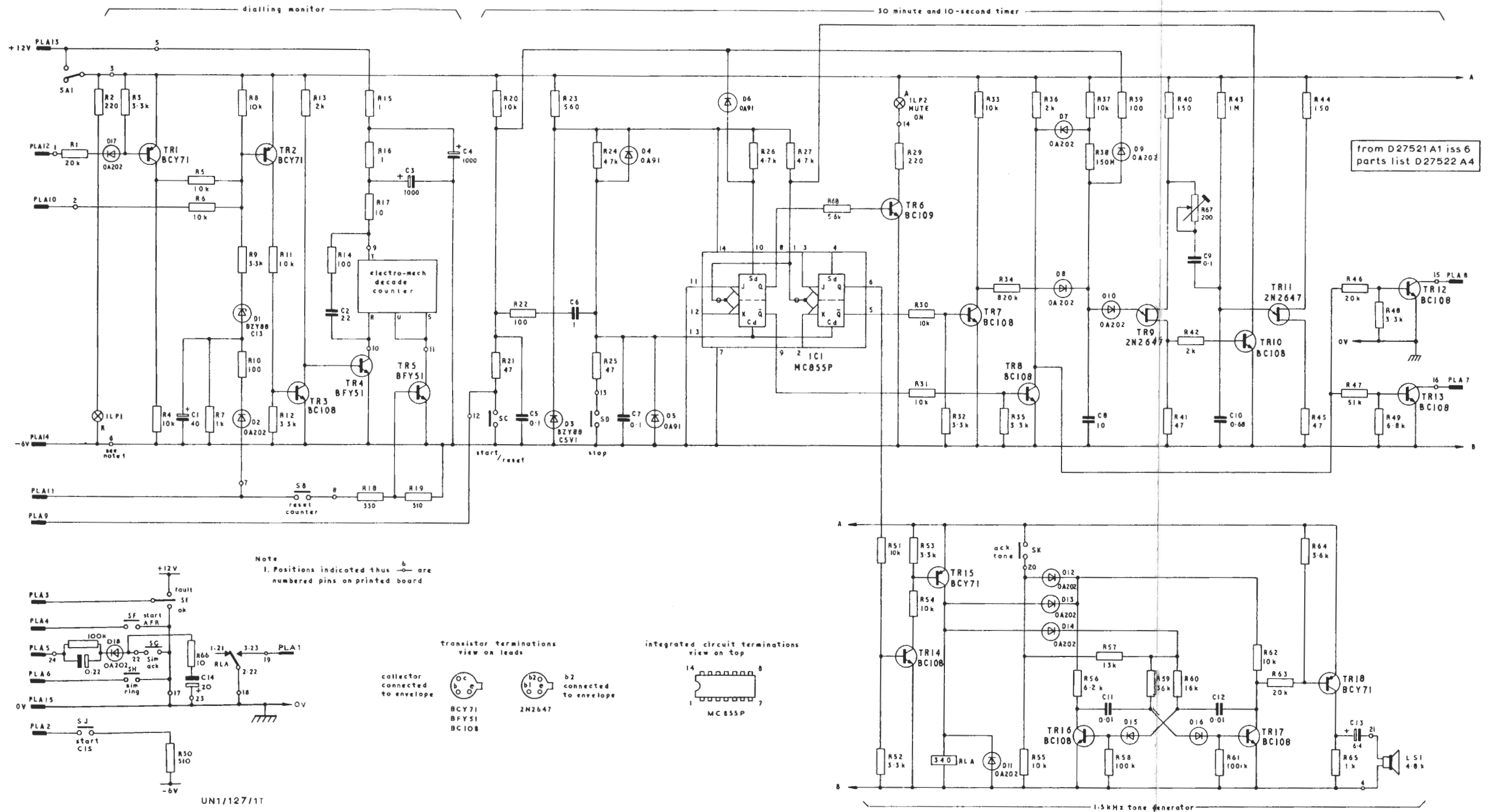
(2) Transistor TR6 is switched on and a *Mute On* lamp, ILP2, lights. Transistor TR8 is cut off, diode D7 is reverse-biased and capacitor C8 begins to charge through resistor R38. Transistors TR12 and TR13 are switched on.

(c) After about 30 minutes, a positive-going pulse appears across resistor R41, which causes transistor TR10 to conduct. The pulse at the collector of TR10 is used to clock bistable circuit IC1.

(1) The *Mute On* lamp is switched off. Diode D7 is forward-biased and transistors TR12 and TR13 are cut off. The Q output of the second stage of IC1, pin 6, goes to logic level 1 and starts the tone generator. Transistor TR7 is cut off. Capacitor C8 is charged through components D8, R34 and R33.

(2) After about 10 seconds, the capacitor is discharged through u.j.t. TR9. A negative-going pulse occurs at the collector of

* The Unijunction Transistor, O. Greiter: *Wireless World*, July and August 1970.



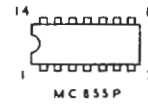
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Note 1. Positions indicated thus **b** are numbered pins on printed board

transistor terminations view on leads

integrated circuit terminations view on top

collector connected to envelope



UNI/127/11

Fig. 1. Circuit of UNI/127

transistor TR10 which clocks bistable circuit IC1. Both stages of IC1 change state, pin 6 goes to logic level 0 and the tone generator is switched off. Pin 5 goes to logic level 1 and switches on transistor TR7.

The circuit has now returned to its quiescent state.

The muting action can be cancelled at any time by operating *Mute Stop* pushbutton switch, SD. This puts a logic 0 signal on the C_d input, pin 13, of circuit IC1.

1.5-kHz Tone Generator

Transistors TR16 and TR17 form a conventional astable multivibrator the output of which feeds a common-emitter amplifier TR18. The collector load for TR18 is a telephone earpiece which is fixed to the front panel of the unit.

The oscillator can be switched on manually by operating *Tone* pushbutton switch SK. In this condition the output frequency is 1.5 kHz.

The 10-second alarm operation is achieved by putting a logic 1 signal on the base of transistor TR14. This causes transistor TR15 to saturate and forward-biases diodes D13 and D14. Resistors R59

and R60 are connected to the positive supply rail through TR18. Resistor R57 is not used in this mode and consequently the frequency of the output tone is increased.

Relay RLA is energised when transistor TR15 is on. The relay contacts can be used to give an external alarm.

Simulate Function Switches

Five other pushbutton switches are mounted on the front panel of the unit to enable d.c. signals to be sent to associated units to simulate required conditions. These are:

Fault/O.K. condition	– switch SE
Start A.F.R.	– switch SF
Simulate acknowledgement	– switch SG
Simulate ring	– switch SH
Start C.I.S.	– switch SJ

Test Procedure

The UN1/127 is tested as part of its parent unit.

References to Typical Associated Equipment

1. Peripheral Control Unit UN3/13A.

LPB7/72