FLYWHEEL SYNCHRONISING PULSE REGENERATOR UN1/506 AND UN1/506A

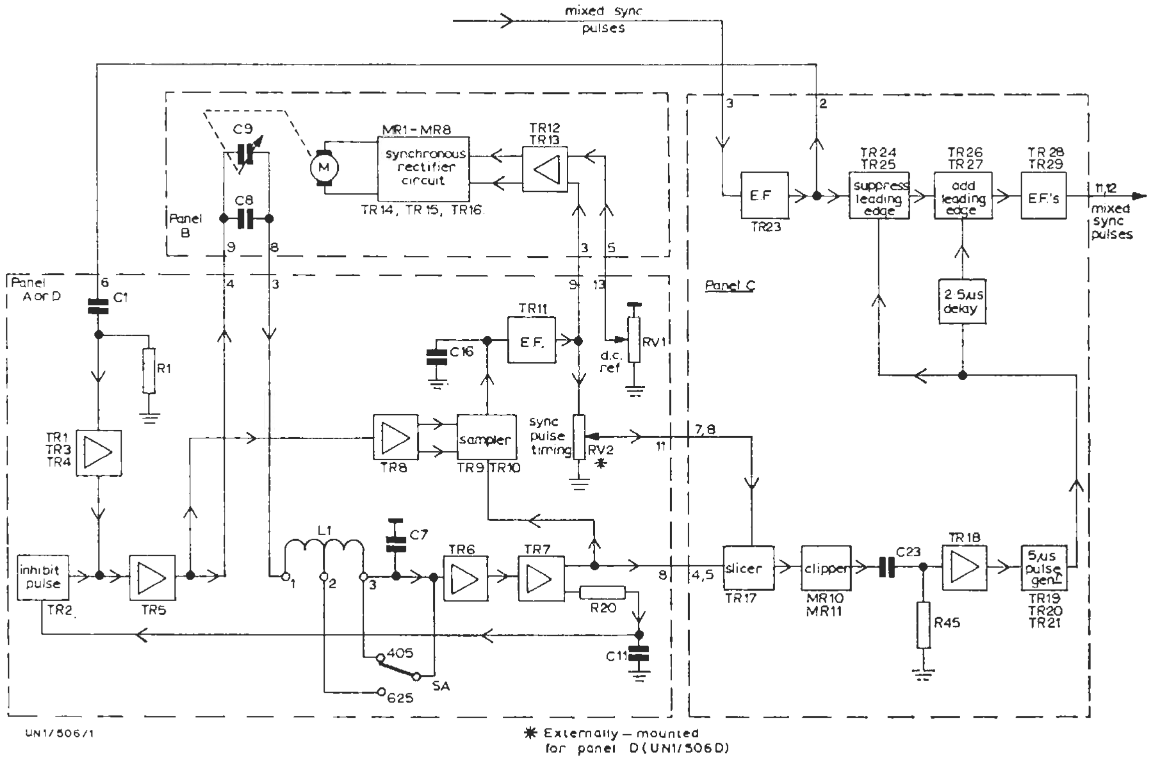

Fig. 1 Block Diagram of Flywheel Synchronising Pulse Regenerator UN1/506

Introduction

The UN1/506 accepts an input of 405-line or 625-line mixed synchronising pulses at an amplitude of 2·0 volts p-p. It produces an output of the same level and with similar waveform but with the timing of the line-frequency pulse leading edges adjusted by the action of a flywheel circuit. The half-line pulses present during the field-blanking period, and positioned between the line-frequency pulses, are not affected by the flywheel action.

The UN1/506 comprises three modules designated panel A, panel B and panel C, each mounted on a CH1/12A chassis.

Panel A contains a limiting amplifier and a tuned (ringing) circuit, which produces the flywheel action, a sampling circuit and a gating transistor for removing the half-line pulses.

Panel B contains a servo-motor and its associated amplifier, together with a motor-controlled variable capacitor which forms part of the ringing circuit in panel A.

Panel C contains a slicing and squaring circuit, two pulse-gating circuits and a pulse generator. These are employed to suppress the leading edge of each original line-sync pulse and replace it with a regenerated leading edge the timing of which has been adjusted by the action of the ringing circuit.

A modified version, the UN1/506A, comprises panels B and C as described above and a module known as panel D which is electrically identical to panel A. However, a variable resistor which is mounted on the panel-A escutcheon plate (RV2, the *Sync Pulse Timing* control) is a separate item in the panel-D version of the module and can be located at some convenient remote point.

The UN1/506 or UN1/506A modules are normally plugged into a PN3/23 chassis together with a power supplier type PS2/503A, a mixer unit type UN1/509 and an AM5/505 or AM5/505A 15-dB video amplifier.

The index-peg positions for the three modules comprising the UN1/506 (or UN1/506A) are as follows.

Panel A (or D)	1 and 2
Panel B	3 and 30
Panel C	3 and 28

General Specification

Signal input

Mixed sync pulses	2 volts p-p

Signal output

Mixed sync pulses (with regenerated line-sync-pulse leading edges)	2 volts p-p

Impedances

Signal input	about 5 kilohms
Signal output	75 ohms

Sync-pulse timing control

Maximum operational range of RV2	±2·5 μs

Power supplies

−12 volts (stabilised) about 60 mA.
250 volts, 50 Hz 50 mA.

Circuit Description

Fig. 1 is a block diagram which shows the main parts of the three modules and gives details of their interconnection.

Panel A

The circuit of panel A is shown in Fig. 2 with drawings of signal waveforms at various points in the module.

Negative-going mixed sync pulses enter panel A via an emitter-follower contained in panel C. The pulses are differentiated by C1 and R1, but only the spikes coincident with the leading edges of the original line-sync pulses are transferred by TR1 to the limiter-amplifier comprising TR3 and TR4. TR5 supplies line-frequency pulses of almost constant amplitude to the ringing circuit L1, C8 and C9. This produces a sine-wave signal whose frequency is the average of the pulse repetition-rate exhibited by the incoming line-sync pulses. Because the tuned circuit has a high Q-factor, the output sine wave cannot vary rapidly in either phase or frequency. Thus the circuit acts as an electrical flywheel.

In practice, the two capacitors which form part of the tuned circuit (C8 and C9) are contained in Panel B. C9 is a variable capacitor and it is adjusted by a servo motor to control the resonance frequency of the tuned circuit. The motor is controlled by error signals developed elsewhere in the equipment.

The facility for operating the UN1/506 (or UN1/506A) on either 405/50 or 625/50 television standards is provided by a switch, SA in Fig. 2, which is mounted on the escutcheon plate of Panel A and marked *405—625*. The switch enables either the whole or only a part of inductor L1 to be included in the tuned circuit thus altering the resonance frequency for 405-line or 625-line operation respectively.

The signal from the ringing circuit is taken from across capacitor C7 which produces a phase shift such that the region of maximum slope of the sine-wave signal fed to amplifiers TR6 and TR7 occurs in approximate coincidence with the leading edge of the incoming line-sync pulses. The output from TR7 emitter is fed to a slicing circuit, contained in panel C, and also to the common-collector connection of the sampler-circuit transistors TR9 and TR10.

Line-frequency pulses are taken from TR5 to a phase-splitting stage TR8 which produces the coincident positive-going and negative-going pulses used to drive TR9 and TR10 into conduction. During each period of conduction, C16 charges through TR9 and TR10 so that the potential across the capacitor becomes the same as that at the emitter of TR7. When TR9 and TR10 are cut off, C16 discharges slowly into the base of TR11. The varying d.c. from this transistor represents an error signal which describes, in magnitude and direction, the phase shift created in the sine-wave output of the ringing circuit by a change in frequency of the pulse input. The variable resistor RV2 is used to feed a proportion of the error signal to the slicing circuit in panel C.

A third output from TR7 is developed across capacitor C11 which, in conjunction with resistor R20, produces a phase shift. This sine-wave signal is then fed to the base of TR2 (in the collector circuit of TR1) so that TR2 varies between cut-off and full conduction. The phase shifts caused by C7 and C11 ensure that full conduction of TR2 occurs between line-sync pulses, and therefore inhibits any output from TR1 during this period. Thus, the half-line pulses present in the incoming mixed sync pulse signal during the field-blanking interval are prevented from affecting the tuned circuit.

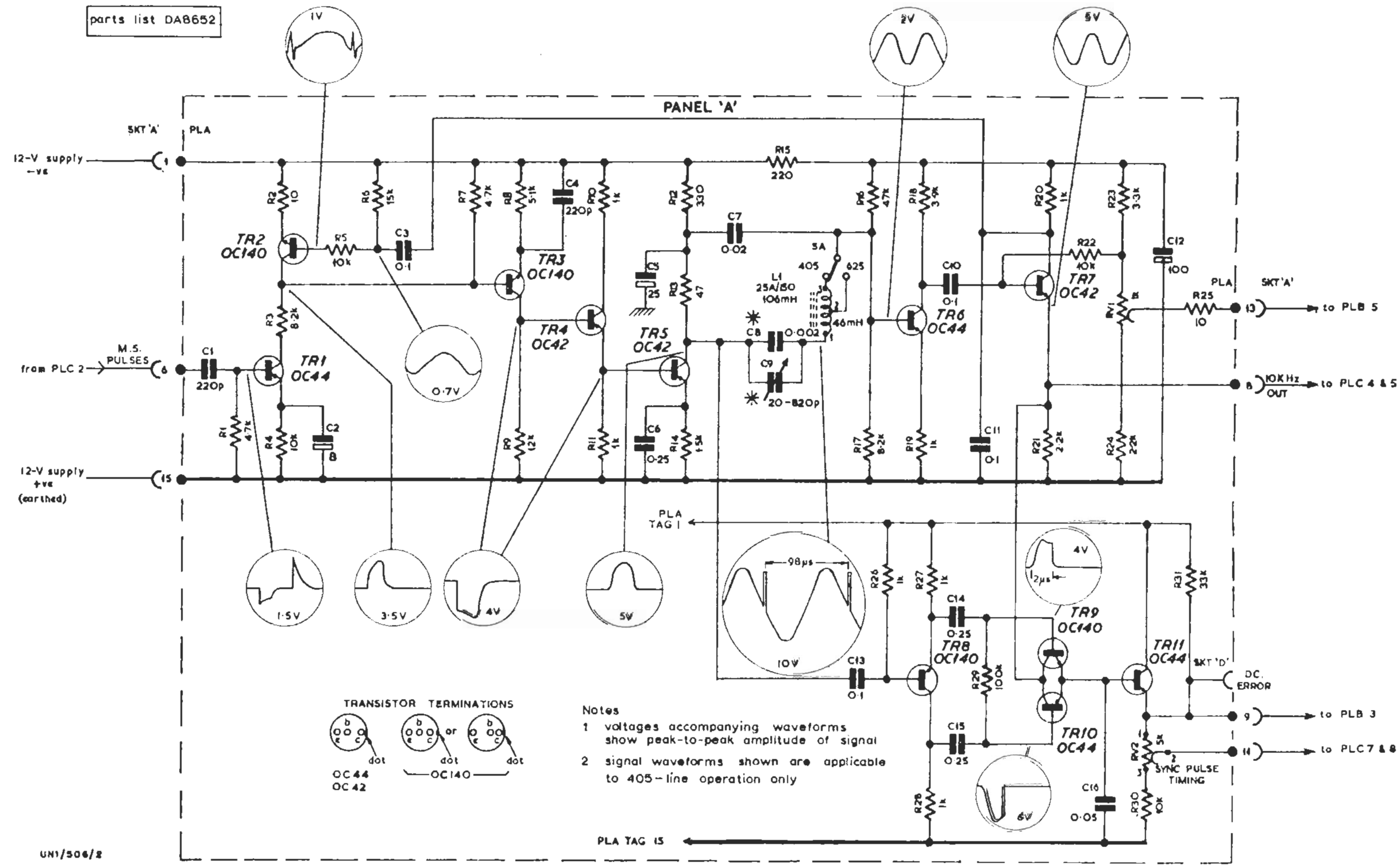

Fig. 2 Circuit of Panel A

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UN1/506

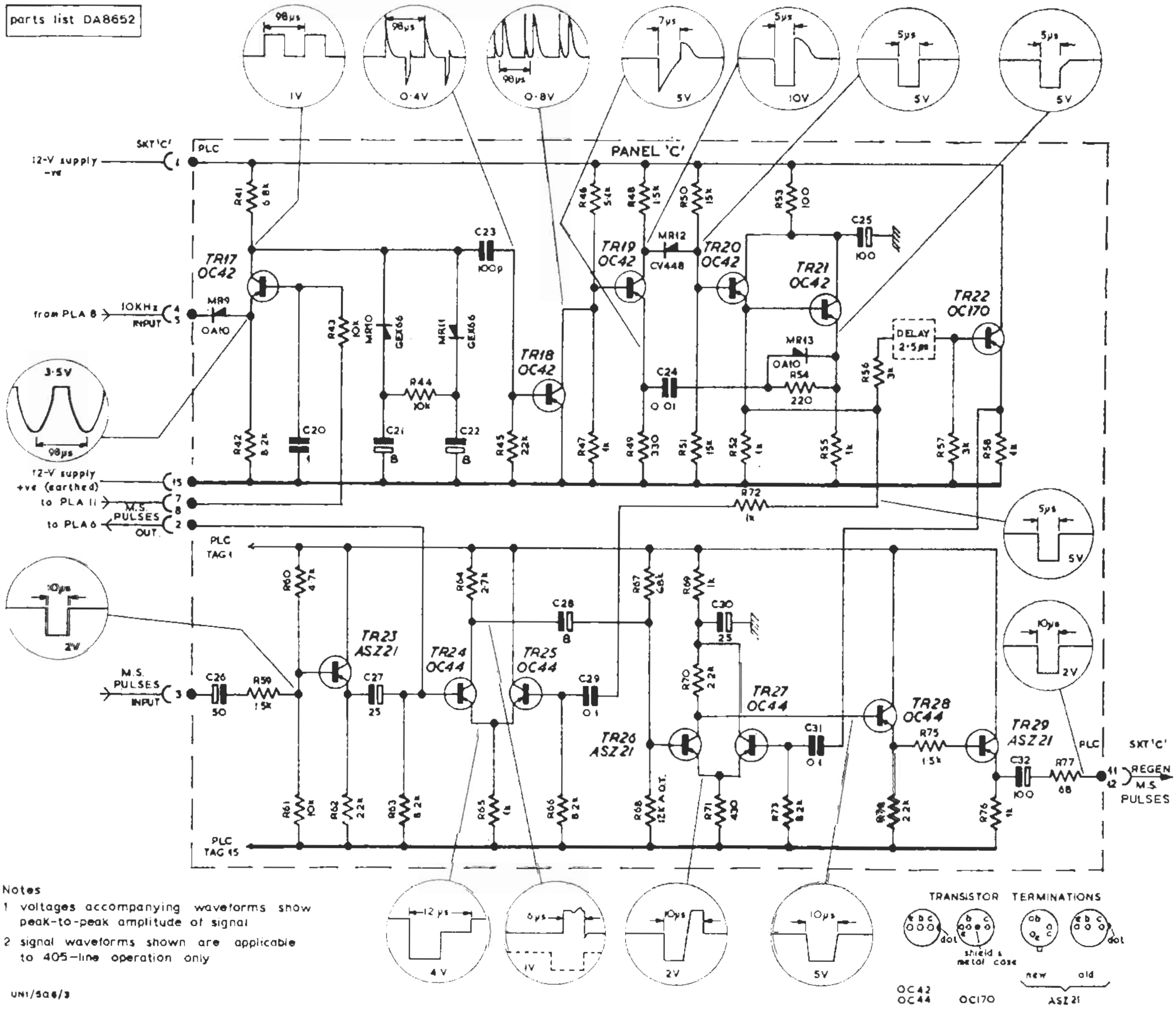

Fig. 3 Circuit of Panel C

Panel C

The circuit of panel C is shown in Fig. 3. The line-frequency sine-wave signal from TR7 is sliced by MR9; the actual slicing potential is determined by TR17 and, ultimately, by the d.c. error signal from RV2. MR10 and MR11 limit the sliced sine-wave signal and the resultant rectangular-waveform signal is differentiated and applied through TR18 to the monostable multivibrator comprising TR19, TR20 and TR21. This circuit is triggered by positive-going spikes from TR18 which are coincident with the negative-going edges of the rectangular waveform signal fed to the differentiator. The output from the emitter of TR20 consists of a train of negative-going 5-μs line-frequency pulses, the timing of which depends ultimately on the value of the d.c. error signal fed to the slicing circuit.

Mixed sync pulses are fed from the input emitter-follower TR23 to an amplifying stage TR24. Part of the load of this transistor is in its emitter circuit and is shared by an emitter-follower TR25. The 5-μs pulses produced by the multivibrator described above are applied to the base of TR25 so that, for the duration of each of these pulses, TR24 is cut off. In practice the 5-μs pulses are timed to begin 2·5 μs before, and to end 2·5 μs after, the leading edges of the line-sync pulses feeding TR24. Thus the output from TR24 collector consists of positive-going line-sync pulses having the first 2·5 μs (about) suppressed by the inhibiting action of the multivibrator pulses.

The circuit comprising TR26 and TR27 is similar to that of TR24 and TR25. The negative-going 5-μs pulses from the multivibrator are fed via a 2·5 μs delay line and an emitter-follower TR22 to the base of TR27 which therefore conducts, cutting off TR26. The positive-going (line-frequency) pulse from TR24, which occurs before the end of the delayed multivibrator pulse, maintains TR26 in the non-conducting state. Thus the signal at the collector of TR26 consists of negative-going mixed-sync pulses, the line-frequency component of which has leading edges re-timed by the action of the ringing circuit. Emitter-followers TR28, TR29 and resistor R77 supply mixed-sync pulses to the external circuit from a source impedance of 75 ohms.

Note that full rotation of the *Sync Pulse Timing* control (i.e. the largest range of manual control of the error signal from RV2) results in a total timing variation of the 5-μs pulses, both delayed and undelayed, of about ±5 μs. However, the maximum range used in practice must be limited to ±2·5 μs otherwise the original line-sync pulse leading edges are not suppressed and this results in a double line-sync pulse.

The action of the line-sync pulse reconstitution circuit described above provides fast-acting automatic adjustment to compensate for small changes in mean frequency of the incoming sync pulses.

Panel B

The circuit of panel B is shown in Fig. 4. TR12 and TR13 are connected as a long-tailed pair. The d.c. error signal from TR7 (panel A or D) is fed to the base of TR12, and a reference voltage (from a variable potential-divider circuit contained also in panel A) is applied to the base of TR13. Any difference in the potential existing at the collectors of TR12 and TR13 causes conduction in either of the complementary transistors TR15 or TR16.

Two diode-bridge circuits, MR1 - MR4 and MR5 - MR8, are associated with the series-aiding secondary windings of the mains-fed transformer T1. One of the secondary windings feeds also a small motor which is connected in series with the diode bridge. This motor is mechanically coupled to the variable capacitor C9 which forms part of the ringing circuit in panel A. The emitter-collector path of transistor TR16 is connected across the bridge which is in series with the motor; the base of TR16 is connected to a point in the other bridge circuit.

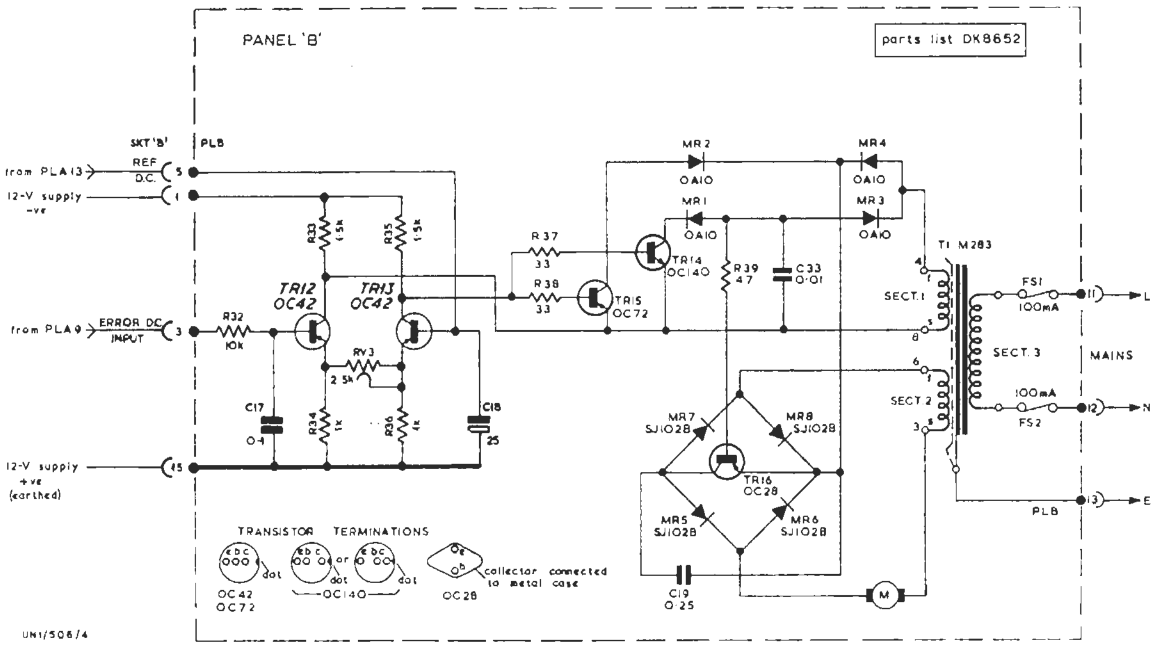

Fig. 4 Circuit of Panel B

When TR14 is conducting, complementary transistor TR16 is driven into conduction during each half-cycle (of the 50-Hz input to T1) that terminal 4 of secondary winding 1 is positive with respect to terminal 8. During the same period, terminal 6 (of secondary winding 2) is positive with respect to terminal 3 and thus (conventional) current will flow through the motor via MR8, TR16 and MR5 (from left to right in Fig. 4).

Conversely, when TR15 is conducting, TR16 conducts during the half-cycle that terminal 8 is positive with respect to terminal 4 and so current flows from terminal 3 through the motor (in the reverse sense to that described previously) via the bridge and TR16 to terminal 6. The motor is geared down and arranged to adjust the value of C9 so that it counteracts the error which originally caused the difference of potential between the collectors of TR12 and TR13. In practice, the reference potential applied to TR13 is adjusted (by RV1 on panel A or D) so that the 5-μs pulses produced by the multivibrator in panel C are disposed symmetrically about the mean position of the leading edges of the incoming line-sync pulses.

The action of the servo-motor control circuit provides slow-acting, automatic adjustment to compensate for large changes in the mean frequency of the incoming line-sync pulses.

Alignment

Test apparatus required

Dual-trace oscilloscope (such as Tektronix Type 535 with type CA plug-in unit)
Chassis extender type CH1/12.

Procedure

1. Apply an input of mixed sync pulses at normal level (2 volts p-p). Use the oscilloscope to inspect the incoming sync-pulse signal at pin 6 of socket A (panel A or D) and check for correct waveform and level.
2. On panel B, rotate the motor shaft (manually) so that the coupled variable capacitor C9 is in the middle of its range of movement.
   On panel A (or D), connect the oscilloscope to the high-impedance point of the tuned circuit (junction of L1 and C9; tag 1 of L1 provides a suitable connection).
   Adjust RV1 (reference potential) until the signal waveform displayed on the oscilloscope corresponds to that shown by the larger-scale drawing marked X in Fig. 2.
3. On panel C, connect oscilloscope channel A to the base of TR23 (input mixed-sync pulse signal). Connect channel B to the emitter of TR29 (output mixed-sync signal).
   Adjust the oscilloscope time-base controls to obtain two locked traces, each of a single line-sync pulse.
   On panel A adjust RV2 (*Sync Pulse Timing*) so that the two pulses are coincident. (On panel D RV2 is located at some point remote from the UN1/506A modules).

Note: The timing of the output line-sync pulses can be altered by further adjustment of RV2 if this is required for operational use. The maximum permissible variation is $\pm 2{\cdot}5$ μs relative to the mean timing of the incoming line-sync pulses.

4. Disconnect the incoming sync-pulse feed.
   On panel B, rotate the motor shaft (manually) so that the variable capacitor is at one end of its range of movement (either fully closed or fully open). Reconnect the sync-pulse feed. Observe the movement of the motor-driven capacitor, as the correct operating conditions are established, and adjust RV3 (on panel B) so that the variable capacitor takes up the required position with barely perceptible overshoot.

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