SECTION 31

LINE PHASE DISCRIMINATORS UN1/531 AND UN1/519

Introduction

Line Phase Discriminators UN1/531 and UN1/519 accept a picture-frequency pulse-input, line-frequency ramp and pulse inputs and three d.c. inputs; they produce a sine-wave output signal with a controlled nominal frequency at twice line frequency.

While the picture-frequency pulses are present the frequency of the twice-line-frequency oscillator is controlled by a circuit in which the line-frequency pulses sample the line-frequency ramp waveform. If the picture-frequency pulses are not present the sampling circuit is inhibited by one d.c. input and a second d.c. input provides the oscillator frequency-control voltage. The third d.c. input operates a relay which transfers the frequency control to a fixed voltage.

The UN1/531 is a dual-standard version of the 405-line standard UN1/519 (see Part 1, Section 19). The Discriminators are constructed on CH1/12A chassis with index peg positions 7 and 14.

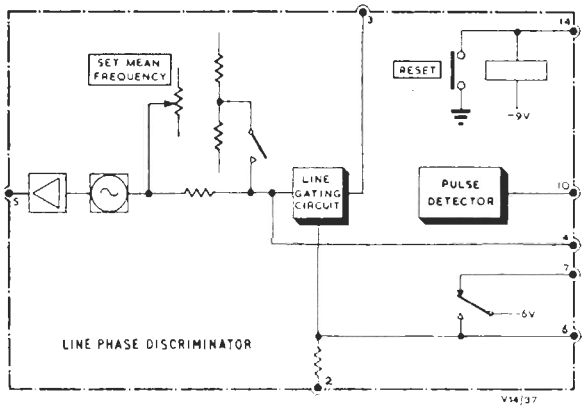

Fig. 31.1 Block Diagram of a Line Phase Discriminator

General Description

A block diagram of a Line Phase Discriminator is shown in Fig. 31.1. It contains a reactance-controlled twice-line-frequency oscillator for which a control voltage is obtained from two sources:

(a) the *Set Mean Frequency* control RV2.
(b) one of the following;
the output of a line sampling circuit,
the output of an external sampling circuit or
a fixed voltage (via the relay contacts).

When used for picture-source synchronising (see Instruction V.1, Original Method of Slavelock) the line-sampling circuit is fed with a line-frequency ramp waveform from a slaved sync separator and with a line-frequency pulse waveform from a reference sync separator. This line-sampling circuit is inhibited either by a d.c. input or by the operation of a relay in a pulse-detector circuit similar to that described in the UN1/542. The pulse-detector is fed with picture-frequency pulses if picture phasing is complete; the pulses cause a relay to be released which feeds an inhibiting potential to the external picture-sampling and mains-sampling circuits.

In the absence of a slaved input signal to the Picture Synchroniser the third d.c. input operates a second relay which transfers the control of the oscillator from the outputs of the sampling circuits to a fixed voltage. This relay may be operated also by means of a *Reset* button SA.

Circuit Description

The circuit of the UN1/531 is given in Fig. 31.2. The pulse-detector circuit includes transistors TR1 to TR3.

The line-frequency ramp waveform is fed via complementary emitter followers TR9 and TR10 to the emitter of the sampling transistor TR4. The base of transistor TR4 is fed with line-frequency sampling pulses. These pulses are short-circuited to the −6 volt supply rail via a relay contact if there is no input to the pulse detector circuit. The relay contact also feeds −6 volts to pin 6 to inhibit the external sampling circuits.

The sampled waveform fed to transistor TR4 is made up of the line-frequency ramp waveform and a d.c. component obtained from the variable resistor RV1. In steady-state operation, the oscillator frequency controlling the frequency of the ramp waveform is the same as that of the sampling pulses. A change in the d.c. component causes a change in the output voltage of the sampling transistor which in turn causes a change in the oscillator frequency. This advances or retards the ramp waveform relative to the sampling pulses until a new steady-state condition is achieved; in this the frequency of the oscillator and the output voltage of the sampling transistor are the same as in the previous steady-state condition. The change in the d.c. component

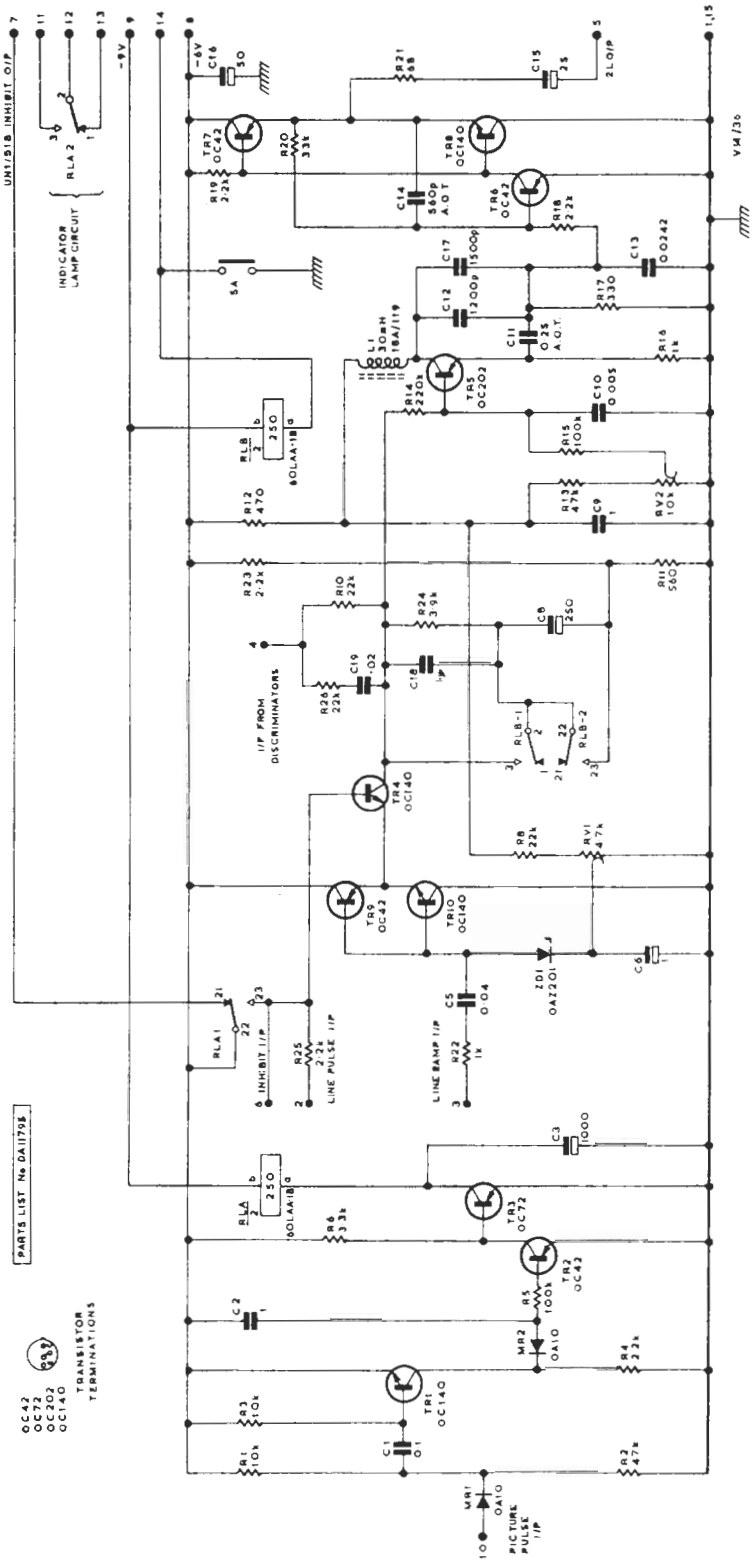

Fig. 31.2 Circuit of the UNI/531

is related to the timing of the slaved input by the slope of the sampled edge of the ramp waveform.

Transistor TR5 is part of a combined Colpitts oscillator and variable reactance stage. This latter function is achieved by shunting capacitor C13 with a resistor. This introduces into the collector current a quadrature component whose magnitude is controlled by the mutual conductance of the transistor. This is controlled by varying the base current. The mean frequency of the oscillator is set by means of the variable resistor RV2.

The output of the oscillator is fed via a negative-feedback amplifier, the feedback of which increases with frequency. The feedback reduces the output impedance of the amplifier and, because of the increase with frequency, it also reduces the harmonic content of the output.

Test Schedule

When testing Line Phase Discriminators, a Picture Synchroniser (described in Section 28) may be used as a test jig and source of power.

Apparatus Required

Electronic frequency meter J. Langham Thompson Type 6010/7.
Tektronix oscilloscope Type 515.
Two 10-kilohm ½-watt resistors.
75-ohm ½-watt resistor.
Selection of capacitors in the ranges:
100 - 1000 pF
0·05 - 0·25 μF

Test Procedure

A change of line-standard on the UN1/531 is achieved by reversing plug-in cards and this unit should be tested on both line-standards. Where the test figures vary; (A) refers to the UN1/531 on the 625-line standard, (B) refers to the UN1/531 on the 405-line standard and (C) refers to the UN1/519.

1. Connect pin 6 to pin 8.
   Connect one 10-kilohm resistor between pins 1 and 4 and the other 10-kilohm resistor between pins 4 and 8.
   Short circuit capacitor C8.
   Connect the frequency meter to the *Ext M.O. to P.G.* plug on the Picture Synchroniser.
   Plug in the Line Phase Discriminator using an extender board and switch on.
2. Adjust: (A) RV2B so that the output frequency is 31,250 ± 10 Hz.
   (B) RV2A so that the output frequency is 20,250 ± 10 Hz.
   (C) RV2 so that the output frequency is 20,250 ± 10 Hz.
   If the frequency lies outside the range of the variable resistor change capacitor:
   (A) C17 (B) C12A (C) C17
   Decreasing the value of the capacitor increases the frequency.
3. Short circuit pins 1 and 4. The output frequency should drop by:
   (A) 100 to 150 Hz.
   (B and C) 70 to 100 Hz.
   If the change of frequency is outside these limits change capacitor:
   (A) C11B (B) C11A (C) C11
   and readjust the *Set Mean Frequency* control. Decreasing the value of the capacitor increases the change in frequency.
   Remove the short circuit from between pins 1 and 4.
4. Measure the output signal on the oscilloscope. Its amplitude should be 0·8 to 1·5 volts p-p.
   If the amplitude lies outside these limits change capacitor C14. Decreasing the value of the capacitor increases the output amplitude.
   Remove the connections made in step 1.

Further Information

Typical voltages at transistor terminals are given below. Connect pins 6 and 8, short circuit the *Reset* switch and make the measurements with an Avometer Model 8.

Transistor	*Emitter*	*Base*	*Collector*
TR1	−6·4	−6·4	0
TR2	0	0	−0·25
TR3	0	−0·25	−0·1
TR4	−1	−6·3	−1·3
TR5	−0·25	−0·3	−6·3
TR6	0	−0·2	−3
TR7	−3	−3	−6·4
TR8	−3	−3	0
TR9	−1	−1	−6·4
TR10	−1	−1	0