

SECTION 23

SYNC PULSE SEPARATOR UNIT UN1/523

Introduction

The UN1/523 provides a 2-volt output of separated sync pulses from a 1-volt p-p video input signal (see also Sync Pulse Separation and Monitor Panels PA1/513 and PA1/520, Instruction V.13). The unit operates, without adjustment, on 405, 525 and 625-line monochrome signals and also on 625-line N.T.S.C. colour signals. It can be used for 525-line colour signals by energising an internal relay.

The unit is constructed on a CH1/12A chassis with index-peg positions 3 and 7. Input and output monitor sockets are provided on the front panel. Power supplies at +12 volts and -6 volts are obtained from a PS2/20 stabilised Power Supplier (Instruction G.2). A 50-volt supply, for relay operation, is also required.

General Specification

Input	1 volt p-p \pm 6 dB
Output	2 volts p-p \pm 1 dB
Input Impedance	6 kilohms (approx)
Output Impedance	75 ohms

Output-signal Rise-time	less than 0.2 μ s
Output-signal Pulse Duration	as for input \pm 0.2 μ s
Delay Through Unit	0.2 μ s \pm 0.05 μ s
Field Tilt	less than 2 per cent
50-Hz Rejection	less than 300 mV p-p at input is not discernible at output
Relay Supply (for 525-line colour)	50 volts d.c. at 16 mA
Power Inputs	12 volts \pm 4% (75 mA) 6 volts \pm 4% (15 mA)
Weight	1 lb.

Circuit Description

A block diagram, which shows the waveforms at various points in the programme chain, is shown in Fig. 23.1 and a circuit diagram in Fig. 23.2.

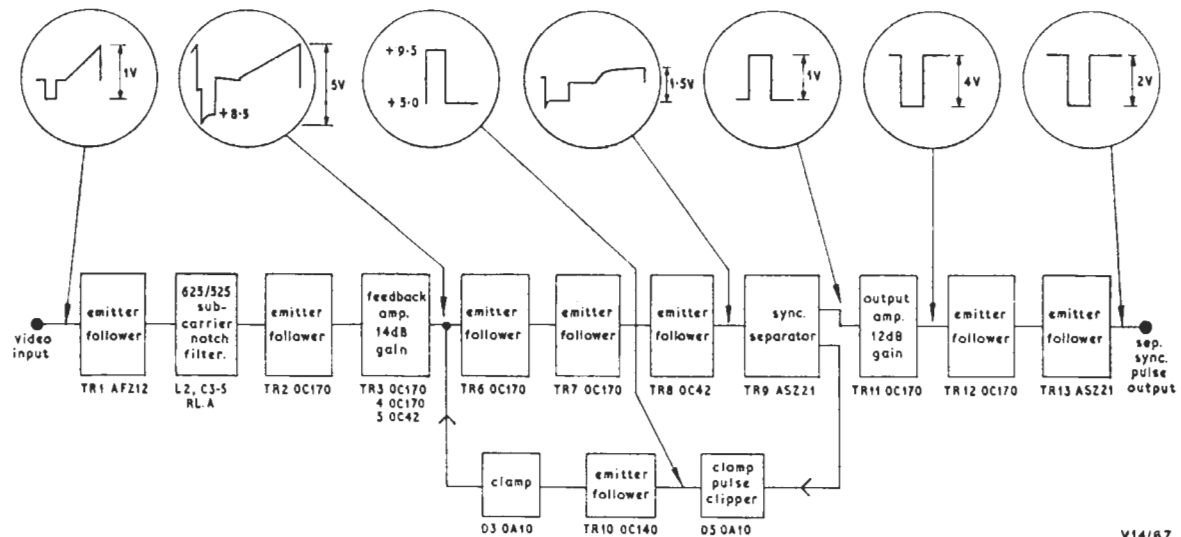


Fig. 23.1 Block Diagram of the UN1/523

Instruction V.14
Part 1, Section 23

parts list DA 11337

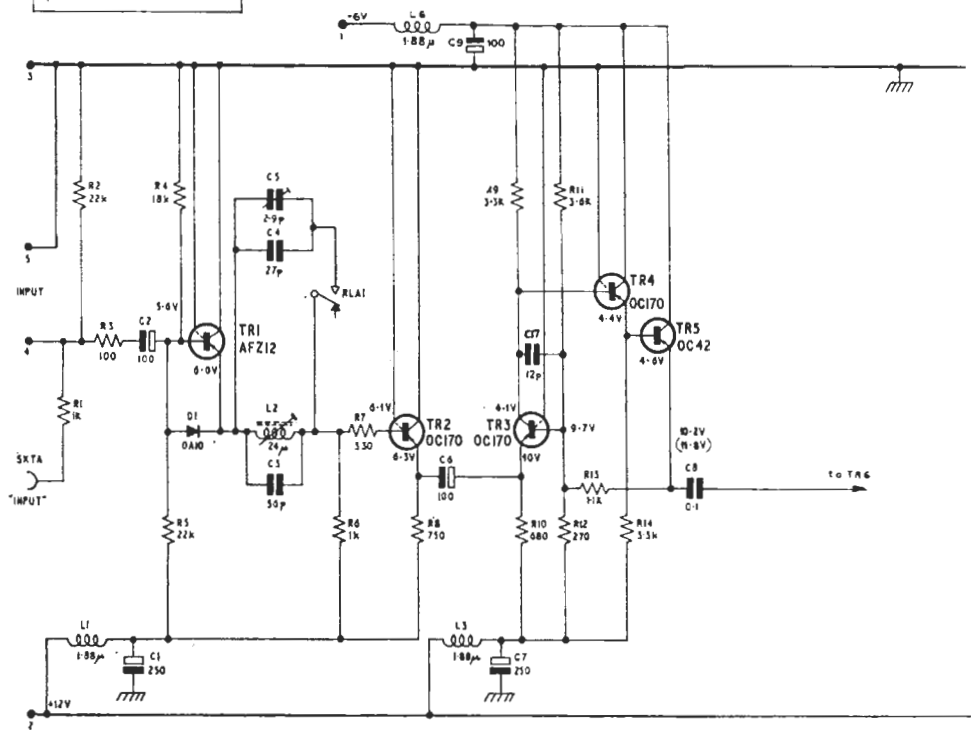
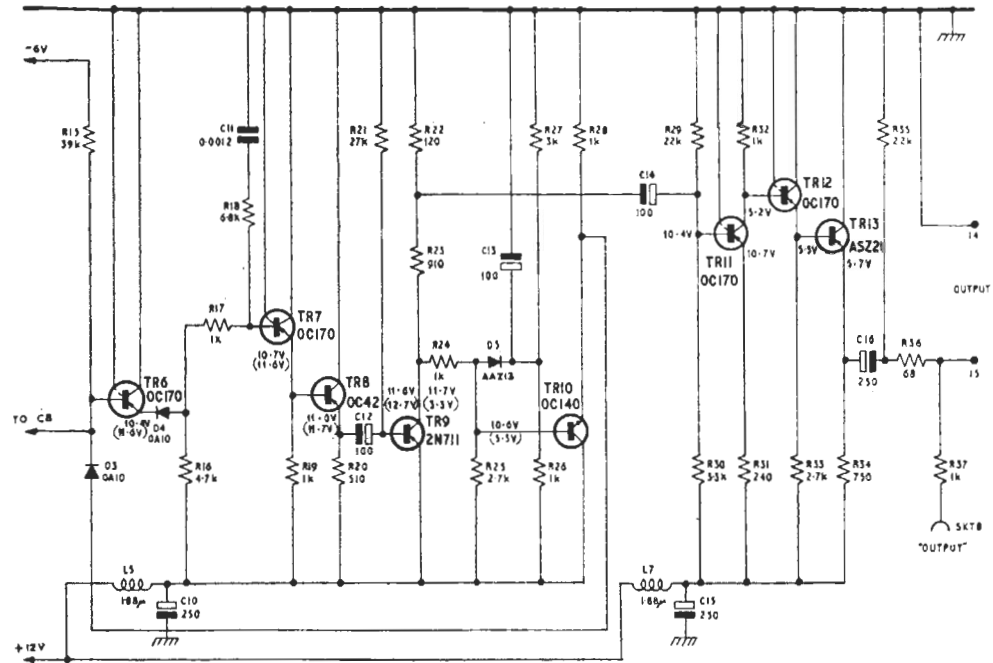


Fig. 23.2
Circuit of the UNI/523



NOTE: D.C. VOLTAGES IN BRACKETS ARE MEASURED FOR A 1 VOLT COMPOSITE S/T INPUT.

TRANSISTOR TERMINATIONS VIEW ON LEADS

CLARE RELAY RP7641 TERMINATIONS VIEWED ON PINS

VI4/66

The input signal is applied, via emitter-follower TR1, to a chrominance-stop filter. This attenuates the 4.43 MHz sub-carrier when the unit is used for 625-line colour working. For 525-line colour working RLA-1 is operated and capacitors C4 and C5 modify the response of the filter so that it resonates at 3.58 MHz.

The output from the chrominance filter is applied, via emitter-follower TR2, to a feedback amplifier consisting of transistors TR3, TR4 and TR5. From this amplifier the signal is applied to the base of TR6 where the tips of the sync pulses are clamped by diode D3. Most of the positive portion of the signal developed at the emitter of TR6 is removed by the clipping action of diode D4, thus making the subsequent sync separation less dependent on picture content. From D4 the signal passes, via emitter-followers TR7 and TR8, to the sync separator stage TR9. The low-frequency boost network R17, R18, C11 provides correction for tilt introduced into the signal waveform by the time-constant of C8 and R15.

Negative-going sync pulses are d.c. restored at the base-emitter junction of TR9. The positive-going sync pulses developed at the collector of this stage are fed, via amplifier-inverter TR11, to the cascaded emitter-follower output stage TR12 —TR13 and also to the clamp-pulse circuit D5 and TR10.

When TR9 is cut off D5 is held in a non-conductive state by the potential present at the junction of

R26 and R27. When a sync pulse is applied to the base of TR9 the transistor bottoms, D5 conducts and a pulse is developed at the emitter of TR10. This pulse is applied as a clamp pulse to the base of TR6, via diode D3.

Maintenance

Check voltages throughout the unit against those shown in Fig. 23.2. Any serious discrepancy usually indicates a fault. The loading introduced by some meters and oscilloscopes may cause instability and, in these instances, a 1-kilohm resistor should be used in series with the test prod.

If faults within the clamp feedback-loop are difficult to locate:

- (a) Open the loop by disconnecting the base of TR10 from the circuit and connecting it to the junction of R26 and R27.
- (b) Check that D3 acts as a d.c. restorer and holds the tips of the sync pulses at a potential of about +8.5 volts. (If not, the fault lies between D3 and the junction of R26 and R27.)
- (c) Check waveforms and voltages between TR6 and TR9.

Note: The clamp circuit has appreciable gain; great care must be taken when checking potentials in this region as a short-circuited electrode would result in the destruction of the subsequent semiconductor.

TES 1/67