SECTION 27

SYNC SEPARATOR UN1/527

Introduction

The Sync Separator UN1/527 provides a total of seven outputs at line, field and picture repetition rates from an input which is either a composite video signal or mixed sync-pulses.

The UN1/527 is constructed on a CH1/12A chassis with index peg positions 7 and 14.

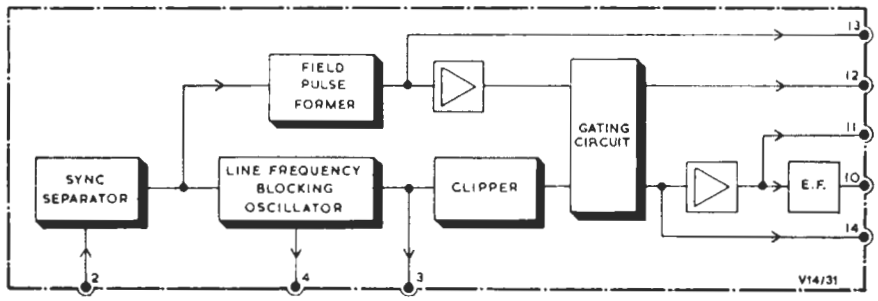

Fig. 27.1 Block Diagram of the UN1/527

General Description

A block diagram of the Sync Separator is shown in Fig. 27.1. A sync separator stage removes any picture information from the input signal on pin 2. The sync-pulses are fed to a blocking oscillator[1,2] which has two outputs; a line-frequency ramp waveform on pin 3 and positive-going line-frequency pulses on pin 4. The sync-pulses are also fed to a field-pulse former which gives positive-going field pulses on pin 13. The field and line pulses are gated together to give positive-going odd-field picture-frequency pulses on pin 12 and negative-going even-field picture-frequency pulses on pin 14. The latter are lengthened in duration to give an output on pin 11. The lengthened pulses are also used as an input to a coincidence gate formed by joining together the outputs from the emitter followers (pin 10) of two UN1/527 units.

Circuit Description

The circuit of the UN1/527 is given in Fig. 27.2 and relevant waveforms in Fig. 27.3. The input signal, Fig. 27.3(a), is fed through an emitter follower to a sync-separator stage. In the absence of a signal transistor TR2 is bottomed through resistor R4. Application of a signal causes d.c. restoration and the transistor is cut off except during sync-pulses, Fig. 27.3(b). These sync-pulses are fed to a line-frequency blocking oscillator. The relaxation time of the oscillator is adjusted, by varying the value of resistor R8, to avoid double triggering during the field signal. The outputs of the oscillator are shown in Figs. 27.3(c) and 27.3(d). The ramp waveform is fed via a complementary emitter follower, transistors TR5 and TR6, to the emitters of the switching transistors TR9 and TR10.

The sync-pulses are also fed to the base of transistor TR7 through a differentiating circuit with a time constant of 22 μs. This produces a droop in the waveform, Fig. 27.4(f). Only in the intervals between the broad pulses is the base sufficiently negative to cause transistor TR7 to conduct. The collector of transistor TR7 is connected via capacitor C5 and a low impedance to a positive potential. In the interval after the first broad pulse, transistor TR7 conducts and discharges capacitor C5. The capacitor cannot recharge during the remainder of the broad pulse period as its supply, which comes via diode D3 and resistor R22 from the collector of transistor TR2, is virtually at earth potential during this period. Thus, a single negative-going pulse is produced at the emitter of transistor TR7, Fig. 27.4 (g). This pulse is inverted by transistor TR8 and fed to the bases of the switching transistors TR9 and TR10; Fig. 27.4(h).

Transistors TR9 and TR10 are symmetrical switching transistors[1]. A current pulse applied to

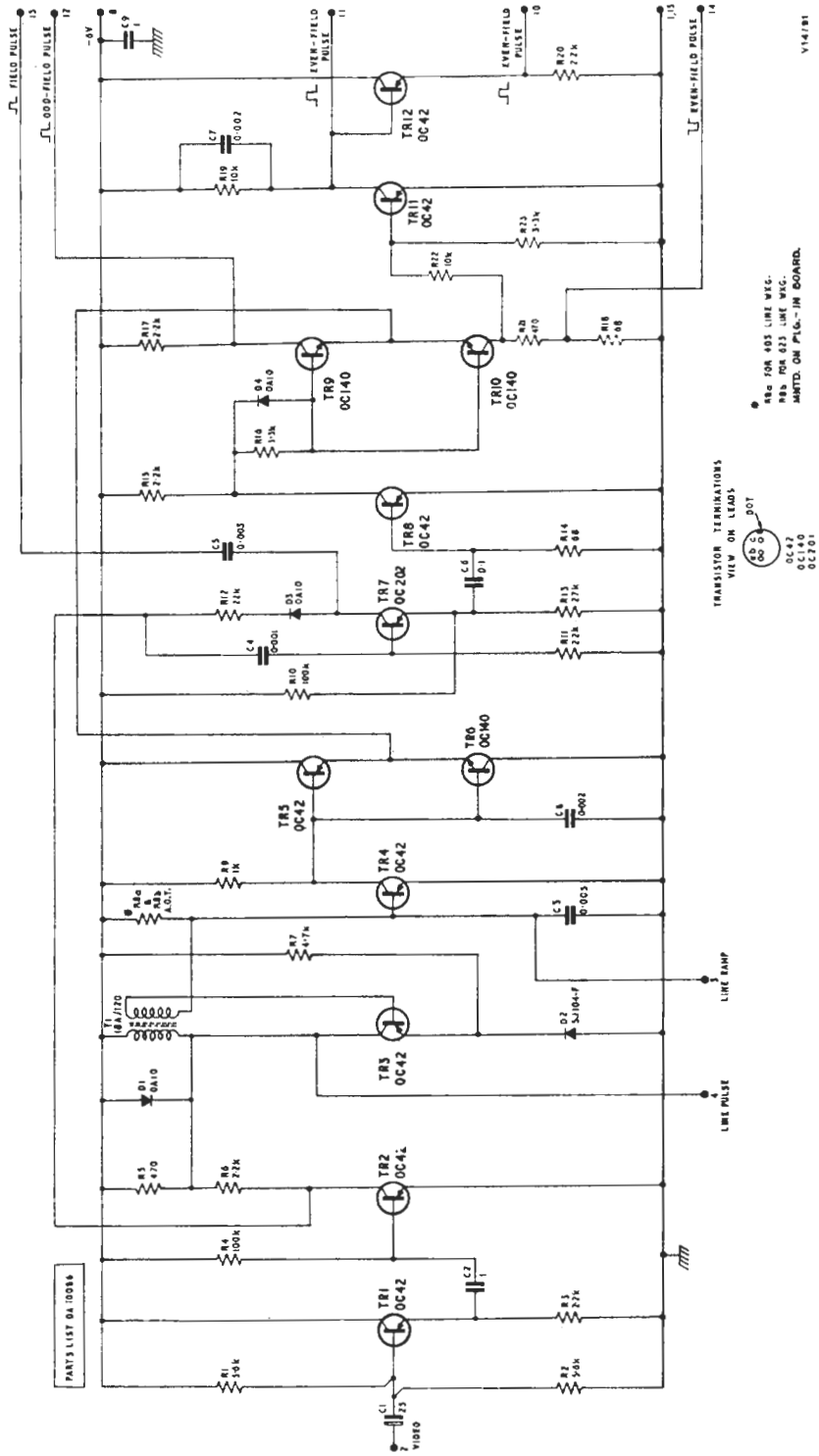

Fig. 27.2 Circuit of the UN1/527

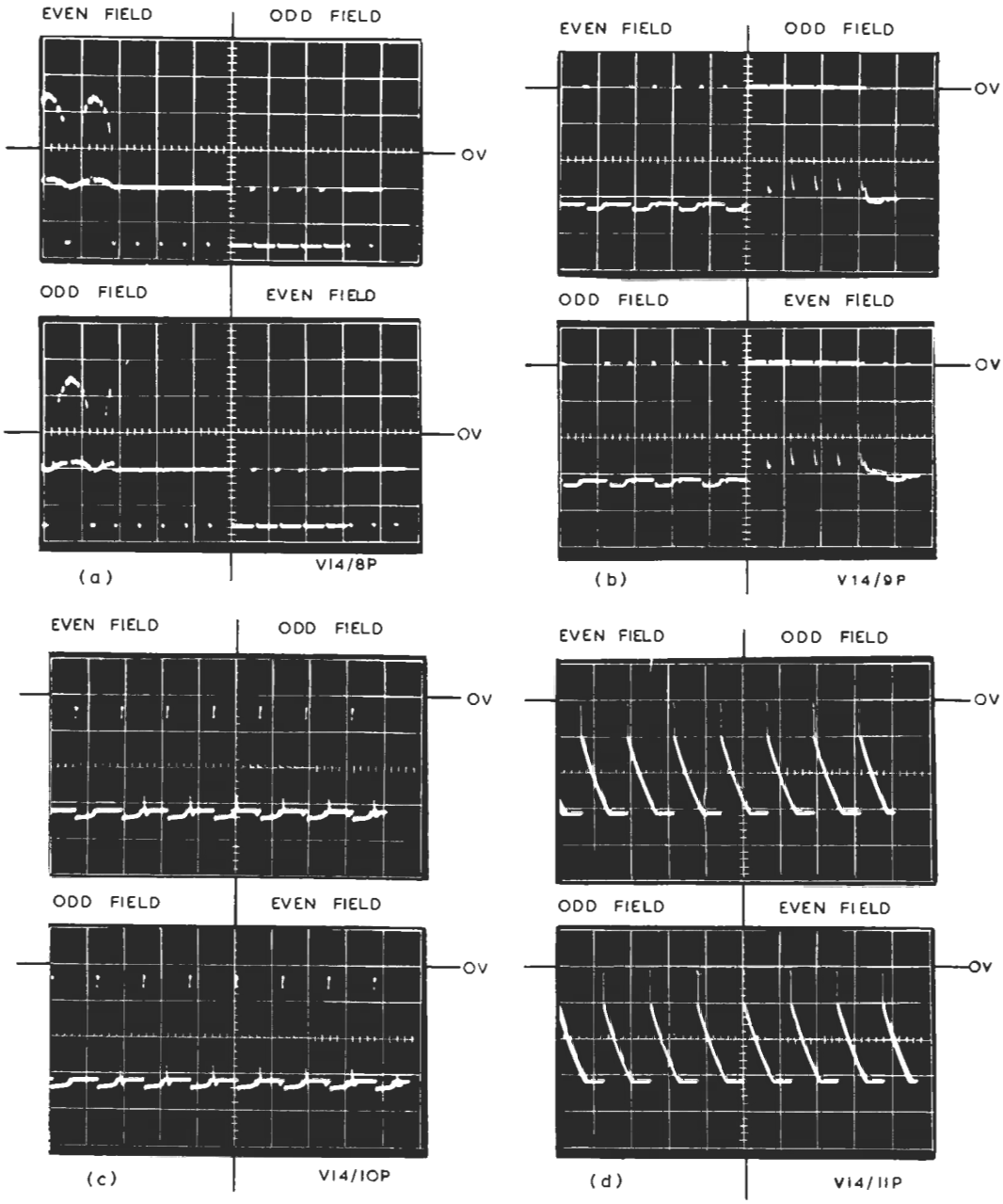

Fig. 27.3 Waveforms in the UN1/527
(a) pin 2 (b) collector TR2 (c) pin 4 (d) pin 3
Vertical scale: (a) 0·2 volts/square
(b), (c), (d) 2·0 volts/square
Horizontal scale: 50 μs/square

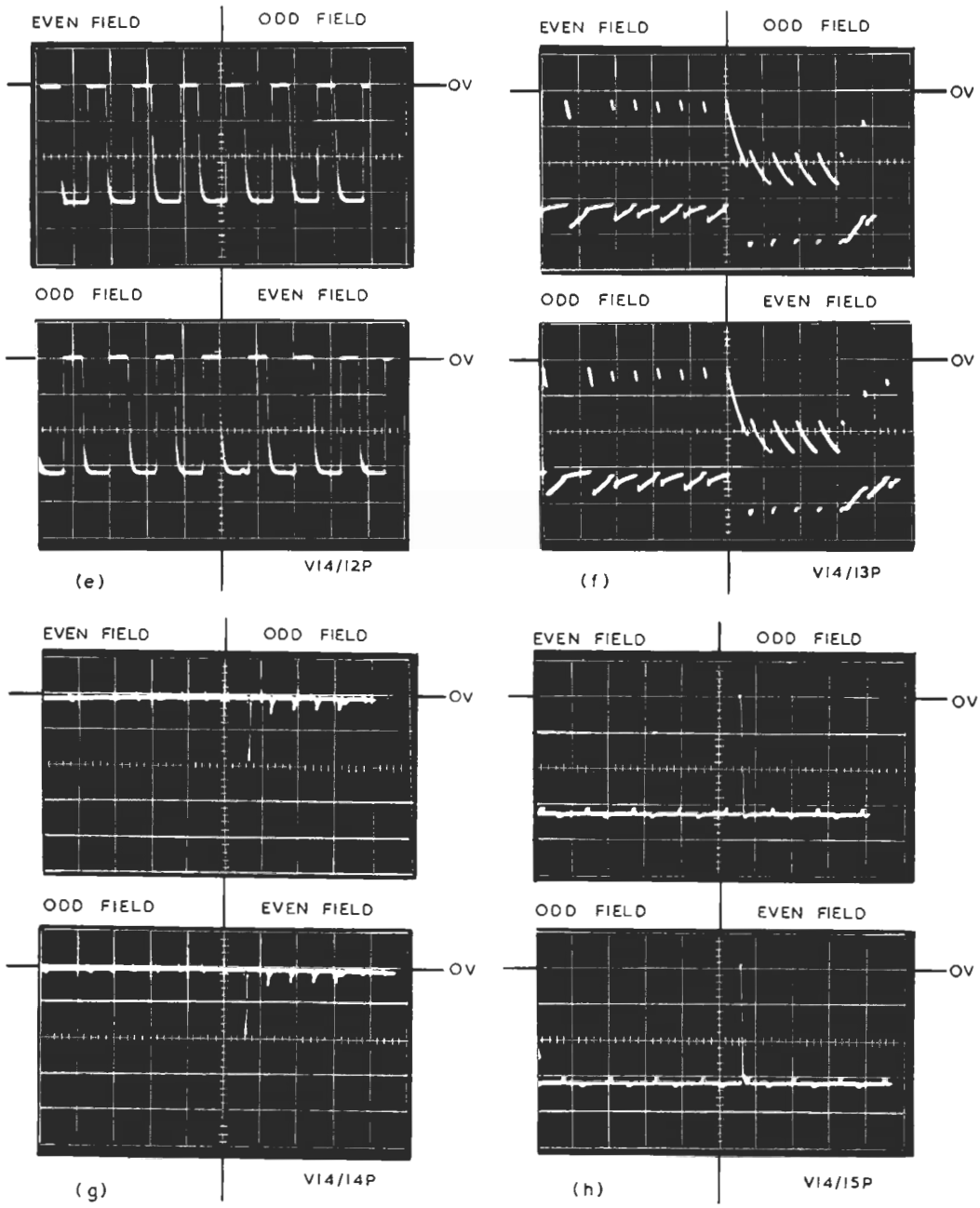

Fig. 27.4 Waveforms in the UN1/527
(e) emitters TR5, TR6, TR9, TR10 (f) base TR7 (g) base TR8 (h) bases TR9, TR10
Vertical scale: 2·0 volts/square
Horizontal scale: 50 μs/square

their bases causes their emitter-collector resistance to drop to about one ohm. Their emitter and base waveforms are shown in Fig. 27.5(j). On each odd field the emitters are at a positive potential and so a positive-going pulse appears at the collector of transistor TR9; Fig. 27.5(l). Similarly, on each even field a negative-going pulse appears at the collector of transistor TR10; Fig. 27.5(k). This pulse, fed to transistor TR11, charges capacitor C7 giving a stretched pulse; Fig. 27.5(m).

The emitters of transistors TR12 in the two Sync Separators are sometimes joined together so that they form a pulse coincidence detector[3].

Test Schedule

A Picture Synchroniser UN1/528 may be used as a test jig and source of power for the UN1/527. The steps given in the test procedure are identical on both line standards. Where the figures differ, the 625-line standard test figures are given in brackets. The tests are to be carried out on both line standards.

Apparatus Required

Line strobing oscilloscope, Tektronix Type 524AD.
4-dB switched attenuator.
Sources of 405-line and 625-line composite video signals.
Extender board CH1A/1 if tests are carried out using a UN1/528 as a test jig.

Test Procedure

1. Check that the plug-in card is in the 405-line (625-line) position. Short circuit pins 8 and 13. Feed the video signal at normal level to the terminated input of the Sync Separator.
   Externally trigger the oscilloscope at line frequency from pin 2.
2. Observe the output at pin 3. Its general form should be that shown in Fig. 27.3(d). The horizontal portion of the waveform should have a duration within the limits 25—30 μs (15—20 μs). If the duration lies outside these limits change the value of resistor R8A (R8B). Increasing the value of the resistor decreases the duration. The amplitude of the waveform should be 5—7 volts p-p.
   Check that the oscillator is not being double-triggered during the field signal period.
3. The waveform at pin 4 should be as shown in Fig. 27.3(c). The amplitude should be 6·0 ± 0·3 volts and the duration of the pulse should be 1·9 ± 0·3 μs.
4. Observe the waveform at pin 12 with the oscilloscope set to display the field signal period. The waveform, shown in Fig. 27.5(l), should have an amplitude of 6·0 ± 0·3 volts. Spurious signals in both fields should have an amplitude less than 0·5 volts.
5. The waveforms at pins 10 and 11 should be as shown in Fig. 27.5(m). The amplitude should be 6·0 ± 0·5 volts and the duration should not be less than 10 μs.
6. The waveform at pin 14 should be as shown in Fig. 27.5(k). The amplitude should be 0·8 ± 0·1 volts and the duration should be about 5 μs. Spurious signals on both fields should be less than 0·2 volts.
7. Check that a 4-dB reduction in input level does not appreciably affect the output waveforms. Remove the short circuit from between pins 8 and 13.

Further Information

Typical voltages at transistor terminals, measured with an Avometer Model 8, with a normal input are given in Table 1 to assist with fault finding.

TABLE 1

Transistor	*Emitter*	*Base*	*Collector*
TR1	−3·0	−3·1	−6·4
TR2	0	+0·2	−5·7
TR3	−0·5	+1·0	−6·4
TR4	0	+1·0	−5·0
TR5	−5·0	−5·0	−6·4
TR6	−5·0	−5·0	0
TR7	−1·0	0	−5·5
TR8	0	0	−6·4
TR9	−5·0	−6·3	−6·4
TR10	−5·0	−6·3	0
TR11	0	0	−6·4
TR12	−5·9	−6·0	−6·4

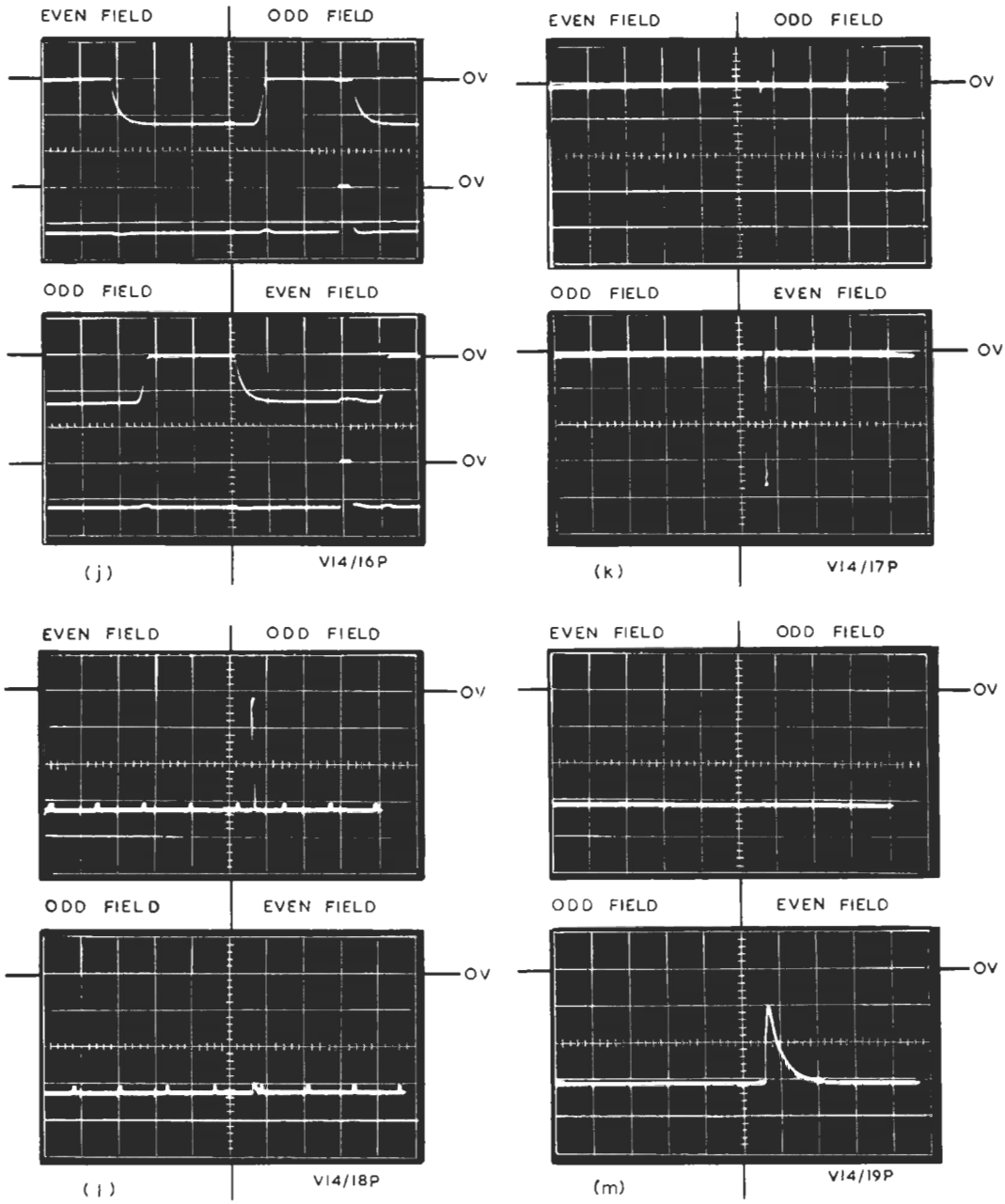

Fig. 27.5 Waveforms in the UN1/527
(j) emitters TR9, TR10; bases TR9, TR10 (k) collector TR10 (l) collector TR9 (m) pin 11

Vertical scale:	*(j)*	*10 volts/square*
	(k), (l), (m)	*2 volts/square*
Horizontal scale:	*(j)*	*20 μs/square*
	(k), (l), (m)	*50 μs/square*

Bibliography

1. Amos, S. W.; Principles of Transistor Circuits: Iliffe.
2. Television Engineering (Vol 3): Iliffe.
3. Technical Instruction V.6.

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