SUBCARRIER PHASE SHIFTER UN1/537 and UN1/537A

Introduction

The UN1/537 accepts an input of 4·43 MHz (3·58 MHz for UN1/537A) colour subcarrier at a level of 1 volt p-p, and produces an output signal having the same frequency but shifted in phase with respect to the input by any value between 0 and 360 degrees. An a.g.c. circuit forming part of the unit maintains the output level at 1 volt p-p for changes of input level not greater than ±6 dB (with reference to 1 volt).

The unit is constructed on a CH1/12B chassis with index-pin positions 4 and 29. A d.c. power supplier is incorporated in the unit, and consumes 8 watts from an a.c. input of 230 volts.

General Specification

Input Signal Level (externally terminated)	1 volt p-p ±6 dB
Output Signal Level	1 volt p-p ±0·1 dB
Output Phase Variation (for change in input level of ±6 dB)	Less than 1 degree
Output Phase Controls	
Calibrated control 1	0°-270° in 90° steps
Calibrated control 2	0°-100° in 20° steps
Uncalibrated control	0°-35° continuously variable
Temperature Stability (operating range)	20°C-45°C
Power Consumption	8 watts at 230 volts ± 6 per cent

Circuit Description

Fig. 1 shows the complete circuit diagram of the UN1/537 (or UN1/537A).

Power Supplier Section

Diodes D5 to D8 are fed with low-voltage a.c. from transformer T3 and produce a d.c. output which is applied to a conventional series regulator circuit comprising TR15, TR16 and TR17. Zener diode D9 provides the necessary voltage reference; variable resistor R50 enables the supplier output to be adjusted to the required value of 12 volts.

Phase-shifter Section

The incoming subcarrier signal is capacitively-coupled to TR1 which feeds the first stepped phase-shifter circuit via transformer T1. A total of 270 degrees of phase shift at 4·43 MHz (or 3·58 MHz for the UN1/537A) can be obtained from these networks. Any one of the four values of phase shift arranged in increments of 90 degrees can be selected by S1. Emitter follower TR2 offers a high impedance to the output from the switch, and passes the signal to the second series of phase-shift networks through T2. Switch S2 provides a further 100-degree adjustment of the total phase shift in steps of 20 degrees.

The two calibrated-control knobs (for operating S1 and S2) are mounted on the front panel and jointly labelled ADJUST PHASE. Note that, unlike the 90-degree-stepped network, the 0-degree position of S2 does not give direct connection to the transformer, but actually produces an opposing phase-shift of 40 degrees. This circuit configuration is necessary so that zero insertion-loss conditions can be more easily satisfied; it also results in a smaller variation of the network output level with change of tapping point. The unwanted 40 degrees of 'leading' phase shift produced by this connection is compensated by additional 'lagging' phase shifts elsewhere in the circuit such that, with all controls set to zero, the unit produces 0 degrees of phase shift.

Emitter follower TR4 feeds the subcarrier signal to a phase shift network comprising L1, R18, R19 and C13, with resistor R18 providing continuously-

variable adjustment of the phase shift. R18 is controlled by an uncalibrated knob located on the front panel and marked FINE CONTROL. The maximum phase shift produced by this circuit is limited (by R19) to 35 degrees; the inductance of L1 is set so that the minimum possible phase shift through the circuit is zero degrees.

Output-level-controlled Attenuator (A.G.C.)

The subcarrier signal from the phase-shift networks is applied to emitter-follower stages TR5 and TR6, which provide a low-impedance source for the balanced-diode, d.c.-controlled attenuator comprising diodes D1 and D2. These diodes are forward-biased by the current from TR7, the value of which determines the impedance presented to the subcarrier signal at the junction of D1 and D2. By varying the current (and hence the effective impedance), the signal level may be controlled over a range of 12 dB. Note that two diodes are employed so that their non-linear characteristics are mutually compensating thereby reducing signal distortion to a minimum.

The 100-mV subcarrier signal at the diode junction is passed to a four-stage output amplifier where it is raised in level to 1 volt p-p from emitter-follower TR14. The signal at this point is also used to provide negative feedback to the first of the four stages (TR11), and to supply a sample of the output signal via emitter-follower TR10 to a peak-level detector circuit comprising diodes D3 and D4. By this means a uni-directional voltage appears across C17 having a value which varies in sympathy with the unit subcarrier output level. The voltage on C17 is applied to TR9 (one half of the long-tailed pair TR8, TR9) and is thus compared with a reference voltage from R25 through TR8. The output from TR9 collector is used to vary the current through TR7, and hence controls the sub-carrier-signal attenuation effected by diodes D1 and D2.

The range of voltage available from R25 is such that the output level from the unit can be adjusted to any value within 3 dB of 1 volt p-p.

Maintenance

Regular maintenance is not required for the UN1/537, and adjustment of internal controls should not be needed except after component replacement.

R50 must be adjusted to give a supply of −12 volts with reference to the chassis potential (0 volts).

R25 acts as the output amplitude control, and is adjusted so that the unit produces a level of 1 volt p-p into 75 ohms. Note that the level from the front-panel monitor point (marked OUTPUT LEVEL) is not an accurate indication of the actual output level.

As a guide to fault finding the following table of voltages is typical of a correctly-operating unit. All voltages were measured with an Avo Model 8 meter on the 25-volt range, and are referred to the chassis potential. Note also that, in a typical unit, each of the stepped phase-shift networks offers a 6-dB insertion loss. Thus, the p-p signal level at the emitter of TR3 should be about 0·5 volt and that at the emitter of TR4 should be about 0·25 volt (for an input level of 1 volt p-p).

Transistor	*e* (V)	*b* (V)	*c* (V)
TR1	−10·0	−9·3	0
TR2	−9·8	−9·1	0
TR3	−10·5	−9·8	0
TR4	−8·5	−7·8	0
TR5	−9·2	−8·5	0
TR6	−10·0	−9·2	0
TR7	−10·7	−10·0	−0·2
TR8	−1·3	−1·8	−7·5
TR9	−1·3	−1·8	−10·0
TR10	−1·4	−1·2	−12·0
TR11	−5·6	−5·8	−9·4
TR12	−10·2	−9·4	−5·1
TR13	−4·3	−5·1	−12·0
TR14	−5·0	−4·3	0
TR15	−12·0	−12·2	−21·8
TR16	−12·2	−12·3	−21·8
TR17	−6·2	−6·4	−12·3

References

Designs Department Technical Memorandum No. 8.182(65).
Designs Department Technical Specification No. 8.196(65).

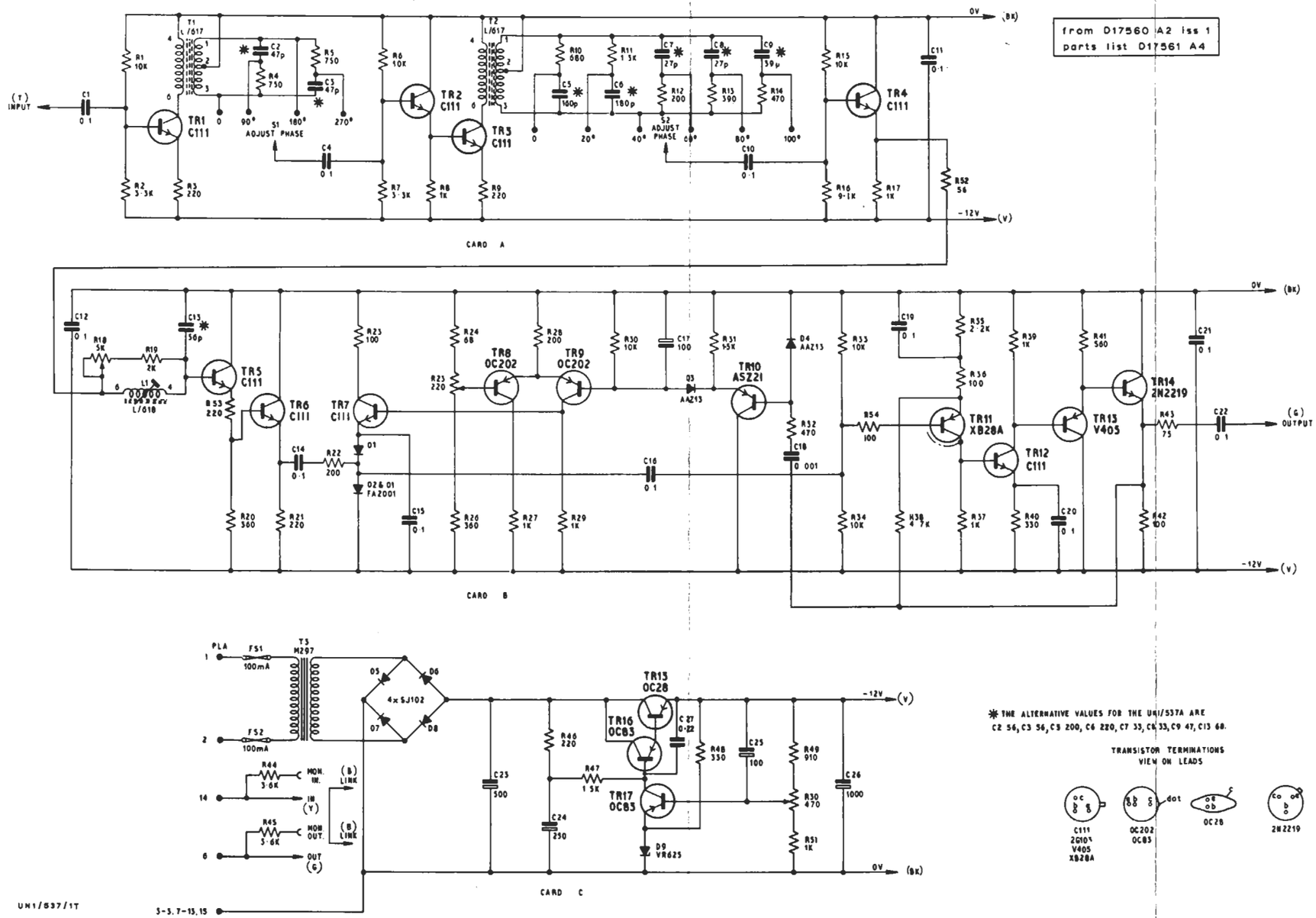

Fig.1 Subcarrier Phase-shifter UNI/537