TRIGGER UNIT UN1/558

Introduction

This unit accepts either a composite video signal or a mixed-sync signal and provides a selection of pulse waveforms which can be used to trigger the x-deflection circuits of waveform monitors[1]. An auxiliary output is provided which consists of the input signal plus a strobe marker pulse. The unit is switchable between the 405 and 525/625 line-standards.

The UN1/558 is constructed on a CH1/12B chassis with index-peg positions 24 and 30. The trigger output and auxiliary output signals appear at Musa plugs, labelled *Output* and *To Pic. Mon.* respectively, which are located on the front panel of the unit. Also located on this panel are *Trigger Selection* and *Field Change* switches and *Red Delay* and *Blue Delay* control knobs.

Power supplies at +5·7 volts and −5·2 volts are derived from an internal mains-driven power supplier. Mains fuses are provided on the rear panel of the unit.

General Specification

Input	
Composite Video	1 V p-p ±0·5 V
Mixed Syncs (alternative)	0·15 to 1 V p-p
Trigger Output	
(a) Unterminated	4 V p-p negative-going
(b) Terminated (recommended for cable lengths of more than 6 ft.).	2 V p-p negative-going
Auxiliary Output	Input signal plus a marker pulse
Impedances	
Input	1 kilohm ±10%
Trigger Output	75 ohms
Auxiliary Output	75 ohms
Mains Input	210-250 V
Power Consumption	5 W at 240 V

General Description

A simplified block diagram of the unit is shown in Fig. 1. This diagram is intended only to show signal paths through the unit and trigger timings; it should not be interpreted as a block version of the circuit diagram. An arrow through a block indicates that the delay provided by that block is variable; the timings given are for 625-line operation. All the gates shown are *And* gates[2] which provide an output only when a signal is present on both inputs.

The letter references *a* to *j* in the selector-switch block correspond to the same references on the circuit diagram. The T.L.S./strobe switch forms part of the selector switch. The trigger pulses provided for each position of this switch are listed below.

1. *Line* One trigger pulse per line, coinciding with the negative-going edge of syncs.
2. *Field* One trigger pulse per field, coinciding with the leading edge of the first sync pulse to occur in the middle of a line. Note that this trigger pulse gives a non-interlaced display.
3. *Pulse* (Sine-squared Pulse) One trigger pulse per line, occurring at about the same time as the sine-squared pulse in a pulse-and-bar waveform. The timing of this pulse can be adjusted by the *Red Delay* control.
4. *P and B* (Sine-squared Pulse and Bar) Two trigger pulses per line; the first as in position 3 above, the second occurring during the bar signal in a pulse-and-bar waveform. The timing of the second pulse relative to that of the first can be adjusted by the *Blue Delay* control.
5. *Bar* One trigger pulse per line, occurring at the same time as the second trigger pulse in position 4. The timing can be adjusted by the *Red Delay* and *Blue Delay* controls.
6. *Strobe* One line-sync trigger pulse per picture, selected by the *Red Delay* control in conjunction with the *Change Field* switch.
7. *Strobe Dl'd* (Strobe Delayed) One trigger pulse per picture, delayed by between one

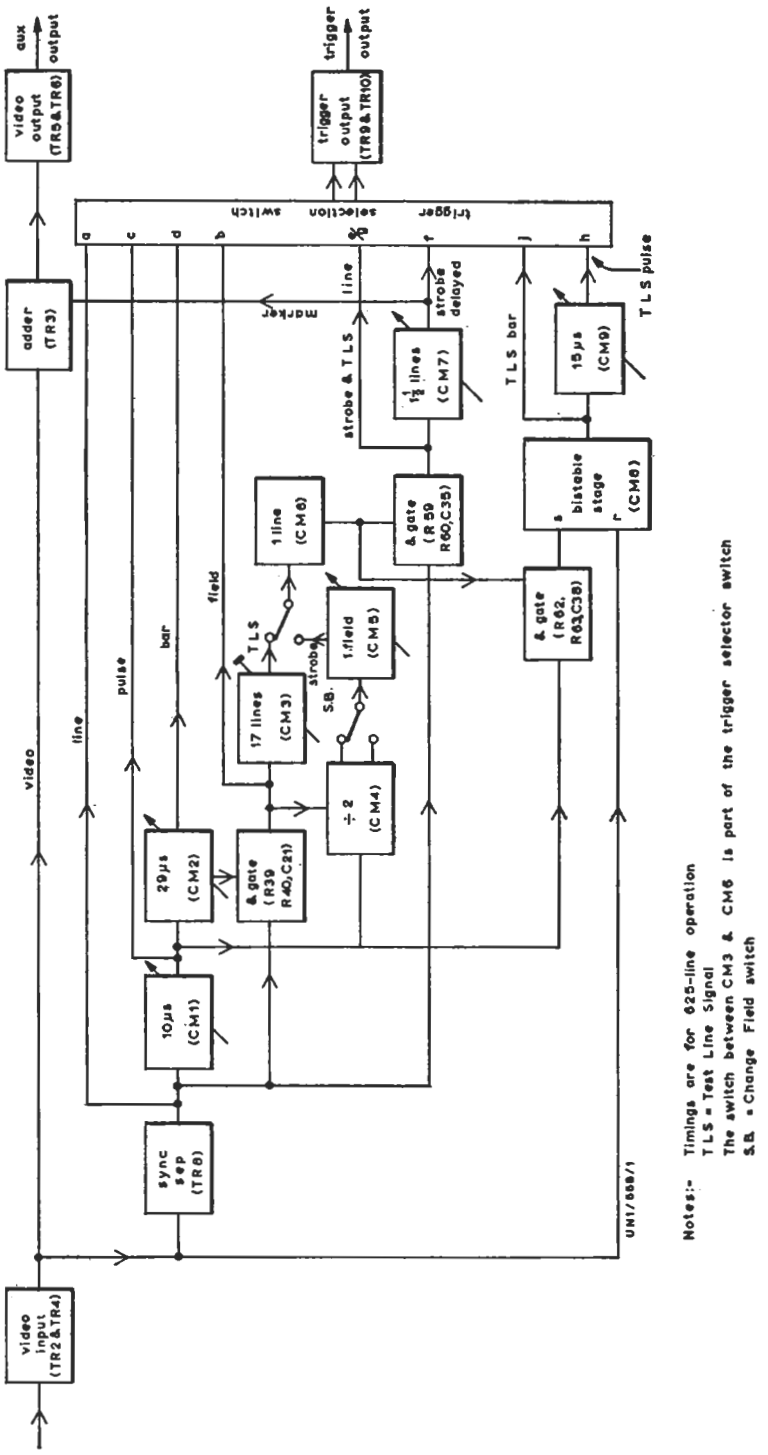


Fig. 1. Simplified Block Diagram of UN1/558

and two lines with respect to the *Strobe* trigger pulse. The additional delay is provided by the *Blue Delay* control. A marker pulse appears on the auxiliary output of the unit coincident with this trigger.

8. *Test Line Signal—Line* One trigger pulse per field coincident with the leading edge of the line-sync pulse immediately preceding the field blanking interval Test Line Signal[3]. The timing of this trigger pulse is preset by means of RV1; on early models it is set for lines 12 and 214 for 405-line working, and lines 16 and 329 for 625-line working.

   A Test Line Signal (or Insertion Test Signal) waveform is shown in Instruction V1, Appendix B. Note that, although *Test Line Signal* is engraved on the front panel of the UN1/558 against the appropriate switch positions, this waveform is now known as Insertion Test Signal 1. However, for the sake of clarity, it will be referred to as a Test Line Signal throughout this Instruction.
9. *Test Line Signal—Pulse* One trigger pulse per field, delayed by means of the *Red Delay* control with respect to the positive-going edge of the Test Line Signal Bar so that it occurs in the vicinity of the Test Line Signal sine-squared pulse. Note that, in instances where the Test Line Signal carries colour information, the sine-squared pulse referred to is the 2T luminance pulse and not the 10T luminance-plus-chrominance pulse.
10. *Test Line Signal—Pulse and Bar* Two trigger pulses per field; the first coincident with the positive-going edge of the Test Line Signal bar, the second as in position 9 above.

Circuit Description

The circuit diagram is given in Fig. 2 on page 7. The following description assumes 625-line working.

Integrated Circuits

Only one type of integrated circuit module (Motorala type MC352 G) is used in the UN1/558. This consists of a bistable device which has a two-input OR gate[2] associated with each input and thus has four inputs and two outputs. Nine integrated circuit modules are used in the unit; one (CM8) is used in the bistable mode and the others are modified by the addition of external components. Of the modified modules, one (CM4) is converted to a divide-by-two stage and the remaining seven are converted to monostable multibrators.

Positive logic is used throughout; a voltage of −0·8 volts is referred to as a *1* Signal and a voltage of −1·6 volts is referred to as a *0* Signal. Voltages more negative than −1·6 have the same effect as a *0*.

A truth table for the MC352 G module, which shows the output provided for any combination of inputs, is given in the circuit diagram. The waveforms shown adjacent to the truth table illustrate typical triggering pulses. The differentiating time constants used at the module inputs are about 150 ns and the rise and fall times of the output waveforms are about 10 ns.

And Gates

All the *And* gates in this unit consist of a potential divider network and a capacitor; for example the gate at the R input of module CM3 consists of R39, R40 and C21. The inputs to this gate are output P of CM2 and output P of CM1.

The values of R39 and R40 are such that the steady potential at their junction is about 0·8 volts more negative than that at the P output of CM2 (if P = *1* it is −1·6 volts, if P = *0* it is −2·4 volts). When output P of CM1 changes rapidly from *0* to *1*, the change is applied via C21 to the junction of R39 and R40 and momentarily increases the potential at that point by 0·8 volts. If output P of CM2 is already at *1* the potential at the resistor junction will rise from −1·6 volts to −0·8 volts (logic *1* level) and an output will be produced. If output P of CM2 is at *0* the resistor junction potential will rise only to −1·6 volts and a logic output will not be produced. Thus the gate will provide an output at *1* only when output P of CM2 is at *1* and output P of CM1 changes from *0* to *1*.

Input, Sync Separator and Auxiliary Output Stages

The input signal is applied to a long-tailed pair comprising transistors TR2 and TR4. The signal appearing at the collector of TR2 is fed, via driver stage TR6, to the auxiliary output of the unit and, via emitter-follower TR7, to the sync separator stage TR8. The positive-going sync pulses appearing at the collector of TR8 are applied to module CM1.

A marker pulse which is derived from module CM7 is shaped and clipped by transistor TR3 and is then added to the signal present at the collector of TR4. This signal is then applied to emitter-follower TR5; the emitter of TR5 is connected to the auxiliary output of the unit together with the collector of TR6 and so, because

continued on page 6

TABLE 1

Module	*Function*	*Remarks*
CM1	Provides a *Line* trigger pulse when P changes to *1* and a *Pulse* trigger pulse when Q changes to *1*.	Duration of unstable state 10·5 μs. For certain positions of the trigger-selector switch the timing can be varied by means of the *Red Delay* control.
CM2	Provides a *Bar* trigger pulse when Q changes to *1*.	Duration of unstable state 29 μs. Diode D10 helps the timing capacitors to discharge quickly and thus shortens the reset time. For certain positions of the trigger-selector switch the timing can be varied by means of the *Blue Delay* control.
CM3	Provides a *Field* trigger pulse when P changes to *1*.	Nominal duration of unstable state is 17 lines (see value of C22 in Table 2). Triggered when the P output of CM2 is *1* and the P output of CM1 changes to *1*; this happens only during field-blanking periods and, for 625-line working, first occurs during equalising pulses on lines 311 and 623. Subsequent trigger pulses occurring during the same field-blanking period are ignored. The trigger pulse provided is non-interlacing and occurs in the middle of a line for both fields.
CM4	A divide-by-two stage which converts the field-frequency trigger pulses from CM3 to picture-frequency trigger pulses for feeding to CM5.	The input *And* gates are arranged so that they steer the applied trigger pulse from one input to the other on alternate fields. It does not matter whether the *1* is at output P for even fields and output Q for odd fields or conversely, as a *Change Field* switch is provided between CM4 and CM5.
CM5	A line-selector stage which provides the run-down period from the field trigger pulses to the portion of the picture selected for strobing.	This module remains in the unstable state for long periods and so a transistor is used to drive the timing capacitor C30. TR11 is biased so that it normally conducts; thus the normal charge on C30 is small and the voltage applied to input R (pin 10) is more negative than a logic *0* and is thus equivalent to *0*. When a trigger pulse is applied to input S, output P falls to *0* and the negative-going transition cuts TR11 off. C30 now commences to charge up through R52 (modified by RV2 and R69 when SA is in positions 6 and 7) and the resulting ramp voltage is applied to input R (pin 10). When the ramp voltage approaches *0* the next trigger pulse from CM2 gets through to the input and changes the state of the module. Output P than changes to *1*, TR11 conducts and C30 discharges through R53 and the transistor. Input R (pin 9) plays no part in the normal operation of the module, but it ensures that the correct working conditions are established when

Module	*Function*	*Remarks*
		the unit is switched on. To this end the associated *And* gate is arranged so that the module is switched to the P = *1* state by the first trigger pulse emanating from CM4. Subsequent trigger pulses will always switch the module to the Q = *1* state.
CM6	Opens the *And* gates associated with input R of CM7 and input S of CM8 when P changes to *1*.	Duration of unstable state almost one line. When SA is in positions 8, 9 and 10 the gate associated with input R (pin 10) is open and the module is triggered to P = *1* when the Q output of CM3 changes to *1*. When SA is in positions 6 and 7 the gate associated with input R (pin 9) is open and the module is triggered to P = 1 when the P output of CM5 changes to *1*. In the first instance the trigger pulses are at field rate, in the second instance they are at picture rate. When SA is in positions 1 to 5 the module is not triggered.
CM7	Provides a *Test Line Signal—Line* when P changes to *1* and CM6 is triggered at field frequency. When CM6 is triggered at picture frequency a *Strobe Line* trigger pulse is provided when P changes to *1* and a Strobe Delayed trigger pulse when Q changes to *1*. The Q output is applied also to transistor TR3 where it is used to produce a white marker pulse for addition to the video signal.	The positive-going edge of the Q output is nominally delayed by 102 μs with respect to the positive-going edge of the P output; this delay can be varied between one and two lines by means of the *Blue Delay* control. The marker pulse does not pass through the selector switch and so it is added to the video output whenever Q changes to *1*, regardless of the switch position. When the switch is in positions 8, 9 and 10 there will be two marker pulses per picture, on the lines following the Test Line Signal.
CM8	This is a bistable stage which triggers CM9 when P changes to *1*.	CM8 is set to Q = *1* when output P of CM6 is *1* and output Q of CM1 changes from *0* to *1* (a combination that occurs only during the Test Line Signal line-period, about 10·5 μs after the leading edge of syncs). The module is reset to P = *1* when a positive-going pulse of more than 0·2 volts in amplitude is applied to input R. (Input R is fed via a differentiating circuit with the video signal present at the emitter of TR2). The first such pulse to occur after the module has changed to the Q = *1* state is derived from the leading edge of the Test Line Signal bar; if the Test Line Signal is missing from the video waveform the pulse will be provided by the leading edge of the sync pulse in the next line.
CM9	Provides a *Test Line Signal—Bar* trigger pulse when P changes to *1* and a *Test Line Signal—Pulse* trigger pulse when Q changes to *1*.	When SA is in position 9 only the Q output of the module is used; when SA is in position 10 both the Q and P outputs are used. Both outputs are time-related to the positive-going edge of the Test Line Signal bar, and this eliminates any jitter that the Test Line Signal may have with respect to line syncs.

the signals at both points are in phase, the auxiliary output (*labelled Pic. Mon. Output* in the circuit diagram) is taken jointly from transistors TR5 and TR6.

Circuit Modules

The integrated circuit modules from which the various trigger pulses are derived are described in tabular form in Table 1. For 405-line working the timing capacitors of the monostable modules are altered in value by the operation of the line-standards switch SB.

Trigger Output Stage

Transistors TR9 and TR10 form the trigger output stage of the unit. In the absence of input signals both transistors are cut off, but when positive-going transitions of 0·8 volts in amplitude are applied, via the input differentiating circuits, to the base of TR9 both transistors bottom and a negative-going output signal, with a duration of about 1 μs, is developed at the emitter of TR10. Diodes D8 and D9 provide isolation between the two inputs to the stage.

Power Supplier

Transistor TR1 functions as a series regulator; the reference voltage is provided by zener diode D5. The positive (+5·7 volt) and negative (−5·2 volt) supply rails are individually regulated by zener diodes D6 and D7 respectively.

Alignment

Adjustment of RV1

The delay control RV1 is the only component in the unit that is likely to need adjustment; adjustment becomes necessary if C22 is changed in value or if either of the following conditions apply:

(a) If, with the trigger-selector switch set to *Test Line Signal—Line*, an incorrect line trigger pulse is produced or a line trigger pulse is not produced (on either line standard).

(b) If, with the trigger-selector switch set to *Test Line Signal—Bar*, the output trigger pulse corresponds to the trailing edge of a line-sync pulse.

In both instances the Test Line Signal applied to the unit must be present on the same lines as in the initial line-up of the unit. On early models the Test Line Signal line numbers were 16 and 329 for 625-line working and 12 and 214 for 405-line working. (See Appendix for methods of determining the line numbers of Test Line Signals.)

To adjust RV1 proceed as follows:

1. Power the unit and apply a composite video waveform, carrying a Test Line Signal on the appropriate lines, to the input.
2. Set the trigger-selection switch to *Field* and feed the output trigger to the X-input of an oscilloscope. Feed the Y-input of the oscilloscope with the same signal as that applied to the UN1/558 and set the oscilloscope time-base to give a display of three or four lines.
3. Switch to *Test Line Signal—Line* and adjust RV1 until the Test Line Signal appears on the first line displayed on the oscilloscope. (To adjust RV1 remove the left-hand back-plate and insert a screwdriver into the hole provided in the left-hand printed-wiring board.)
4. Switch to *Test Line Signal—P and B* and check that the oscilloscope is triggered near the positive-going edge of the bar. If not, slightly readjust RV1 and then check that the line-sync pulse is still correctly selected.
5. If a television signal containing a correctly positioned Test Line Signal is available on the other line standard, change over the line-standards switch and check that the corresponding triggers are correctly selected by the trigger unit. If it is not possible to obtain the correct triggers on both line standards it is possible that C22 (see Table 2) has been selected for a different combination of Test Line Signals to those being used.

TABLE 2

Line numbers for 625-line Test Line Signals	*Line numbers for 405-line Test Line Signals*			
	11 and 213	*12 and 214*	*13 and 215*	*14 and 216*
	Value of C22 in μF			
15 and 328	0·003	0·082	—	—
16 and 329	0·051	0·024	0	—
17 and 330	0·068	0·043	0·015	—
18 and 331	0·091	0·056	0·30	0·0062
19 and 332	0·11	0·075	0·047	0·020
20 and 333	0·12	0·091	0·062	0·033
21 and 334	0·15	0·11	0·075	0·047

from D16225
parts list D16226

M1 M269 — 12V, 6V, 0V, 12V, 6V, 0V — FS1 100mA, FS2 100mA — D1 D2 D3 D4 1B10J10 — C1 250 — D5 OAZ204 — +5·7V — C2 1000, C3 1000 — D6 VR375A F, D7 VR525B F — R1 3·6k — R2 100, R3 200 — TR1 BFY52 — −3·2V

PLA14 input — C4 100 — R4 10k, R5 1·1k, R6 100 — TR2 PEP5 — R8 1k, R9 430

CM7/5 — C5 0·01, R10 330 — TR3 OC43 — R11 3·6k — R7 910

R12 910 — TR4 PEP5 — R13 1·3k

TR5 BFY52 — R14 1·1k, C6 100, R15 1k, C7 100 — TR6 BFY52 — R16 1·3k, R17 91, R18 110, C8 200

TR7 V405 — R19 33, R21 2·2k — C9 1000, R20 56, PLC pic mon output plug and PLA 12

C10 0·02 — TR8 OC43 — R22 270k, R23 4·7k, R24 1·1k

CM1/6 via C15

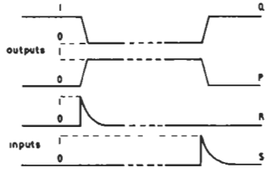
from SA2 & SA3 — C11 560p
from SA4 — C12 560p
R25 91k, R26 91k — D8 OA47, D9 OA47 — R27 180 — R28 4·7k — TR9 PEP5
R29 4·7k, R30 470 — TR10 V405 — C13 1 — R31 56 — PLB trigger output plug and PLA 10 — R32 100k
trigger output stage

① a c — SB1 525/625 405 — C16 0·0012, C17 0·0022 — R33 3·9k — CM1 MC352G
② d — SB2 — C19 0·0033, C20 0·0062, D10 OA47 — R38 3·9k — CM2 MC352G
b — SB3 — C22 *, C23 0·25 — R41 5k, RV1 1k — CM3 MC352G
+5·7V — R43 1·8k — CM4 MC352G — C24 100p, C25 100p — R42 10k, R45 10k
SC — C26 100p, C27 100p — R49 1·8k — CM5 MC352G — R44 1·8k, R46 10k, R47 10k, C28 100p, R48 1·8k, R50 1·8k
C29 — TR11 PEP5 — R53 100, C30a 0·22, C30b 0·33 — R51 500k, R52 120k
⑤ +5·7V
SB4 — C33 0·0068, C34 0·015 — R58 3·9k — CM6 MC352G — C31 100p, R54 1·8k, R55 10k, R56 10k, C32 100p, R57 1·8k
⑦ e/g f — SB5 — C36 0·011, C37 0·022 — R61 3·9k — CM7 MC352G — R59 1·8k, C35 100p, R60 10k
to C5 — C39 560p — CM8 MC352G — C38 100p, R63 10k, R64 10k
⑨ h j — SB6 — C41 0·005, C42 0·005 — R68 3·9k — CM9 MC352G — C40 100p, R62 1·8k, R65 1·5k, R66 10k, R67 1·8k

TR6 collector — C15 470 — R34 1·8k, R35 10k — C18 100p — R37 1·8k, R36 10k — R39 1·8k, R40 10k, C21 100p
−5·2V
PLA6 — C14 0·1 — R71 68

* C22 to be fitted on test

TRUTH TABLE			
S	R	Q	P
0	0	no change	
1	0	1	0
0	1	0	1
1	1	not allowed	



UM1/558/2T

SA1 — +5·7V — RV2 100k — R69 100k — −5·2V red delay — ① CM1/6, ⑤, ⑨ CM9/6

SA2 — +5·7V — RV3 100k — R70 100k — −5·2V blue delay — ② CM2/6, ⑦ CM7/6, j CM9/4

SA3 — d CM2/5 — to C11

SA4 — CM1/4 a, CM3/4 b, CM1/5 c, CM2/5 d, CM7/4 e/g, CM7/5 f, CM9/5 h — line, field, pulse, P & B, bar, strobe, strobe delayed, T.L.S. line, T.L.S. pulse, T.L.S. P & B — to C12

		switch pos
a	line	1
b	field	2
c	pulse	3 & 4
d	bar	4 & 5
e	strobed line	6
f	strobe delayed	7
g	T.L.S. line	8
h	T.L.S. pulse	9 & 10
j	T.L.S. bar	10

transistor terminations view on lines

NOMINAL MULTIVIBRATOR TIMINGS		
line standard	525 & 625	405
CM 1	10·5μs	16μs
CM 2	29μs	45μs
CM 3	(m+1) lines	(n−2) lines
CM 5	16 to 36 ms	16 to 36 ms
CM 6	62μs	93μs
CM 7	102μs	160μs
CM 9	15μs	29μs

Where the 625 line Teet Line Signal is on line numbers m and (m+315) and the 405 line Test Line Signal is on line numbers n and (n+202)

Fig. 2. Circuit of the UN1/558

Note that certain combinations of Test Line Signal are not obtainable. For example, if the 625-line signal is required on lines 15 and 328 then the 405-line signal is not obtainable on lines 13 and 215 or on lines 14 and 216.

Selection of C22

The value of capacitor C22 is chosen for the required Test Line Signal during the initial line-up. If the unit is required to work with Test Line Signals other than those for which C22 was originally selected, then the value of the capacitor must be changed as shown in Table 2. If C22 is changed RV1 *must* be re-adjusted.

Appendix

Two methods of determining the line numbers for Test Line Signals on the 405 and 625-line standards are given below.

Method 1

1. Set the trigger-selection switch to *Field* and apply the trigger output to the X-input of the oscilloscope on which the signal to be checked is displayed. Set the oscilloscope time-base so that the Test Line Signal is just within the display (at the right-hand edge).
2. Count the number of lines from the start of the display to the centre of the line containing the Test Line Signal. Let this number (which should be an integer) be p.
3. The Test Line Signal of the displayed waveform is on lines p −2 and p +311 for 625-line signals, and p +1 and p +203 for 405-line signals.

Method 2

This is an easier method, but it can only be used if it is known for certain how many whole lines there are in the field-blanking period.

1. Count the number of whole lines between the Test Line Signal (exclusive) and the first line containing picture information (exclusive). Let this number be q. (This may be done with any type of display, but if line strobe is used check that both fields give the same number for q.)
2. If the field-blanking period is b lines then the Test Line Signal is on lines b−q−3 and b−q+310 (for 625-line signals) and b−q and b−q+212 (for 405-line signals).
   For example: if it is known that the field-blanking period of a 625-line signal is 25 lines and the number of blank lines between the Test Line Signal and the first picture-information line is seen to be six, then the Test Line Signal is on line numbers (25−6−3) =16 and (25−6+310)=329.
   Note: The difference between line numbers on odd and even fields should always be 313 for 625-line signals and 202 for 405-line signals.

References

1. Waveform Monitor Auxiliary Panel PA1M/529
2. Fundamentals of Switching Circuits, Instruction G.1.
3. Television Standard Waveforms in Studio and Network Distribution Circuits; Instruction V.1, Appendix B.

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