SECTION 61

REVERSIBLE BINARY COUNTER UN1/561

Introduction

The UN1/561 is a six-stage reversible counter[1]. It accepts a pulse input at field frequency and two d.c. direction-control voltages. There are outputs from each stage and two gated outputs which indicate when either end of the counting range has been reached.

The UN1/561 is constructed on a CH1/12A chassis with index peg positions 16 and 28.

General Specification

Inputs

Trigger	3-volt positive-going field-frequency pulses.
Direction control	0 volts and −5 volts.
Output levels	0 volts and −11 volts (approximately).
Output impedance	2 kilohms.

Circuit Description

The circuit of the UN1/561, shown in Fig. 61.1, comprises six bistable stages of conventional design. The first five stages are followed by inverting gate circuits which select the appropriate negative-going output transition to trigger the following stage. The gates are controlled by the *Direction Control* input voltages.

These inputs are 0 volts and −5 volts in one of two possible combinations. The order in which the combinations of output states occur during counting for one combination of direction control voltages is reversed for the alternative combination.

The *End Stop Logic* outputs are negative when the corresponding transistors in all the bistable stages are cut off and are positive under all other conditions.

Test Schedule

Apparatus Required

Oscilloscope.
12-volt and 5-volt power supplies.
Feed of field trigger pulses.

Test Procedure

1. Terminate the feed of field trigger pulses at pin 7 in 75 ohms.
   Connect the 12-volt supply as shown in Fig. 61.1.
   Connect the 5-volt supply: negative to pin 8 and positive to pins 3 and 9.
2. Observe the input waveform and check that the positive-going transitions have a rise-time less than 1 μs.
3. Observe the waveforms at pins 4, 5 and 10 to 15. Check that they have an amplitude of approximately 11 volts and that they conform to the descriptions given in Table 1.

TABLE 1

Pin No.	*Waveform*	*Period (msec)*
4	negative-going 20-ms pulse	1280
5		
10	square wave	40
11		80
12		160
13		320
14		640
15		1280

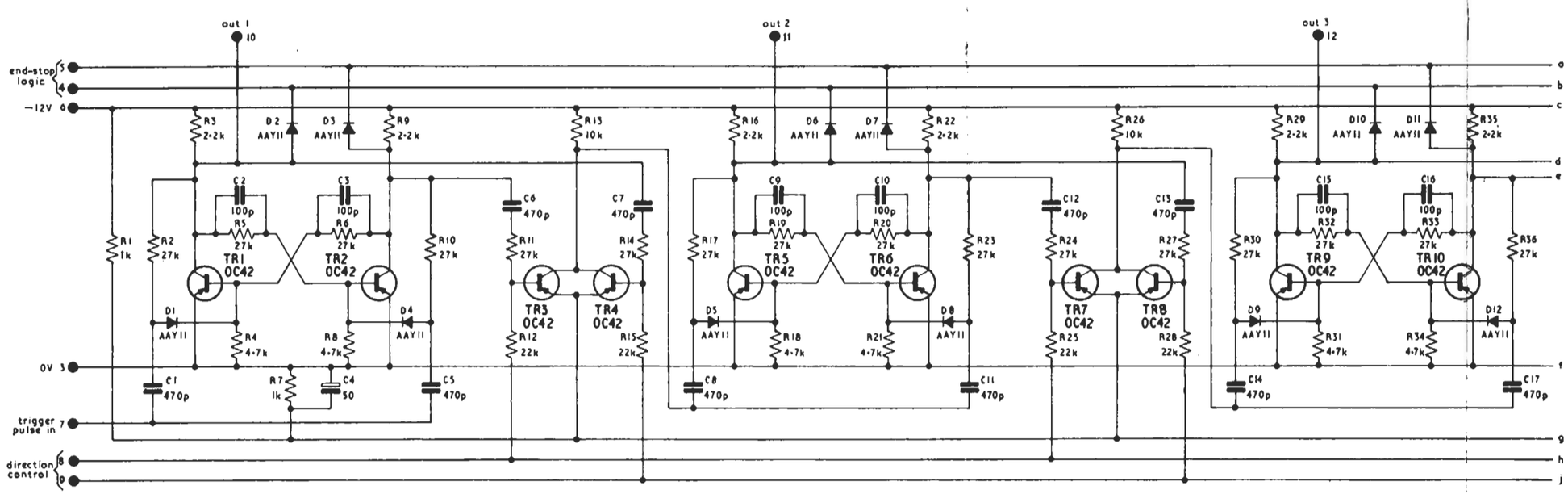
4. Observe the difference waveform between the outputs on pins 4 and 5 and check that the pulse on pin 4 occurs immediately before the pulse on pin 5.
   Exchange the connections on pins 8 and 9. Check that the order of the pulses on pins 4 and 5 has been reversed. Check that the outputs on pins 4, 5 and 10 to 15 otherwise conform to the descriptions given in Table 1.

Bibliography

1. Dean, K. J.; *An Introduction to Counting Techniques and Transistor Circuit Logic:* Chapman and Hall.

See page 61.3 for Fig. 61.1 MJR 11/66

parts list D16317A4



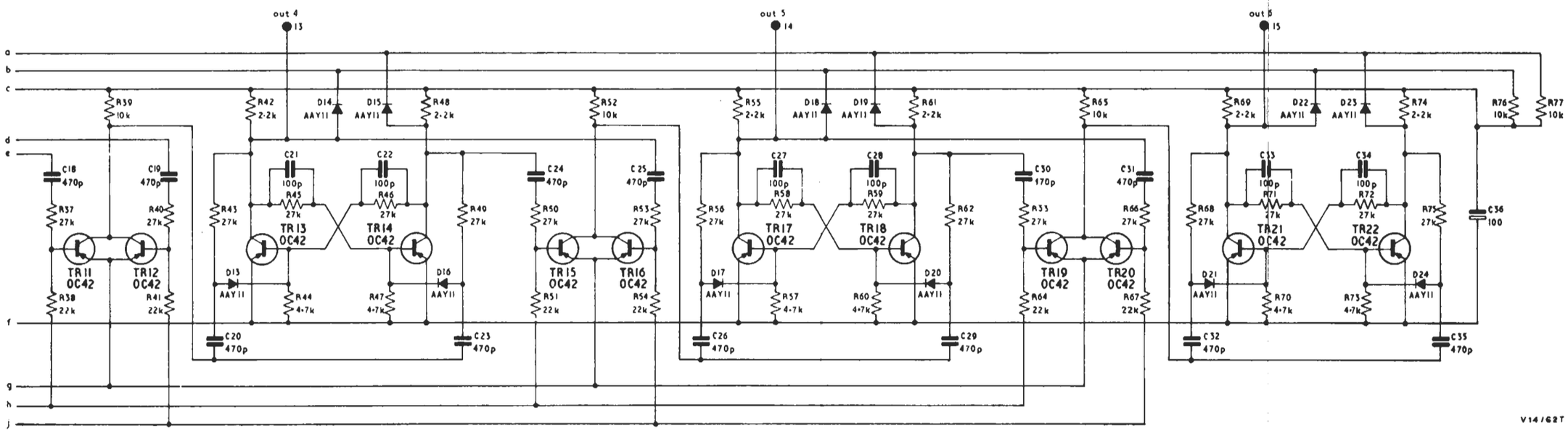


Fig. 61.1 Circuit of the UN1/561