

VISION A.G.C. UNIT UNI/564 SERIES

Introduction

The UNI/564 is a vision a.g.c. unit designed for use in u.h.f. television rebroadcast receivers¹. The unit accepts a direct-coupled video signal with negative-going syncs and derives a positive-going control voltage which depends on the signal level at blanking level. By means of a switch, manual gain control is possible.

The unit is built on to a printed card and mounted in a CH1/12A chassis.

General Specification

Video Input Level (relative to earth) 280 mV p-p with bottom of syncs at -340 mV

Sensitivity: change in output voltage for 0.2 dB change in input greater than 2 V change

Supply Voltages +25 volts
-10 volts

Power Consumption 2.5 watts

Weight 1 lb 5 ozs

Index Pegs 16 and 30

Circuit Description

The circuit is given in Fig. 1. The normal input signal² has positive-going picture with negative syncs and is taken directly to a compound emitter follower which provides a high input impedance and low output impedance. The filter, C21/L1, in shunt with the input, removes the colour sub-carrier. From the emitter of TR2, the signal is fed to an a.g.c. rectifier circuit, to a gating pulse circuit and to an anti lock-out circuit.

The a.g.c. rectifier circuit is fed via the diode gate which is closed except when pulsed from the gating pulse circuit. The pulses occur in the line suppression period immediately following the line-sync pulse. For the duration of the pulse, C1 is effectively connected to the emitter of TR2 which, at blanking level, is at a potential of ap-

proximately -0.25 volts. When the gate is open, a positive pulse appears at the collector of TR6 and this is passed to the rectifier D7. The resulting d.c., after amplification by the long-tailed pair TR13/TR14 and passing through the manual/a.g.c. switch SA, is fed to the output by the emitter follower TR16. The diode, D10, prevents the potential at the base of TR16 from falling below about 10 volts. RV2 sets the a.g.c. bias level.

RV1 is adjusted for minimum disturbance of the waveform in the frame sync period, see Figs. 2(b), 2(c), 2(d).

If the switch SA is in its *Manual* position, the output bias voltage depends on the setting of RV3.

In the clamp-pulse circuit the signal, with positive sync and negative picture, appears at the base of TR7. This transistor operates as a sync separator and negative going sync pulses appear at the collector. These pulses are differentiated by C6/R31 and the positive going spikes, after amplification and inversion, are passed to TR11 and thence via the balancing transformer, to the diode gate.

The anti lock-out circuit (TR15 and TR17) prevents interference with the operation of the unit when a sudden high level signal is applied to the input of the receiver¹ of which the UNI/564 forms an integral part. In such a case, before the a.g.c. voltage can develop, the signal will have been considerably limited with probable loss of syncs. Without a sync-signal input, a.g.c. bias is not developed and control is lost. If the input signal is repetitive in character, the circuit endeavours to produce an a.g.c. bias from parts of the picture signal and the unit may stabilise, along with other associated units^{1,3}, in an entirely spurious condition. To prevent this, TR15 (normally on) is cut off immediately on the arrival of the high-level signal. The base of TR17 then goes to the potential of the supply line, approximately 25 volts positive, and this potential is passed via D11 to TR16 and the output, thus biasing the associated controlled units to minimum gain. The input to the UNI/564 is reduced and TR15 starts to conduct again. As its collector potential falls D9 becomes reversed biased and C18 starts to discharge through TR17, delaying the restoration of automatic control for approximately 1 second.

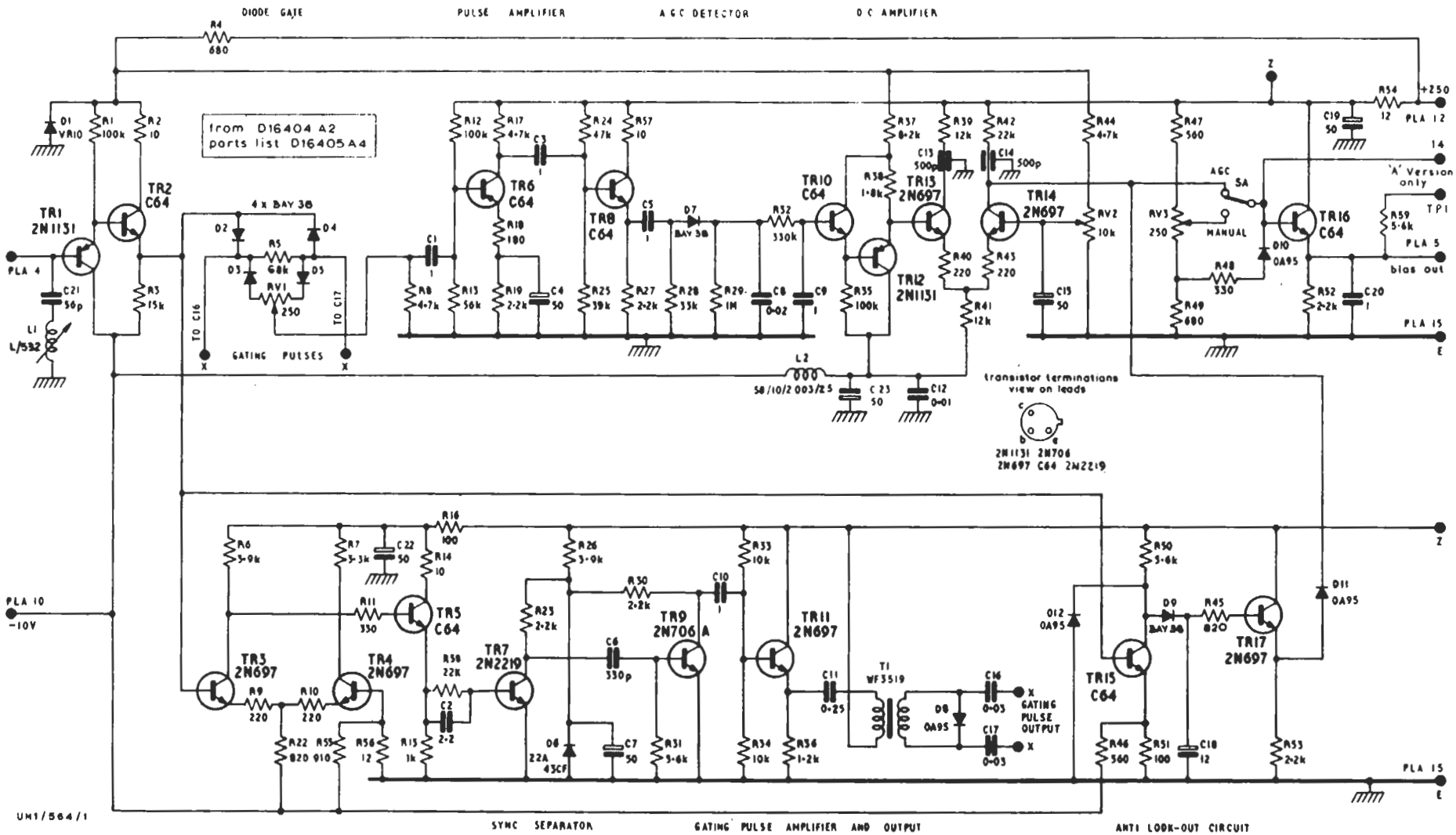


Fig. 1. Circuit of the UN1/564

UN1/564/1

from D16404 A2 parts list D16405A4

transistor terminations
view on leads

2N1131 2N706
2N697 C64 2N2219

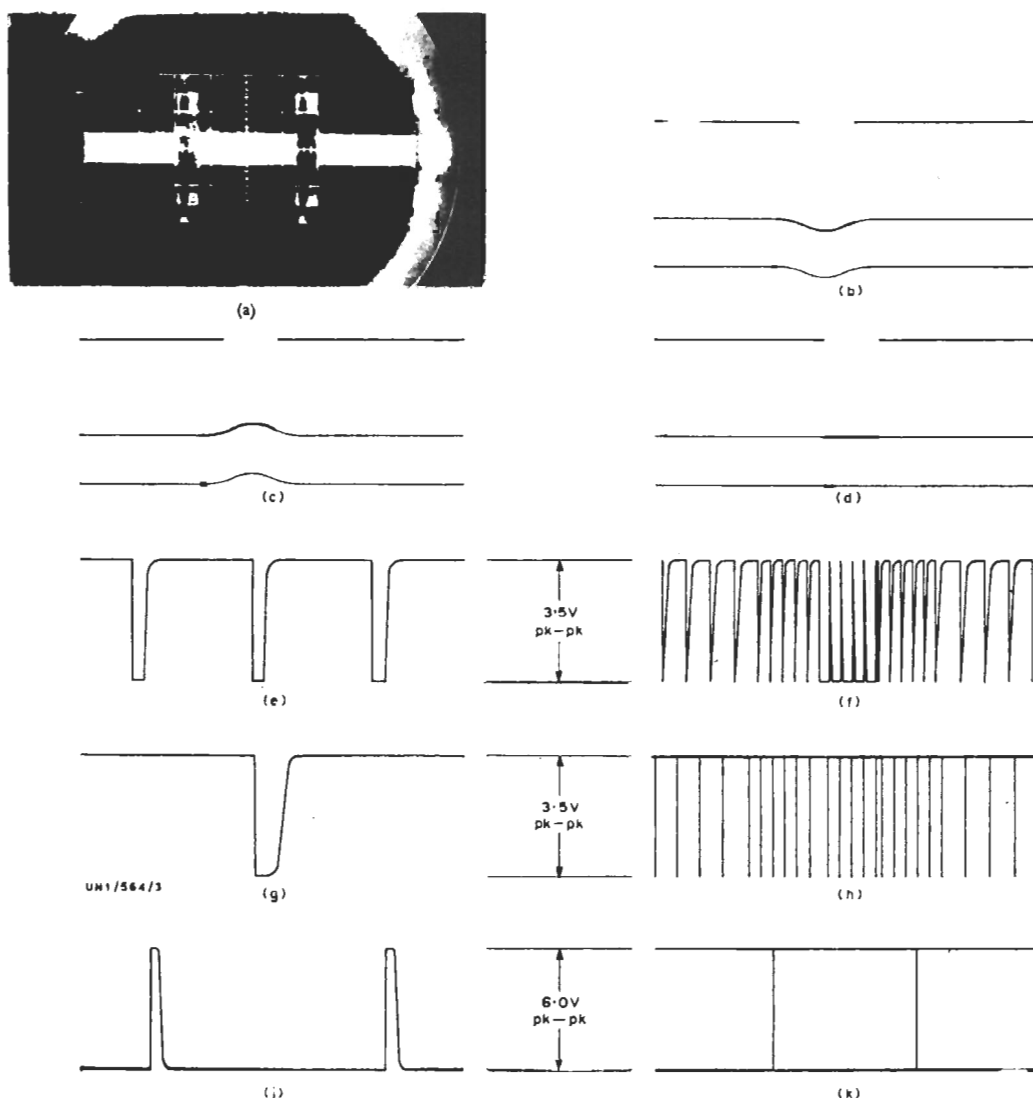


Fig. 2 Waveforms in the UNI/564

- (a) Modulated i.f. waveform with 20% residual carrier
- (b) and (c) Waveforms at the receiver; output with RVI adjusted incorrectly
- (d) Receiver output with RVI adjusted correctly
- (e) Line syncs at collector of TR7
- (f) Field syncs at collector of TR7
- (g) Line pulse at collector of TR9
- (h) Pulses at collector of TR9 during frame-sync period
- (i) Pulses at collector of TR6 displayed at line rate
- (j) Pulses at collector of TR6 displayed at picture rate

Maintenance

Routine maintenance is not required. If faults occur, the unit must be tested in its normal position in the receiver¹; Fig. 2 indicates the waveforms to be expected at various points.

References

1. Television U.H.F. Receiver RC5M/501
2. Vision Demodulator DM2/504
3. Vision I.F. Amplifier AM1/543
4. Designs Department Specification 6.115(66)
AIB 10/68