COLOUR WAVEFORM PROCESSOR UN1/576

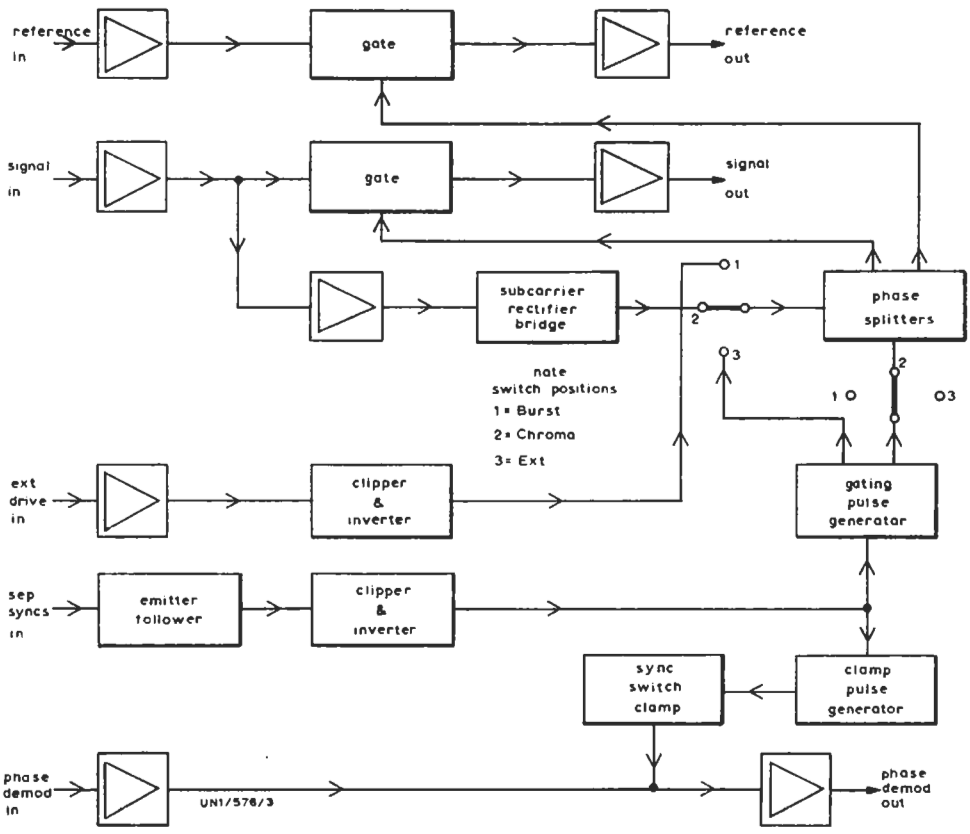

Fig. 1 Simplified Block Diagram of the UN1/576

Introduction

This unit is used in conjunction with a Signal Analyser UN1/541 and normally forms part of a remote signal analyser[1]. It gates out the unwanted portions of the signal applied to the UN1/541 and clamps the phase-demodulated output of that unit.

The inputs to the UN1/576 are:

a staircase-plus-subcarrier non-linearity test signal[2]

a reference subcarrier signal[3]

separated sync pulses[4]

gating pulses

the phase-demodulated output of the UN1/541

The outputs from the UN1/576 are:

gated staircase-plus-subcarrier

gated reference subcarrier

the phase-demodulated output of the UN1/541, with the negative peaks clamped at zero volts.

The unit is constructed on a CH1/12A chassis with index-peg positions 2 and 6. Located on the front panel of the unit is a gating-selection switch, labelled *Burst/Chroma/Ext*, and a reference subcarrier *Phase* control. The unit requires power supplies at + 6 volts and −6 volts[5].

General Specification

Inputs

Signal	5-step non-linearity test signal with 140 mV of correctly-blanked subcarrier on each step
Reference	1 V p-p subcarrier (4.43 MHz)
Mixed Syncs	2 V p-p negative going
External Drive (Gating Pulses)	2 V p-p
Output of UN1/541	phase-demodulated waveform
Input Impedances	high w.r.t. 75 ohms

Outputs

Gated Signal	—
Gated Subcarrier	—
Phase-demodulated output of UN1/541, clamped	—
Output Impedances	75 ohms
Operating Temperature	0—45 °C

Circuit Description

A simplified block diagram which shows the signal paths through the unit is given in Fig. 1, on page 1. The circuit diagram is given in Figs. 2 and 3. Fig. 2, on page 3, shows the reference subcarrier path, the signal path, the subcarrier rectifier bridge and the gating pulse phase-splitters; the remainder of the circuit is shown in Fig. 3. Typical waveforms at various points in the circuit are given in Fig. 4; the line-blanking period of the input signal (a) is included for timing comparison.

Reference Path

The reference subcarrier signal is applied via an amplifier stage and a variable phase-shifting network to a bridge circuit, comprising diodes D2 to D5, which functions as a gating stage. Preset resistor R2, in the base circuit of transistor TR1, is adjusted on test to bring the gated portion of the signal to zero volts.

The positive and negative junctions of the gating bridge are fed with line-frequency gating pulses from the phase-splitter TR12. When the gating-selection switch is set to *Burst* the diodes are reverse-biased for the duration of each pulse and pass the subcarrier signal on to the following stage; for the remainder of the line period the diodes are forward-biased and the subcarrier signal is gated out. When the gating-selection switch is set to *Chroma* the pulses applied to the phase-splitter are reversed in polarity and the subcarrier is gated out only for the duration of each burst; i.e. during the line-blanking periods. The normal *Ext* condition is similar to *Chroma*.

The gated subcarrier is applied via a complementary emitter-follower stage to the reference subcarrier output. The gain of the reference path at subcarrier frequency is 0 dB $\pm$0·2 dB.

Signal Path

The signal path is similar in circuit configuration to the reference path described above with the exception of the band-pass transformer L5 (pass-band centred on subcarrier frequency) which is interposed between the input amplifier and the gating stage. Gating pulses are derived from transistor TR13.

In addition to feeding the gating stage the signal developed across the secondary winding of L5 is applied also (via the amplifier stages TR9 and TR10, and another tuned transformer) to a full-wave bridge circuit comprising diodes D13 to D16 which rectifies the chrominance component of the signal. When switch SA1 is set to *Chroma*, the negative junction of this bridge is connected to the inverter stage TR11; the waveform at this point is shown in Fig. 4(b). Thus the rectangular waveform developed at the collector of TR11 will be negative-going during those portions of each line period that do not contain chrominance information; i.e. the line-blanking period with the exception of the back-porch colour burst. This signal is then combined with the output of the gating-pulse generator to suppress the burst waveform, as shown in Fig. 4(c), and applied to the gating pulse phase-splitters TR11 and TR12.

Gating and Clamp Pulse Generators

Gating pulses are derived either from separated sync pulses or from an external drive source. Clamp pulses are always derived from separated syncs.

The external drive pulses are applied via a complementary feedback amplifier, a diode clipper and an inverter stage to the *Ext* position of switch SA1. When the unit is working in the *Ext* condition the pulses are inverted again by TR11 and applied to the phase-splitters TR12 and TR13; see Fig. 4(e).

Separated sync pulses are applied via an emitter-follower and a diode clipper to the inverter stage TR21. Two outputs are taken from this transistor;

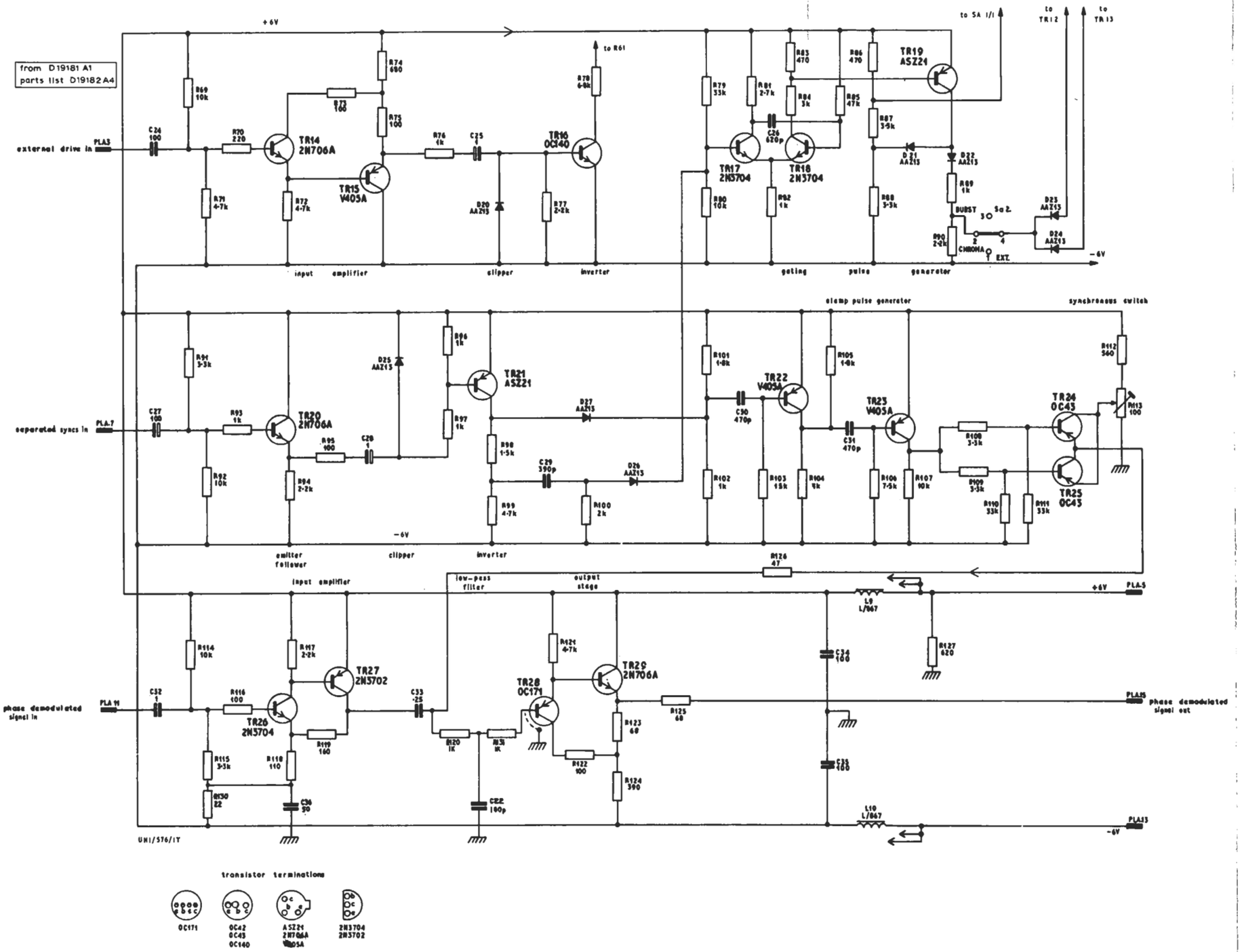

Fig. 2 Circuit of the UN1/576: Sheet 1

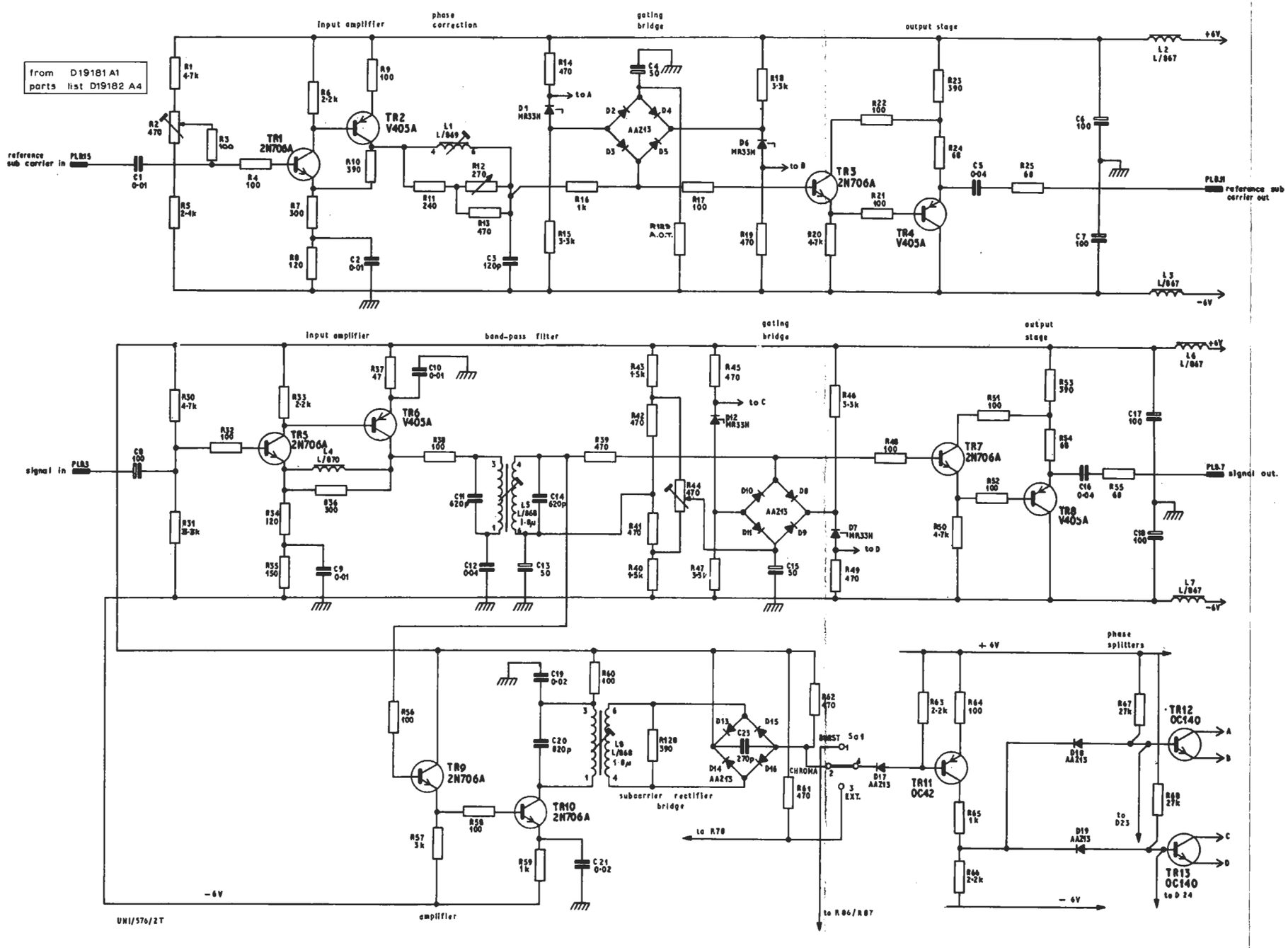

Fig. 3 Circuit of the UNI/576: Sheet 2

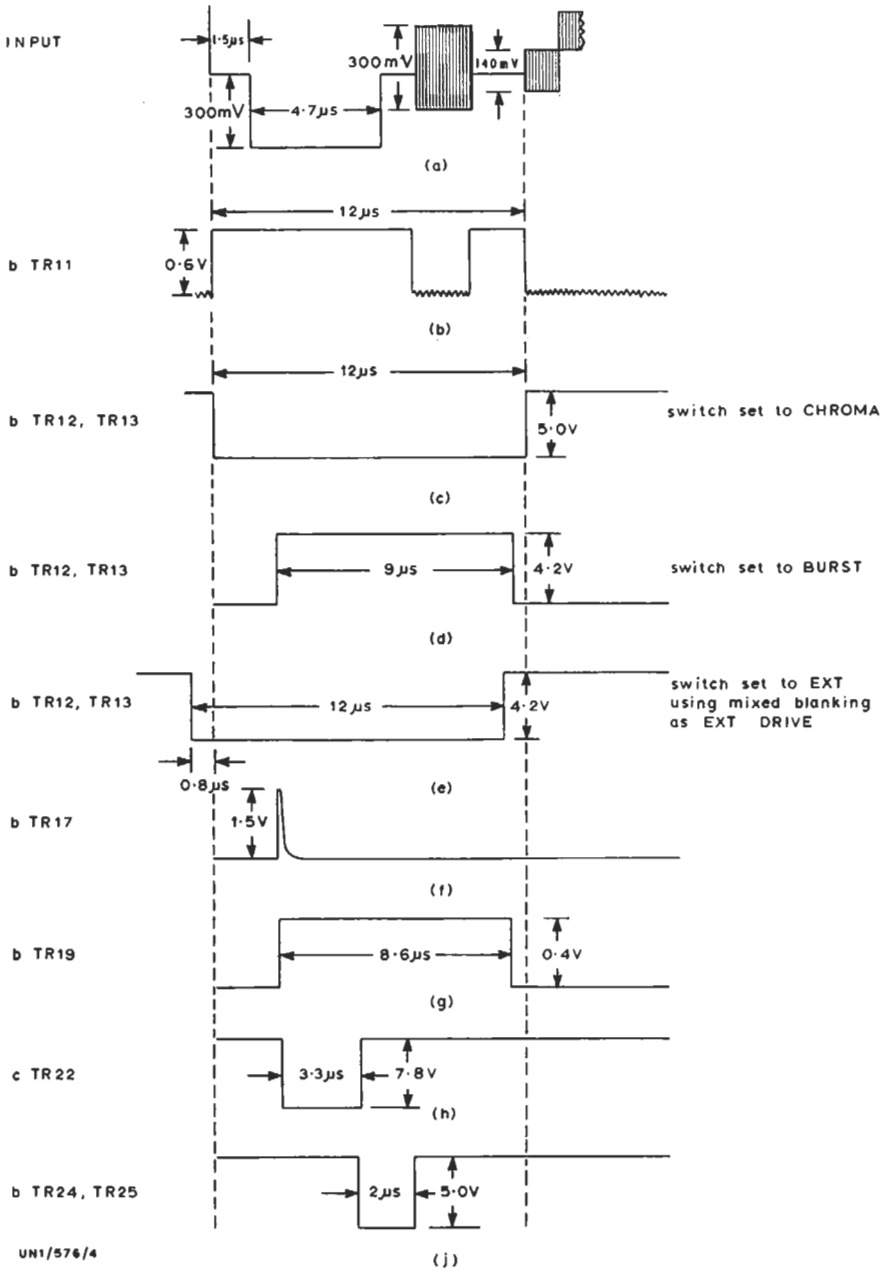

Fig. 4 Typical Waveforms in the UN1/576

one is applied via a differentiating network and a negative-transient clipper to transistor TR17, see Fig. 4(f), which forms part of the gating pulse generator; the other is applied via a diode, which clips the negative-going extremity of the waveform, and a differentiating network to TR22 which forms part of the clamp pulse generator.

Transistors TR17 and TR18 form a monostable multivibrator which functions as a gating pulse generator. The generator output, see Fig. 4(g), is applied via the inverter stage TR19 to the *Burst* position of SA1 and the *Chroma* position of SA2. The waveform produced at the bases of the phase-splitters TR12, TR13 when the gating-selection

switch is set to *Burst* is shown in Fig. 4(d). The pulse applied to the phase-splitters via SA2 fills the hole in the *Chroma* gating pulse caused by the back-porch subcarrier burst; see Fig. 4(b).

The clamp pulse generator comprises transistors TR22 and TR23. Each of these pulse-shaping transistors is preceeded by a differentiating network. The waveform at the collector of TR22 is shown in Fig. 4(h) and the waveform applied from TR23 to the synchronous switch transistors TR24 and TR25 is shown in Fig. 4(j). The synchronous switch clamps the phase-demodulated signal at a level, nominally zero voltage, determined by the setting of R113.

Phase-demodulated Signal Path

The phase-demodulated input signal is fed to a complementary feedback amplifier comprising transistors TR26 and TR27. The output of this amplifier is capacitor-coupled to the following stage and the signal is clamped at the junction of C33 and R120 by clamp pulses derived from the synchronous switch. The clamped signal is then applied, via a low-pass filter which removes unwanted high-frequency components, to the complementary emitter-follower output stage formed by transistors TR28 and TR29.

Maintenance and Alignment

See under parent unit[1]. Note that the UN1/576 carries two plug-in connectors; therefore for maintenance purposes it requires either a chassis extender CH1A/3A or chassis extenders CH1A/1 and CH1A/2.

References to Typical Associated Equipment

1. Remote Signal Analyser EP1L/508.
2. Non-linearity Test Signal Generator GE4/520.
3. Burst-locked Oscillator OS1/502.
4. Sync Separator UN1/540.
5. Stabilised Power Supplier PS2/21B.

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