BINARY STORE UN1/578

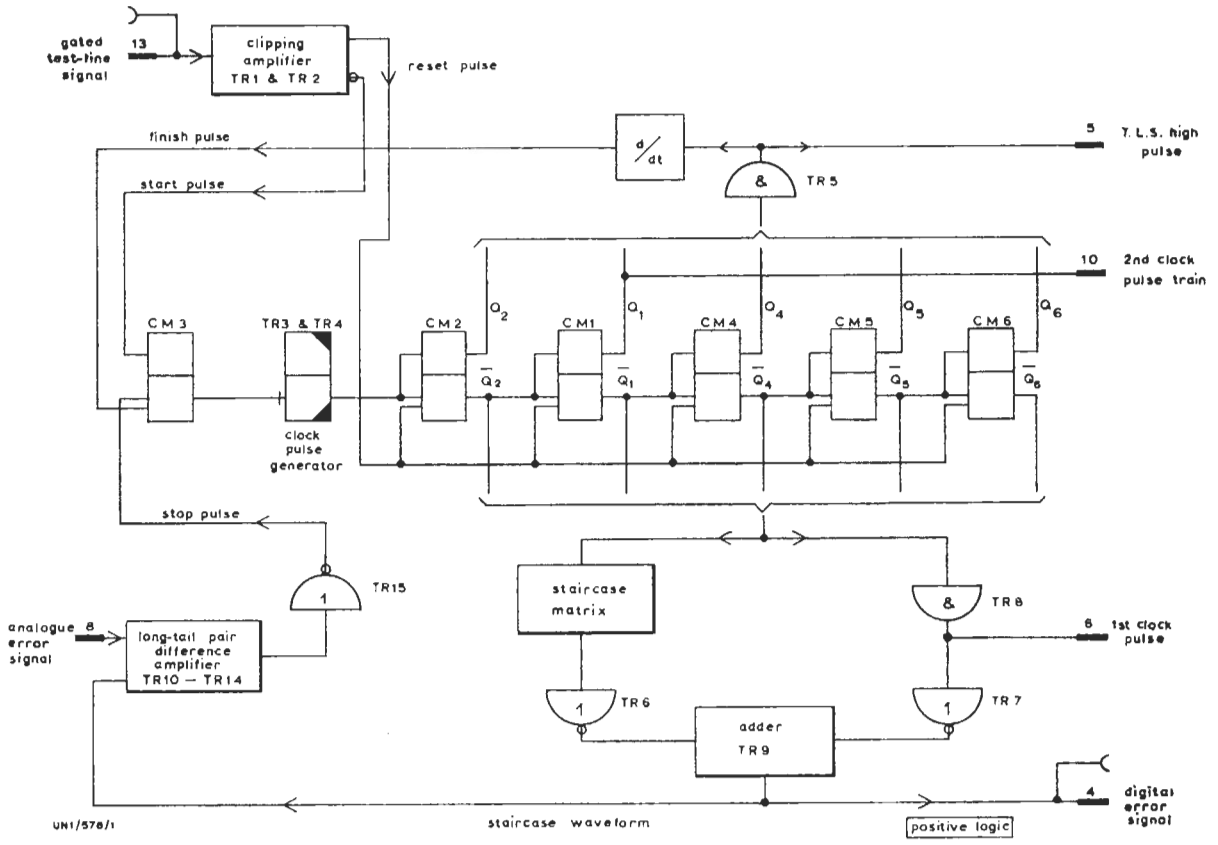

Fig. 1 Block Diagram of the UN1/578

Introduction

The UN1/578 accepts a gated portion of the test-line signal and an analogue error signal: it produces a digital error signal and three pulse outputs in combinations which are related to the permissible range of level of the analogue error signal input. The outputs are repeated every field for which there is a gated test-line signal. If this input is removed the digital error signal remains fixed in level.

The UN1/578 contains six UN9/528 bistable circuits and is constructed on a CH1/12A chassis with index-peg positions 3 and 43.

General Description

A block diagram of the UN1/578 is shown in Fig. 1 and some of the waveforms found in the unit are given in Fig. 2. The unit is built around a five-stage binary counter CM2 to CM6 fed with clock pulses from an astable multivibrator. The clock-pulse generator is inhibited by a bistable multivibrator in the reset condition.

Gated white-level bars from test-line signals are clipped and amplified in a long-tailed pair amplifier. Positive-going bars (reset pulse) Fig. 2(a) switch the counter stages into the reset condition. Inverted

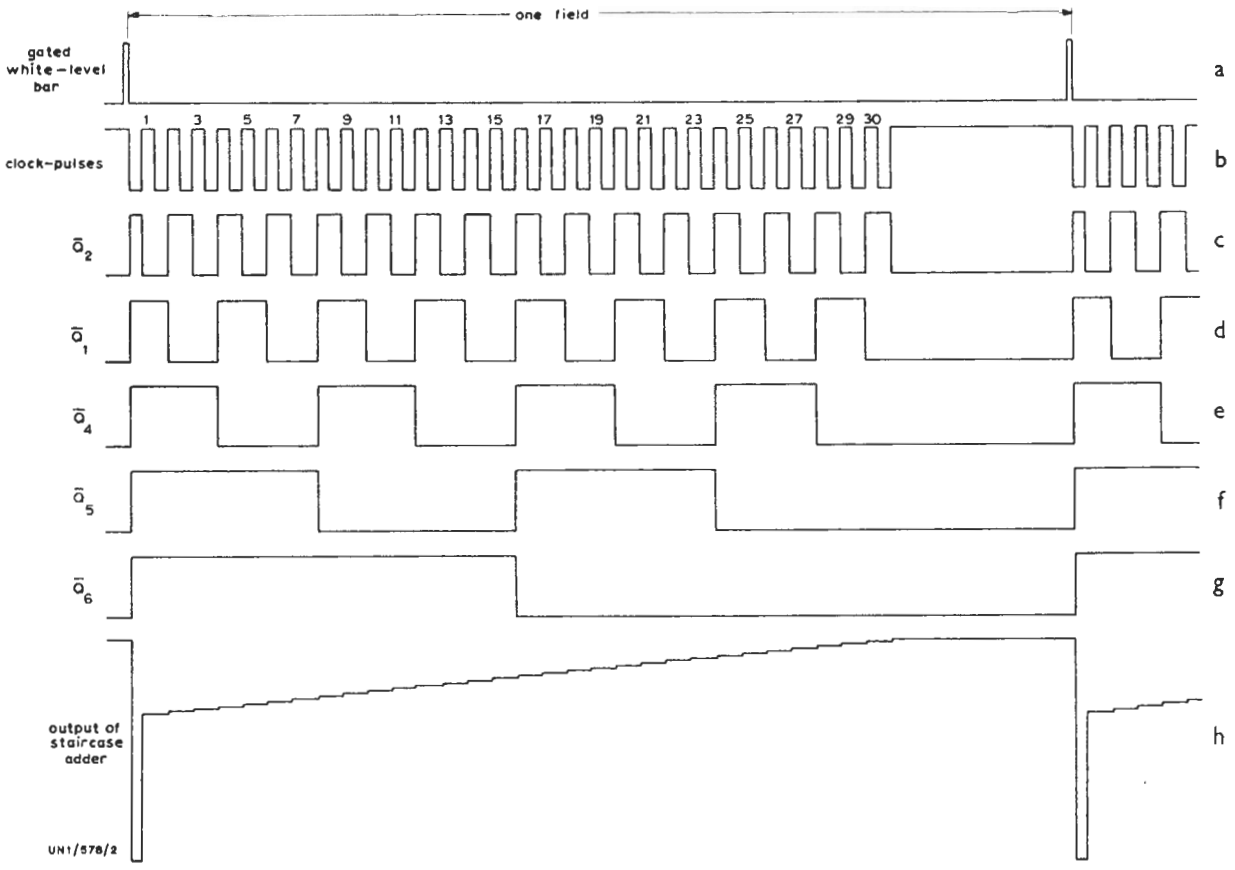

Fig. 2 Waveforms in the UN1/578

bars (start pulse) switch bistable circuit CM3 into the set condition, thus switching on the clock pulse generator. At the 31st clock pulse, the output of the upper AND gate (TR5) produces a finish pulse which puts bistable circuit CM3 into the reset condition and inhibits the clock-pulse generator.

Outputs from the counter stages are matrixed as shown in Fig. 3 to produce an inverted staircase waveform. The outputs are also fed to the lower AND gate (TR8) to produce a pulse which is added to the staircase waveform, Fig. 2(h).

The staircase waveform is fed, together with the analogue error signal input, to a long-tailed pair difference amplifier which produces a negative-going transition when the staircase waveform exceeds the analogue error signal. This transition is inverted (stop pulse) and fed to bistable circuit CM3 to switch it into the reset condition. This inhibits the clock pulse generator and stops further increase of the staircase waveform.

Thus the digital error signal is a truncated staircase waveform with an amplitude just greater than the analogue error signal and which is stored until the next white-level bar. In the event of the test-line signal being removed this stored level is maintained.

Circuit Description

A circuit diagram of the UN1/578 is given in Fig. 4 on page 5. Most of the circuit description is adequately covered in the General Description but the following points should be noted.

Transistors TR3 and TR4 are in the clock pulse generator which is an astable multivibrator with a period of 0·5 ms. Diode D1 enables bistable circuit CM3 to inhibit the generator by cutting off transistor TR3.

Both AND gates are diode gates with emitter follower output stages. The input to emitter follower TR8 is clipped by diode D16 at a voltage determined

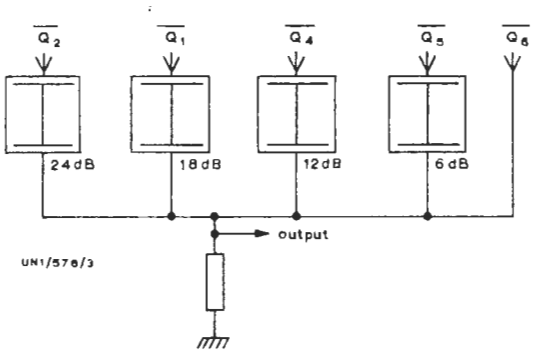

Fig. 3 Addition of Pulse Trains to Form a Staircase Waveform in the UN1/578

by zener diode D15. The output of this transistor is prevented by diode D9, from being fed back to transistor TR6. Zener diodes D7 and D8 are used to set the d.c. levels in the staircase waveform.

Zener diode D17 sets the current for the long-tail pair difference amplifier which includes transistors TR10 to TR14.

Diode D18 removes any positive-going transition in the waveform from the collectors of transistors TR10 and TR11.

Test Procedure

The UN1/578 is tested as part of its parent unit.

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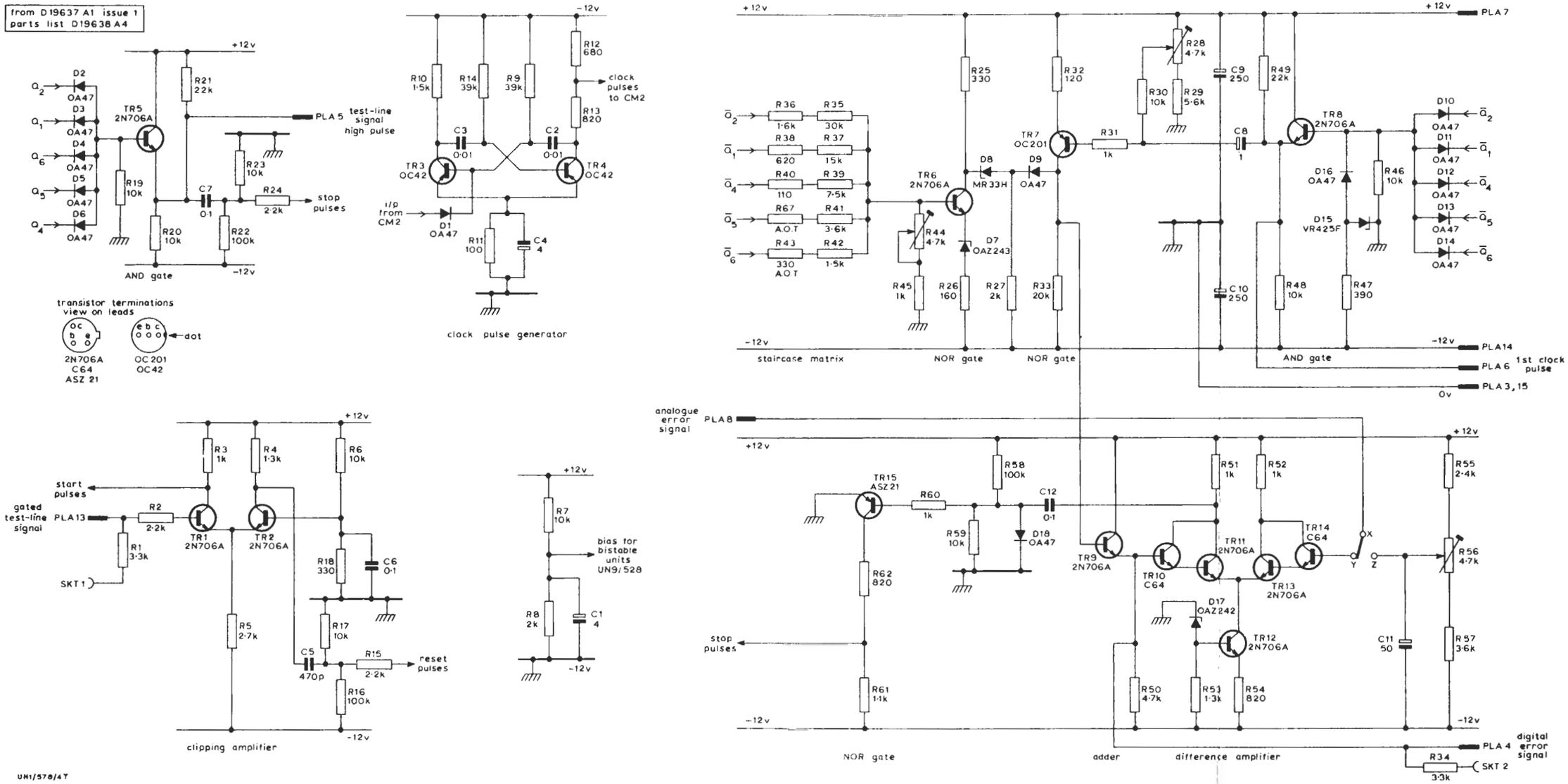

Fig. 4 Circuit of the UN1/578