ERROR SIGNAL UNIT UN1/579

Introduction

The UN1/579 accepts inputs of a video signal, mixed sync pulses, test-line trigger pulses and a digital error signal: it produces two error signal outputs and two outputs of a gated portion of the test-line signal.

The UN1/579 is constructed on a CH1/12A chassis with index-peg positions 2 and 42.

Test-line trigger pulses are fed to a logic circuit which samples the bar in the test-line signal on the second of each successive pair of fields for which there is a trigger pulse. Waveforms found in this circuit are given in Fig. 2.

Circuit Description

The circuit diagram of the UN1/579 is given in

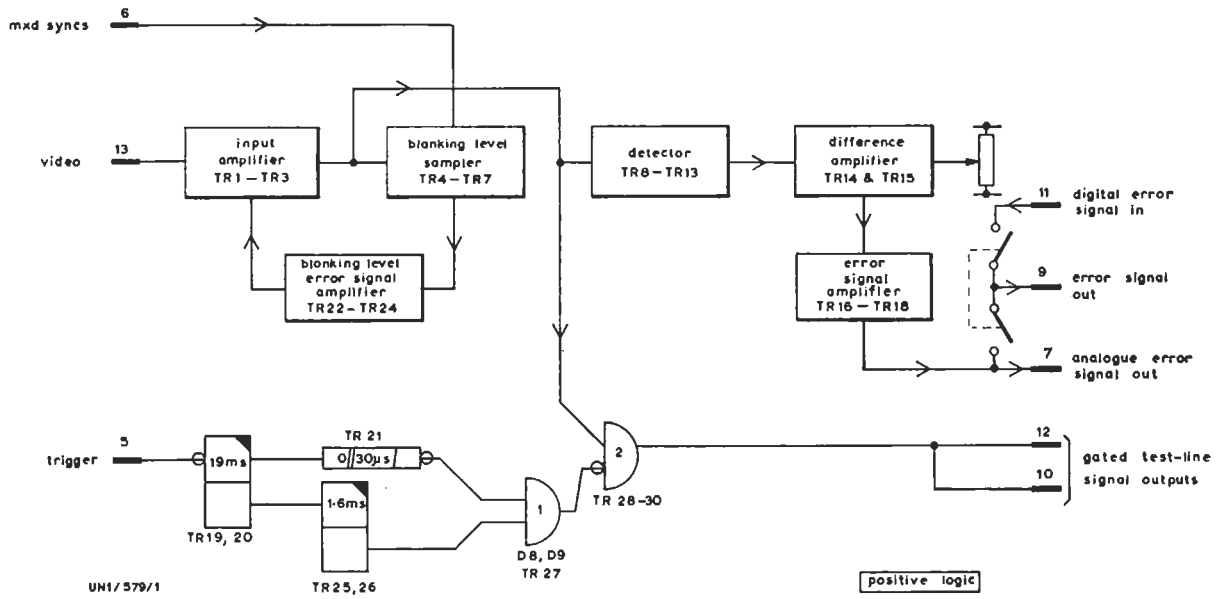

Fig. 1. Block Diagram of the UN1/579

General Description

A block diagram of the UN1/579 is given in Fig. 1. The amplified video input signal is sampled during the back-porch period by pulses derived from the mixed sync pulse input. The sample of blanking level is amplified and fed back to the input amplifier to stabilise the blanking level of the signal fed to the detector. The output of the detector is related to the maximum level of the video input signal. This level does not normally exceed the white-level which occurs during the test-line signal. The output of the detector is compared with a reference voltage in a difference amplifier which produces an analogue error signal.

Fig. 3 on page 3. The input amplifier, which includes transistors TR1 and TR2 connected as a complementary Darlington emitter follower, feeds a band-stop filter used to reduce the level of any chrominance signal. This is followed by transistors TR3 to TR5 which form part of a three-stage negative-feedback amplifier.

The emitter follower TR8 of the detector has a thermistor in its base circuit to compensate for temperature drift in the detector. The detector is made up of two stages each of which comprises a diode (D1 or D3), a capacitor (C9 or C10) and a complementary Darlington emitter follower. Diode D2 provides an additional charging path for

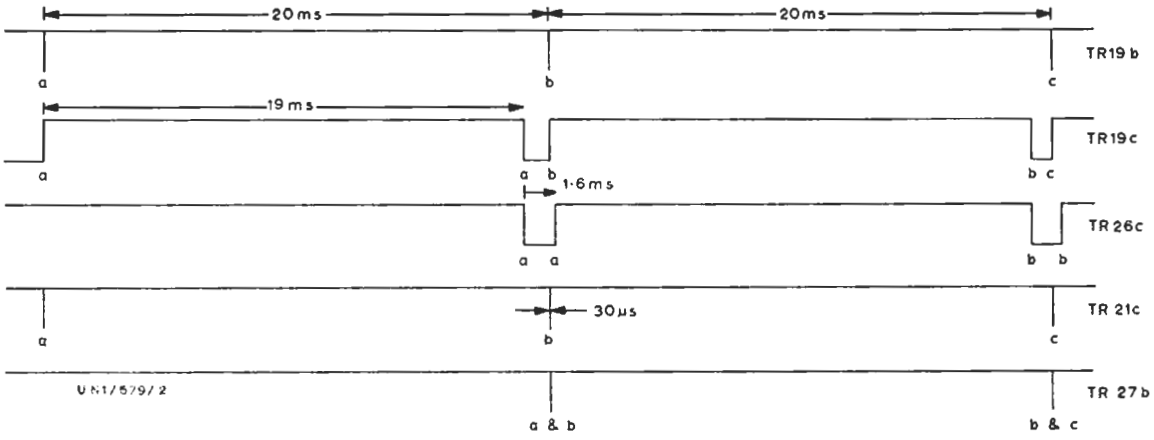

Fig. 2. Waveforms in the UN1/579

capacitor C9 when the unit is switched on.

D.C. negative feedback is provided in the error signal amplifier from the emitter of transistor TR18 to the emitter of transistor TR16. Signal negative feedback is also provided from the collector of transistor TR18 to the base of transistor TR14 in the difference amplifier. This feedback restricts the amplitude-frequency response of these amplifiers to frequencies below 100 Hz.

Diode D11 is a catching diode to assist the recovery time of the circuit, after a reduction of the input video signal level, by preventing the emitter of transistor TR18 from becoming negative. Diodes D4 and D5 prevent interaction between the output of the error signal amplifier and the digital error signal input. The error signal output is the more positive of these two signals.

Mixed sync pulses are differentiated and fed via a common-base transistor TR7 to the base of a switching transistor TR6. The sampled video waveform, integrated in resistor R20 and capacitor C4, is fed via a three-stage d.c. amplifier (transistors TR22 to TR24) to the base of transistor TR3.

In the logic circuit capacitor C20 discharges via the back resistance of diode D10 if the trigger pulse input fails. When the trigger pulses are reapplied capacitor C20 is recharged and this delays the start of the gated test-line signal output.

Test Procedure

The UN1/579 is tested as part of its parent unit.

MJR 2/68

from D19647A1 issue 2
parts list D19648 A4

3

+12
SKT A Sig.In
PLA 13 Video Inputs 2Vpp.
R1 5·3K
C1 100
R5 1K
R4 47K
TR1 C64
TR2 2N1131
R8 68
L1 L/866
L.P. Filter
C2 4
R89 A.D.T.
R11 6·2K
R12 100
TR3 V205
R13 51
R14 910
C3 39p
R15 5K
R16 150
TR4 2N706A
R17 150
TR5 2N697
R18 390
R19 750
R20 820
C5 01
C4 22
R21 10K A.D.T.
R23 2·2K
R22 620
TR6 OC140
C7 1
R24 1·5K
TR7 2N706A
C6 680p
R2 100K
R6 110K A.D.T.
R7 100K
R9 510
R10 75
SKT B Mixed Sync In
R3 5·6K
-12
Input Amplifier
Slanking Level Sampler
R25 470
TR8 2N706A
D1 OA10
TH1
R27 4·7K
R28 220
C8 100
D2 OA10
R29 2·2K
C9 ·022
TR9 C66
TR10 2N1131
D3 OA10
R30 2·2K
C10 01
TR11 2N930
TR12 OC200
TR13 OC200
R34 560
TR14 OC202
R35 560
TR15 OC202
Detector
Difference Amplifier
Reference
R38 2·2K
R39 1K
R37 1·3K
R41 200
TR16 OC202
TR17 2N706A
TH2
C11 25
R43 3·6K
R44 33K
C12 ·1
R47 100
TR18 2N706A
D11 OA47
R48 22K
R49 2·2K
C13 8
D4 OA10
SA1
SA2
D5 OM10
R33 1K
Set Picture Amplitude
R50 5·6K
R51 5·6K
C14 1
R54 910
R40 330
R42 5·6K
R45 150
Error Signal Amplifier
Loop Switch
Close ⟷ Open
+12
R55 3·3K
SKT C
R52 510
R56 3·3K
SKT D
PLA 9 Analogue Error Sig Output to AMF/552
PLA 11 Digital Error Signal Input from UNI/578
PLA 7 Analogue Error Signal Output to UNI/578
-12
PLA 6 Mixed Sync Input
R65 24K
D6 BZY88/C5V6
R69 560
R64 39K
TR22 2N706A
TR23 OC202
TR24 OC202
R66 330
R67 1·6K
R69 2K
R70 2·7K
BL Error Signal Amp
R57 1K
C16 ·002
TR21 OC201
C15 ·047
TR20 OC202
R59 33K
R58 1·8K
TR19 2N706A
19ms Monostable Multivibrator
R60 7·5K A.D.T.
R61 1K
R62 15K A.D.T.
R63 1K
D7 CG61
TLS Gate Pulse Gen
R71 1K
R74 150
TR25 OC42
TR26 OC42
C17 ·01
16ms Monostable Multivibrator
R76 3·9K
D8 CG61
D9 CG61
R79 22K
R80 2·2K
C18 1
R78 470
R81 12K
R82 10K
C19 01
TR27 OC42
OR Gate
TR28 2N706A
R84 1K
R85 4·7K
TR29 OC140
R83 1·5K
R86 4·3K
D10 OA202
C20 0·1
TR30 2N706A
C21 100
R87 2·2K
R88 100K
C22 250
C23 250
PLA 3.15
PLA 12 Gated TLS Output 2
PLA 10 Gated TLS Output 1
-12 PLA 14.4.
TLS Trigger Input
PLA 5
TLS Gate

Transistor terminations view on leads

2N706A	OC140
C64	OC200
V205	OC202
2N697	OC42
2N5131	OC201
2N930	

Fig. 3. Circuit of the UN1/579