VIDEO ERASE UNIT UN1/608 AND UN1/608A

The UN1/608 removes picture or inserted test signals from selected lines in a 625-line video signal during the period 9 to 62·5μs after the leading edge of sync pulses. The erasure is achieved by switching an internally generated black level voltage to the output during the required erase period. Fig. 1 is a block text diagram of the unit. The UN1/608 and UN1/608A differ only in their output stages to provide alternative output impedances.

The unit is constructed on a CH1/12A chassis with index peg positions 28 and 35.

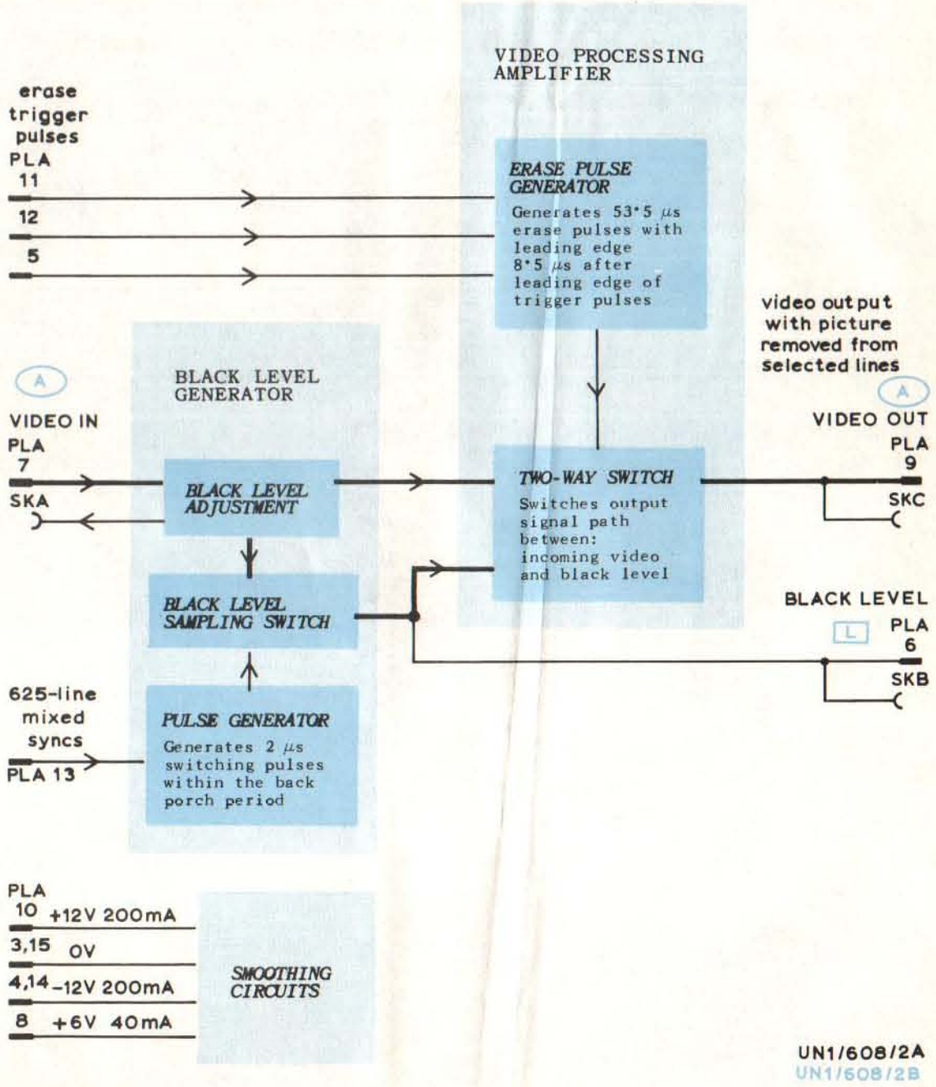

Fig. 1 Block Text Diagram

General Specification

Inputs

Video.	1V p-p (+4dB to -6dB), 7·5kΩ input impedance.
Mixed Syncs:	4V p-p
Trigger Pulses:	5V p-p, +ve or -ve going pulses the leading edges of which are coincident with the leading edges of the line-sync pulses of the lines to be erased.

Video Outputs

UN1/608:	0±0·1 dB across 75Ω
UN1/608A:	0±0·1 dB across 64Ω
Differential Phase:	Less than ±0·15°
Differential Gain:	Less than ±0·3%
k rating:	Less than 1%
Level of erase trigger pulse spikes on video at 9 and 62·5μs:	Less than 15mV
Timing error between the negative edges of mixed syncs and the video signal:	Less than 0·2μs
Black Level Output:	Nominally 0V

MH 4/72

The remainder of this Instruction comprises the following:

This Technical Instruction is prepared in a new form of visual presentation. To assist in evaluation and development of the techniques comments are invited and should be sent to:
Head of Technical Publications Section
Wood Norton

BLACK LEVEL GENERATOR

PLA13 — 625 line mixed syncs

IC4d. INVERTER
+ve going output

IC3. MONOSTABLE
Generates line-rate pulses, triggered from the rear edge of syncs. R88 is selected to give pulse duration of 2 ±0·2 μs

TP8

TR11. TR12. LONG-TAILED PAIR
+ve going switching pulse output within the back porch period

TP3

TP9

TR1. TR2. R4
Adds a voltage to the incoming video to adjust the inserted black level. R4 is adjusted to give required level measured at TP5.

TR3. LONG-TAILED PAIR

TR4. TR5. EMITTER FOLLOWER. INVERTER

TP2

SUB-CARRIER REJECTOR
L1 is adjusted for minimum sub-carrier at TP2

TR6. LONG-TAILED PAIR

TR7. TR8. EMITTER FOLLOWER. INVERTER

TR9, TR10, D2. BLACK LEVEL SAMPLING STAGE
+ve going switching pulses turn TR9 on during back porch period and C7 charges to the black level voltage.
TR10 and D2 ensure that TR9 functions over a wide range of input signal levels

TR13. LONG-TAILED PAIR

TR15. TR14. EMITTER FOLLOWER. INVERTER

PLA7 — video input

C1 100

R1 22k

R91 1k

TP1

SKA

VIDEO IN

PLA 6

R92 1k SKB — BLACK LEVEL

R93 1k SKC

PLA9 VIDEO OUT

TP6

VIDEO PROCESSING AMPLIFIER

TR16. BLACK LEVEL SWITCH
Passes black level when gate potential is +ve.
TR17. D4. ensure that TR16 functions over a wide range of input signal levels

TR21. INPUT VIDEO SWITCH
Passes video input signal when gate potential is +ve.
TR20. D5. ensure that TR21 functions over a wide range of input signal levels

TP4

TR22. TR23. LONG-TAILED PAIR

TR24. TR25 COMPOUND EMITTER FOLLOWER

TP5

TP7

PLA11 — insertion trigger pulses

PLA12

PLA5 -ve — trigger inhibit

IC4a.b.c. TRIGGER INPUT STAGE
Produces +ve going erase trigger pulses from a variety of inputs. For output trigger edges coincident with +ve going input edges, PLA5 must be connected to 0V

IC2. MONOSTABLE
Generates +ve going 8·5 μs pulses triggered from +ve going edges.
R84 is selected so that the +ve going edges of TP7 waveform occur 9 ±0·2 μs after the leading edge of syncs

IC1. MONOSTABLE
Generates +ve going 53 μs pulses triggered from -ve going edges of IC2 output.
R80 is selected so that the -ve going edge of TP7 waveform occurs 2 ±0·2 μs before the leading edge of the following sync pulse

TR18. TR19. LONG-TAILED PAIR
Provides two switching pulse outputs.
+ve going switching pulses at TR18 collector during the required erasure period and at TR19 collector during the non-erasure period

UN1/608/1A

SMOOTHING CIRCUITS

+12V

-12V

+5V

Fig. 2A Block Text Diagram

BLACK LEVEL GENERATOR

PLA13 625 line mixed syncs — IC4d — +5V

IC3 MC851p — C15 220p — R85 3·3k — R88 2·2k AOT — R86 2k — R87 9·1k — +5V

TP8

R35 6·8k — R34 12k — R32 18k — R31 3·9k — +12V

R36 13k — TR12 BC108 — TR11 BC108 — R33 2·7k AOT — D1 MR33C-H — R37 3·9k — −12V — +12V

TP3 TP9

PLA7 video input — C1 100 — R1 22k — R5 2·2k

+12V — R6 39k — R2 5·1k — R4 10k — R9 39k — R3 18k — TR1 BCY72 — TR2 BC108 — R7 10k — R8 10k — −12V

+12V — R10 3·9k — R11 100 — R13 3·9k — C2 200p — TR3 BCY89 — R12 11k — −12V

+12V — R14 120 — R16 75 — TR4 BC108 — TR5 BFX88 — R15 2·4k — R17 470 — −12V

TP2

L1 L/1658 — C4 47p — C3 20p — C5 120p — R18 600

R91 1k — TP1 — SKA — VIDEO IN

+12V — R19 3·9k — R20 100 — R22 3·9k — C6 200 — TR6 BCY89 — R21 11k — −12V

+12V — R23 120 — R25 75 — TR7 BC108 — TR8 BFX88 — R24 2·4k — R26 470 — −12V

+12V — R29 120 — TR10 BC109 — D2 OA200 — R28 1k — TR9 TIS75 — R27 1k — R30 6·2k — −12V — C7 0·1

+12V — R38 3·9k — R39 100 — R41 3·9k — C8 200p — TR13 BCY89 — R40 11k — −12V

+12V — R42 120 — R44 75 — TR11 BC108 — TR15 BFX88 — R43 2·4k — R45 470 — C9 — −12V

PLA 6

R92 1k — SKB — BLACK LEVEL

R93 1k — SKC

PLA9 VIDEO OUT

TP6

VIDEO PROCESSING AMPLIFIER

+12V — R47 120 — TR17 BC109 — R46 1k — D4 AAZ13 — R49 1k — R48 1·1k — TR16 TIS75 — −12V

TP4

R61 1k — TR20 BC109 — R58 120 — +12V — −12V — R59 910 — TR22 TIS75 — R57 1k — D5 AAZ13

R60 22k — C12 100

R66 AOT * — R63 22k — R65 3k — R68 6·2k — TR22 BFY90 — TR23 BFY90 — R62 100 — R64 43k — R67 * — −12V

R69 1·2k — R72 75 — C31 0·1 — TR24 BCY72 — TR25 BFY90 — R73 120 — R76 * — R71 2·2k — R74 * — R70 120 — R75 20 AOT — −12V

TP5

TP7

IC4a — PLA11 insertion trigger pulses — PLA12 — PLA5 −ve trigger inhibit — IC4b MC846p — IC4c — C18 220p — C17 220p — R89 1·8k — R90 1·8k

IC2 MC851p — C14 0·0013 — R81 3·3k — AOT R84 2·2k — R82 2k — R83 9·1k — +5V

IC1 SN74121N — C13 0·0068 — R77 3·3k — AOT R80 2·2k — R79 9·1k — +5V

D7 OA47

+12V — R54 6·8k — R53 5·6k — R51 6·8k — R50 3·9k — C20 120p — R55 13k — TR19 BC108 — TR18 BC108 — D3 MR33C-H — R56 3·9k — R52 910 — −12V

UN1/608/1A

PLA10 +12V — C30 — C10 — +12V — PLA 3,15 — 0V — C11 — C19 — PLA 4,14 — −12V — C16 — PLA8 +6V — D9 — MS2 — 32 — +5V

Transistor termination view on leads

TIS75 — BCY72 BC108 BC109 BFY52 BFX88 — BFY90 — BCY89

view on top — MC851p MC846p SN74121N

*	UN1/608	UN1/608A
R76	75Ω	82Ω
R74	100Ω	82Ω
R66	10kΩ	30kΩ
R67	1·3kΩ	910Ω

positive logic
0 = 0V to +0·4V
1 = +2·4V to +5V

Fig. 2B Functional Circuit Diagram

Test Procedure

Video Output Level

1. Connect a video oscillator terminated in 75 ohms to PLA7 and set it to give 0dB output at 10 kHz.

2. Terminate the video output at PLA9 with the appropriate impedance, UN1/608 75 ohms, UN1/608A 64 ohms (75 ohms in parallel with 430 ohms), and check that the output level is 0±0·1dB. If necessary adjust R75.

3. Reduce the input signal to zero and, with the input and output still terminated, check that the d.c. voltage at TP6 (SKC) is 0V±100 mV. If necessary adjust R66.

4. Set the oscillator to +10 dB at 10 kHz and check that the waveform at TP6 (SKC) is 3V p-p and undistorted.

Inserted Black Level

Check the waveform at TP5 and adjust R4 to give the required inserted black level.

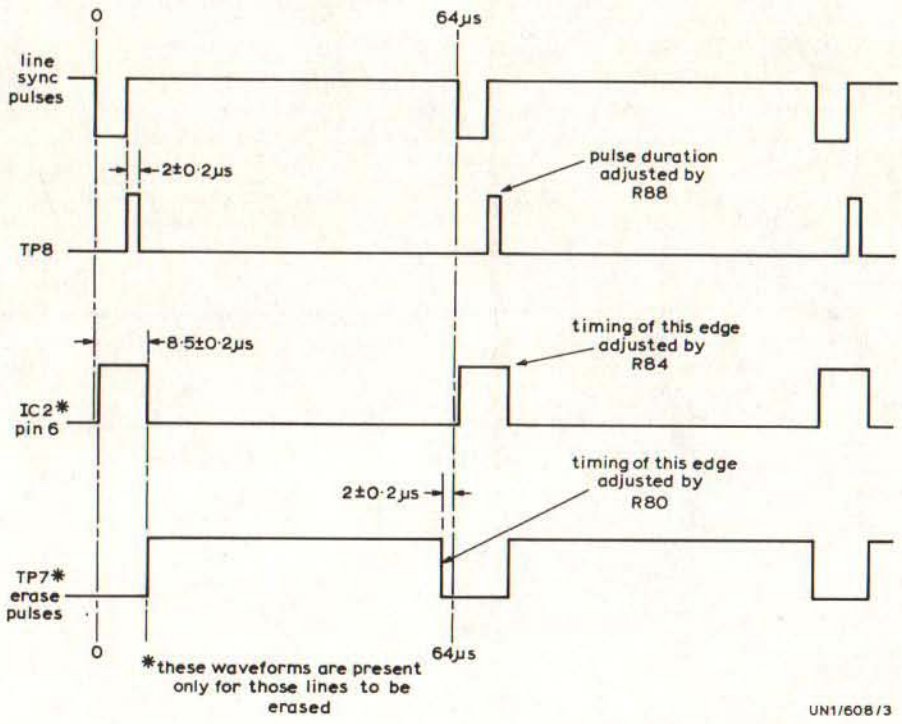

Fig. 3 UN1/608 Waveforms