SCAN UNIT UN1/98

Introduction

The UN1/98 was designed as part of automatic fault reporters PA2M/7A and PA2M/9. The UN1/98 and a scan control unit UN3/16 form the code indicator section (C.I.S.) of the fault reporter, The combination of units has a function similar to that of telephone indicator panel TIP/2. An earth (normal) or open-circuit (fault) condition at an input terminal causes a short or long burst of tone at the output of the associated UN3/16.

Each UN1/98 can monitor up to six inputs. A maximum of five units can be used with the PA2M/7A and 10 units with the PA2M/9.

The UN1/98 is built on a BBC/I.S.E.P. printed wiring board. Segments 19, 25 and 27 are removed from the coding device on the 33-way output connector.

The Group Monitor function indicates that the inputs wired to that group are either all normal or one or more of the inputs is faulty.

The Gap function causes a break of 0·25 second and the Miss a break of 0·015 second. The programme period is 10 seconds long and allows audio signals applied to the UN1/98 to be passed to the UN3/16. The Return function reloads a shift-register so that the whole sequence can be repeated.

Circuit Description

General

Fig. 2 is a circuit diagram of the UN1/98. The unit uses integrated logic circuits which work in a positive logic convention. The logic levels (relative to earth potential) are:

Logic 0	−5·5 to −4·2 volts
Logic 1	−2·5 to 0 volts

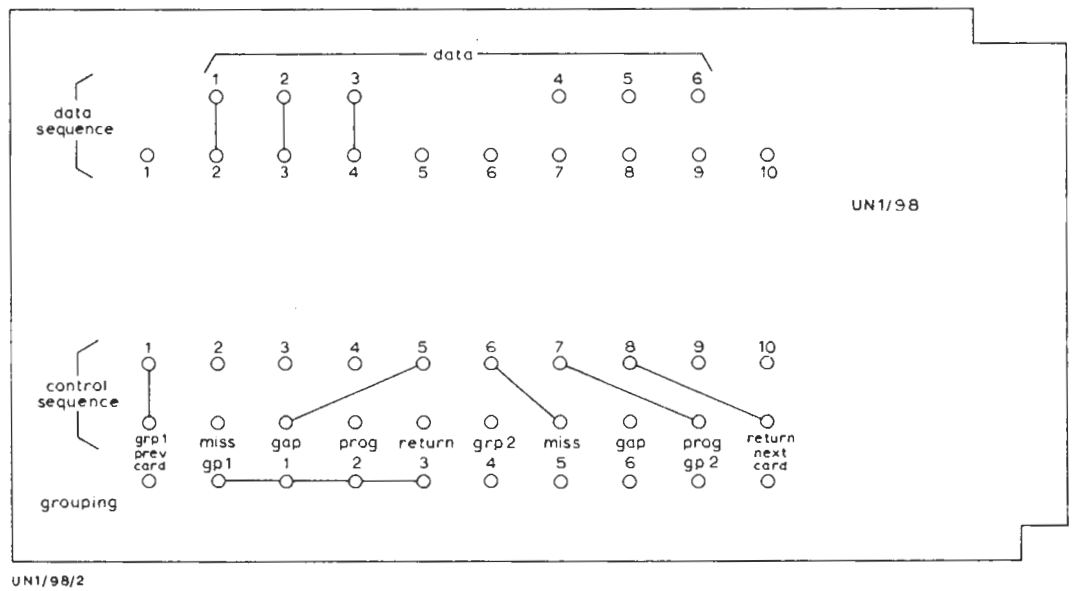

Fig. 1. Layout of Terminals on Printed Wiring Board

General Description

Each individual unit is set up for a particular installation by making suitable connections to terminals on the printed wiring board*. Fig. 1 shows the layout of the terminals which, for the purpose of explanation, are shown wired to provide the following functions:

Group Monitor
Input 1
Input 2
Input 3
Gap
Miss
Programme
Return

*A Guide to Programming the C.I.S., Designs Department Technical Memorandum 2.228(71).

Shift Register

A description of the principles of shift registers is given in Instruction GP.1.

Circuits IC6 to IC10 comprise 10 stages of a 12-bit shift register. The first two stages of the register are in the associated UN3/16. Clock pulses are applied to pin PLA6.

Initially a logic 0 signal is applied to the reset input on PLA5 and the Q-output of each stage of the register is set to logic 0. A logic 1 input to the register is fed via the two stages in the UN3/16 to pin PLA1

and is progressed through the register by the negative-going edge of each clock pulse. The last stage of the register that is used must be connected via an inverting gate to pin PLA22 (Return). This has the effect of putting a logic 1 signal into the first stage in the UN3/16 and thus repeating the whole sequence.

Input Monitor Circuit

Up to six monitored points can be connected to pins PLA11 to PLA16. The normal condition is an earth connection; a fault condition is shown by an open-circuit or 12-volt positive potential. Any input that is earthed causes the associated transistor to be cut off and causes a logic 0 signal to appear at the output of the associated inverting gate.

Programme Circuit

Audio signals applied across pins PLA17 and PLA32 are fed via transformer T1 to the base of transistor TR8. A logic 1 signal applied to transistor TR18 causes it to conduct and pass the audio signal to PLA31. Resistors R7 and R8 serve to maintain a constant d.c. through transformer T1 whatever the state of transistor TR8 and thus avoid switching plops.

Operation

Table 1 shows the logic levels at the outputs for the combinations of inputs.

TABLE 1

Monitor Function		*Shift Register logic 1 at*	*Output*							
			Serial Data (PLA7)	*Serial Reg. (PLA8)*	*Miss (PLA20)*	*Gap (PLA9)*	*Return (PLA22)*	*Group State (PLA18)*	*Prog. Audio (PLA31)*	*Prog. On (PLA30)*
Group Mon.	all inputs normal	IC6 pin 8	0	0	1	1	1	0	off	1
	input 1 faulty	IC6 pin 8	0	0	1	1	1	1	off	1
Input 1	normal	IC6 pin 6	0	0	1	1	1	1	off	1
	faulty	IC6 pin 6	1	0	1	1	1	1	off	1
Input 2	normal	IC7 pin 8	0	0	1	1	1	1	off	1
Input 3	normal	IC7 pin 6	0	0	1	1	1	1	off	1
Gap		IC8 pin 8	1	0	1	0	1	1	off	1
Miss		IC8 pin 6	1	0	0	1	1	1	off	1
Programme		IC9 pin 8	1	0	1	1	1	1	on	0
Return		IC9 pin 6	0	1	1	1	0	1	off	1

Test Procedure

The UN1/98 is tested as part of its parent unit.

LPB7/72.

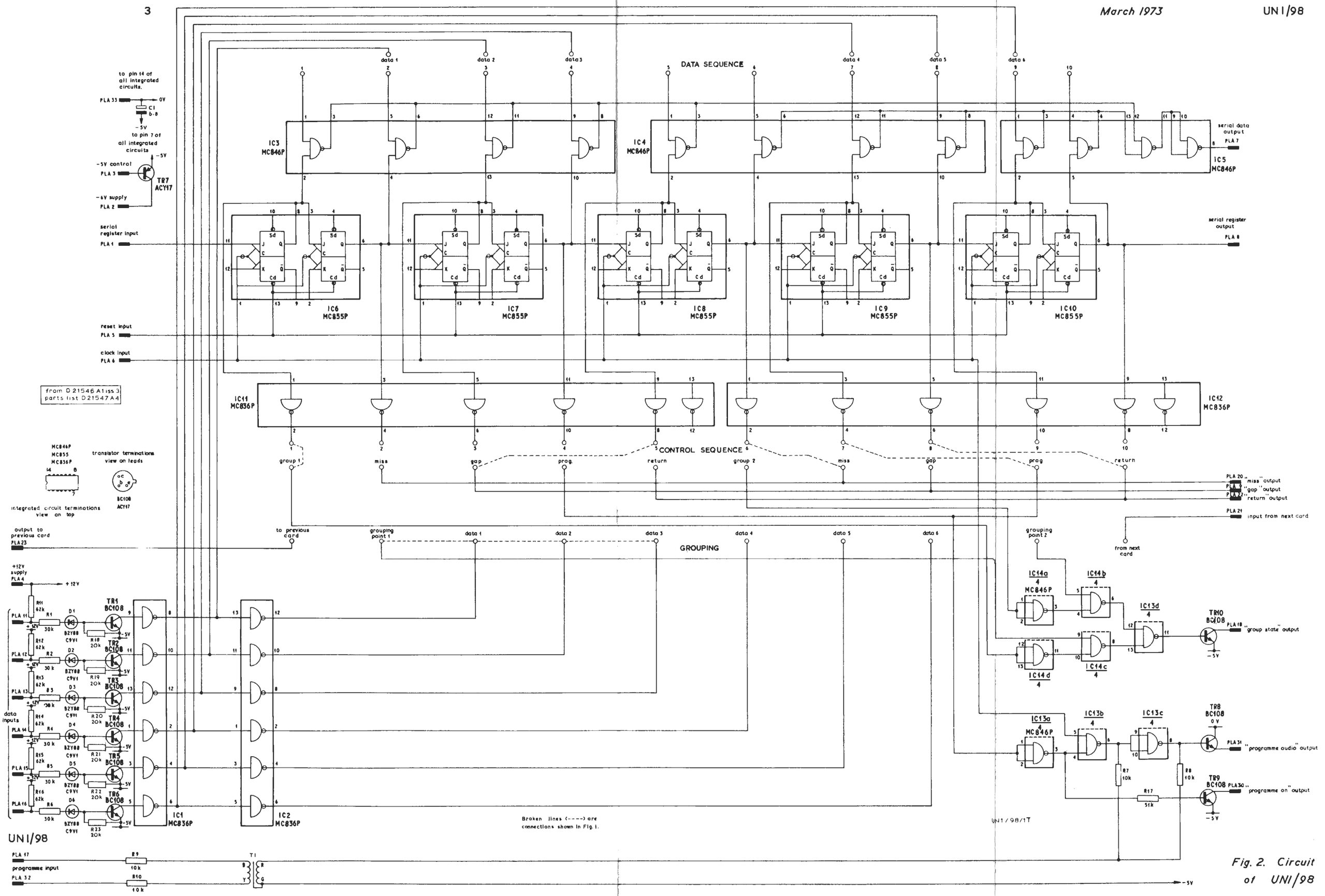

Fig. 2. Circuit of UNI/98