COMPARATOR UNIT UN20/2

General Description

Comparator unit UN20/2 accepts six two-state inputs, each of which may be either −24 volts, representing 'logic value' *0*, or 0 volts (or an open-circuit), representing 'logic value' *1*. Various combinations of input signals light different lamps on the unit and certain combinations also produce an output voltage.

The UN20/2 is used in sound automatic monitors MN2M/2, MN2M/4A and MN2M/6A (and the preceding /4 and /6 versions) for comparing coded signals representing programme levels* at the input and output of a programme link, known as the reference and compared programme levels respectively.

time interval, and by spurious impulsive signals.

The unit comprises two printed wiring cards, A and B, mounted in a chassis CH1/26B having eleven indicator-lamps on the front panel. Card A contains 17 NAND elements and card B contains 16 NAND elements and three output/delay elements. The chassis has indexing pegs in positions 18 and 23.

Lamp Indication (Fig. 5)

Except where the UN20/2 is used in a monitor MN2M/2, the indications given by the 11 lamps just mentioned are as follows. ILP1 to ILP3 show the instantaneous level of the signal at the sending end. ILP4 to ILP8 show the corresponding level at the receiving end. ILP9 (a red lamp) shows a failure in the

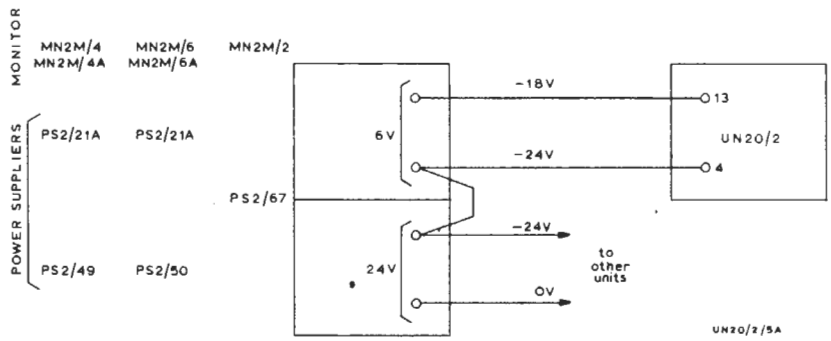

Fig. 1. UN20/2 Power Supply

The unit contains 33 NAND elements and three output/delay elements. Eight of the NAND elements control lamps indicating programme level, three for the reference programme and five for the compared programme. The outputs of these elements are also inverted by eight more NAND elements and taken to another 15 such elements arranged in groups. These are connected so that when the reference and compared programme levels are in the same bands (including the compared programme guard-bands), logic value *0* appears at the input of the output element controlling a green lamp, causing it to light, but when the levels are in different bands the element controlling a yellow lamp is activated instead. A further separate NAND element and output element control a red lamp indicating that the tone signal representing the reference level is not being received. Delay in the output elements is introduced to prevent operation if the signals are separated by only a short

sending end generation of tones, in the transmission path, or in the receiving end tone decoding. ILP10 (a yellow lamp) shows a transmission fault resulting in a difference in sending and receiving levels. ILP11 (a green lamp) shows agreement between sending and receiving levels.

In an MN2M/2 the indications are effectively the same, except that, as there are no monitoring tones, ILP9 is not used.

Circuit Description

The operation of the UN20/2 circuit described here particularly applies to the use of a UN20/2 in monitors MN2M/2, MN2M/4A, and MN2M/6A where the general d.c. supply is −24 volts and the two-state input signals applied to the UN20/2 consist of d.c. potentials at nominally −24 and 0 volts which are fed from processing amplifiers in the AM1M/16 series or tone decoders in the DM1/1 series. As shown in Fig. 1, the UN20/2 employs a 6-volt d.c. supply which is so connected relative to the rest of the monitor that the d.c. rails and two-state signals in the UN20/2 are at −24 and −18 volts with respect to the 0-volt potential in the monitor.

The circuit of the UN20/2 is shown in block form in Fig. 6 at the end of this Instruction. There are six

* The concept of ' programme level ' is introduced here for convenience because it makes the numerical magnitude of programme and tone measurements the same. A *zero programme level signal* produces a peak reading of 4 on a P.P.M. which has been lined up to read 4 on *steady zero level tone*. Zero programme level is thus the same as a programme volume of −8 db.

inputs to the unit, on PLA pins 5 to 10. Signals representing the reference programme level at the input or sending end of the system being monitored are applied to pins 9 and 10, and operate NAND elements A to D on card A. Signals representing the compared programme level at the output or receiving end of the monitored system are applied to PLA pins 5 to 8, and operate NAND elements K to O on card A.

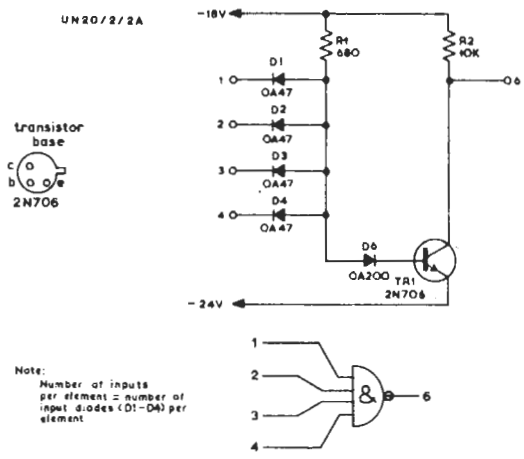

Fig.2. NAND Elements A–T

The NAND elements are transistor diode logic gates connected as in Fig. 2. Each element may have up to four inputs and a fan-out of up to six elements, or of one element and a 40-mA lamp load. If all the inputs to a gate are 0 volts or an open-circuit (both representing logic value *1*), the transistor saturates and terminal 6 is at −24 volts (logic value *0*) neglecting the emitter-collector voltage drop. When one or more inputs are −24 volts, this causes the corresponding diode or diodes, in the group D1 to D4, to conduct and the junction of R1 and D6 develops a potential such that the transistor is cut off. This is because D6 is a silicon diode and has a higher forward voltage drop than the germanium input diodes D1 to D4, thus blocking the parallel path which might otherwise permit a small base current to flow. Provided no appreciable current is taken by the extenal circuit, terminal 6 is at −18 volts (its most positive value, and therefore logic value *1* for this point).

Hence,

(a) when all inputs have the value *1* the output has the value *0*,

(b) with one or more inputs at value *0*, the output is at value *1*.

To understand the action of the gate circuits, consider the effect of programme level on logic values in a monitor system as shown in Fig. 3. This carries the logic signals up to the pins of plug PLA on the UN20/2. From here on the signal path can be followed on Fig. 6.

Suppose the programme level is increasing from below −40 dB toward zero level. Taking the compared programme first, at a level of −40 dB there are inputs at logic value *1* to elements K to O, and pin 6 of element O is at value *0*; lamp 8 therefore lights. Because value *0* on pin 6 of element O is applied as an input to elements K to N, the outputs of all these gates have value *1* (−18 volts) and lamps 4 to 7 are out. As the programme level increases an input of value *0* is applied first to PLA pin 5 (at −38 dB) and then in addition to pins 6, 7 and 8 giving a sequence as shown in Table 1.

For the inputs due to the reference programme, two separate sequences of events must be considered, one for monitor MN2M/2 and another for monitors MN2M/4A and MN2M/6A.

In monitor MN2M/2, the inputs to PLA pins 9 and 10 are derived from an amplifier AM1M/16B and the sequence is as in Table 2.

In monitors MN2M/4A and MN2M/6A, the inputs to PLA pins 9 and 10 are derived from tone decoders DM1/1A and DM1/1B. In this case a programme level below −35 dB is indicated by tone *B* and this produces an output of value *0* from the DM1/1B. The required sequence is obtained by connecting this output to PLA pin 10 and the DM1/1A output to PLA pin 9. The result is shown in Table 3.

Elements G H I P Q R S T on card A are invertors to give correct inputs to elements A to O on card B.

The elements on card B are arranged in three groups of five, A to E, F to J and K to O. One input to each of the elements A to E is fed from element G on card A, representing high level reference programme. The other input of each of the elements A to E on card B is fed from one of the elements P to T on card A representing the five levels of the compared programme. For high level reference programme, value *1* is applied to the commoned input, and for compared programme levels of −6 and −12 dB, value *1* is applied to the second input of elements A and B respectively. With both inputs at value *1*, the outputs are at value *0*, and this causes the green lamp ILP11 to light via delay element W. For lower levels of the compared programme, a second input of value *1* to elements C, D and E will cause the yellow lamp ILP10 to light. A similar action occurs in the other two groups F to J and K to O for the middle and low level regions.

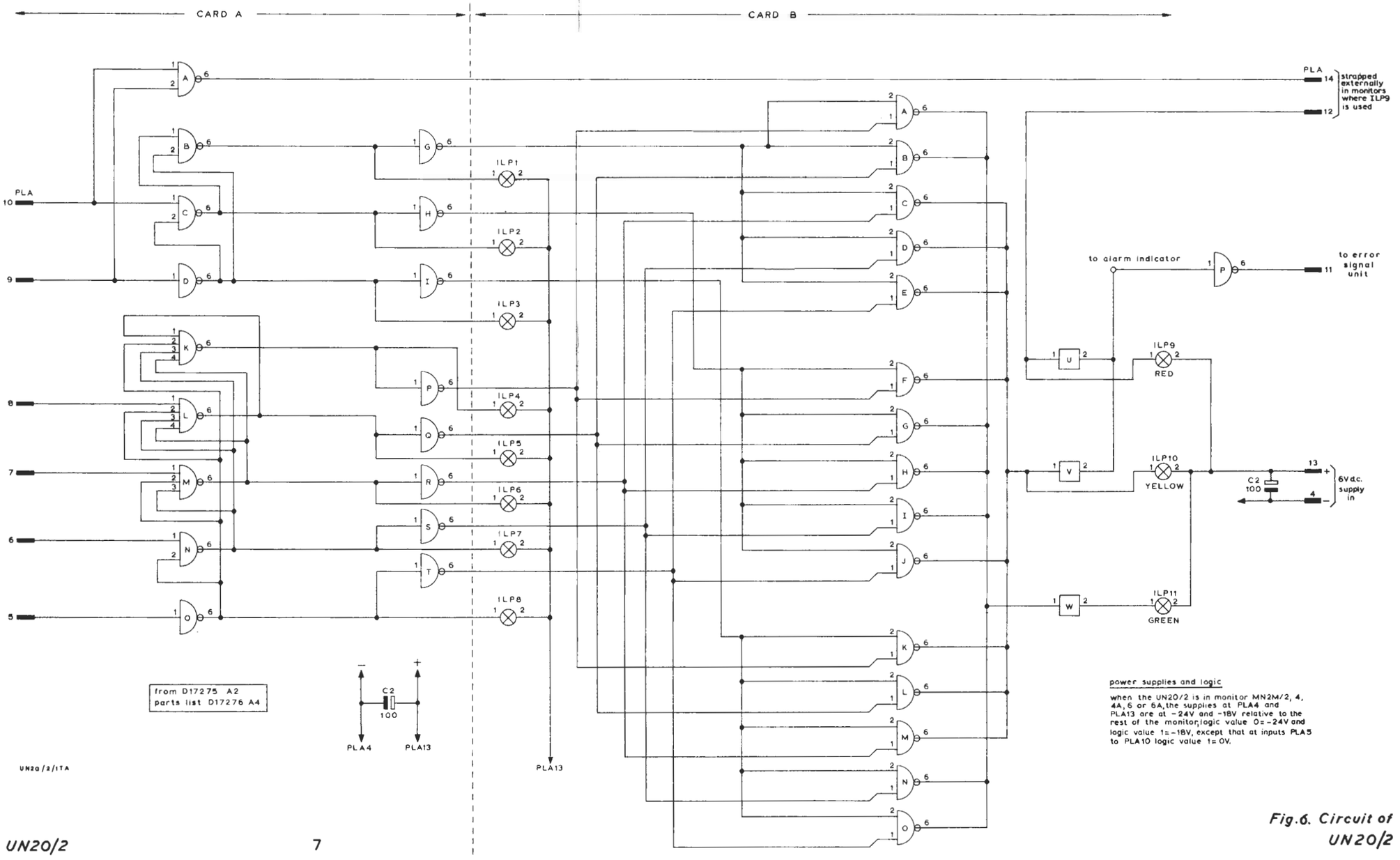

Fig.6. Circuit of UN20/2

The circuit of a delay element is given in Fig. 4. The delay time is that required for C1 to discharge through control RV1 to a voltage determined by D8 and is adjustable up to 25 ms by that control. In particular, the delay in element V is required when a small interval of time separates the arrival of the reference and compared signals, to prevent alarm output signals from the comparator in this interval. In the same circumstances, the delay in element W prevents flickering of the green indicator lamp, ILP10.

The red lamp, ILP9, which indicates the absence of both reference programme tones, is not connected when the UN20/2 is used in an MN2M/2.

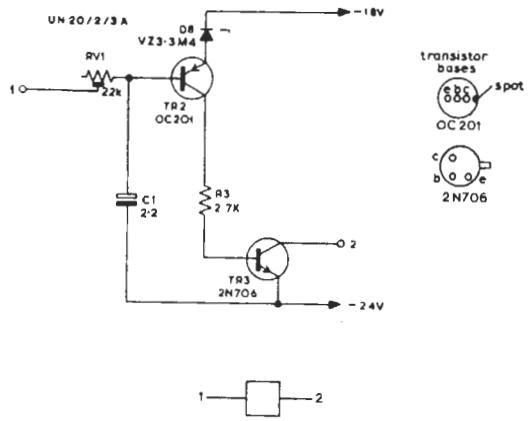

Fig. 4. Output/Delay Elements U–W

Summary of Operation

Indication

(a) The instantaneous levels of the signals at the sending and receiving ends are indicated by lamps ILP1 to ILP3 and ILP4 to ILP8 respectively.

(b) Agreement between sending and receiving levels is indicated by green lamp ILP11.

(c) A transmission fault resulting in a difference in sending and receiving levels is indicated by yellow lamp ILP10.

(d) Failure in the sending end generation of tones, in the transmission path, or in the receiving end tone decoding is indicated by red lamp ILP9. (Except in an MN2M/2.)

Fault Alarm

Under fault conditions, the signal which causes the yellow lamp to light is passed through delay element V and invertor P and forms an output to an error signal unit. The invertor is required for error signal unit Type UN1/99 which requires an input at value *1* to indicate a fault.

The tone failure signal is also passed to the UN1/99, through delay element U.

Test Specification

Power Supply

The unit requires a power supply of 6 volts d.c. connected to PLA pin 13 (positive) and pin 4 (negative). The total current consumption is 350 ±50 mA.

Test Procedure

A full test of the comparator requires the simulation of the 15 possible states arising from the comparison of the three sending levels and five receiving levels. This may be achieved by connecting together pins on plug PLA as detailed in Table 4, and observing the indicating-lamps. (See Fig. 5.) The table also shows the voltage which appears on PLA pin 11 (relative to pin 4).

The information given in the table is applicable to the UN20/2 when tested separately. It does not exactly duplicate the conditions obtaining in all cases when the unit is fitted in a complete monitoring equipment.

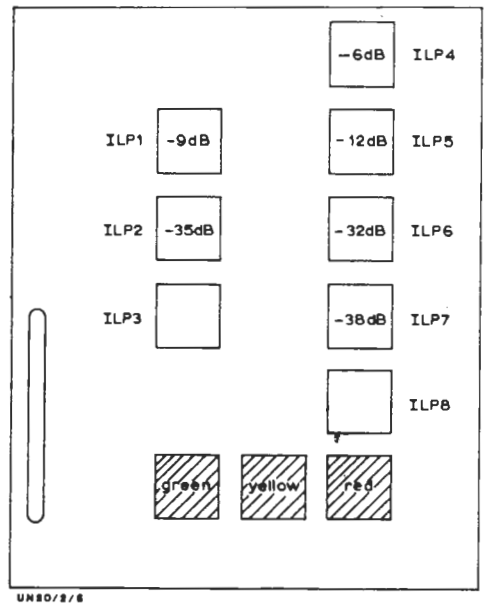

Fig. 5. Indicating Lamps on UN20/2 Front Panel

The variable delay of a delay element, particularly V, can be checked if an oscilloscope is available. To check the delay of element V, connect a switch or relay so that it can be used to apply the voltage at PLA pin 4 to PLA pin 9 (as in test 10, Table 4) and simultaneously to the trigger input of the oscilloscope. By observing the output from terminal 2 of the delay element on the oscilloscope, the delay can be measured. The delay elements of the UN20/2 are finally adjusted as part of the setting-up procedure of the complete monitoring system in which the UN20/2 is installed.